

STM-1 Optical/Mux Unit Type 2

131–8682/xx

General Information

The Unit operates as a fibre optic line terminal and processor (multiplexing/demultiplexing) for the 155Mbit/s STM-1 level.

The treated signal is compliant with ITU-T Recommendation G.957.

————— *For the further details about the STM-1 signal characteristics refer to chapter "Information for the System Engineer"*

The incoming 155Mbit/s signal is processed to manage 1st, 2nd and 3rd level Tributary Units (1.5, 2, 6, 34 or 45Mbit/s) or 3rd and 4th level Administrative Units (45 or 140Mbit/s).

The processing functions obtain every path specified in the ETSI and ITU-T recommendations.

The module processing operations are divided into two separate functions.

The first allows processing at STM-1 level; on the receive side the incoming STM-1 stream is aligned, de-scrambled. On the transmission side the opposite processing is carried out.

The STM-1 so obtained is demultiplexed up to VC-4 level and vice versa. This function is developed by the MUX 1 ASIC.

The second function allows processing from VC3-4 level to TU 1-2-3 level (1.5, 2, 6, 34 or 45Mbit/s Tributary Units) and vice versa, including rej justification and control of the tributary Unit. This function is developed by the TU REJ component.

The Unit supports various protection schemes:

- ◆ *automatic MS Protection of the line (if an extra protection unit is installed);*
- ◆ *duplicate interfaces to the Switch Unit;*
- ◆ *SNCP of the Tributary Units with a signal issued in both connection directions (EAST and WEST).*

The Unit also carries out diagnosis of the Switch Unit.

The Unit supervision functions are managed by a MICROCONTROLLER which communicates with the Communication and Control Unit by means of the Control Bus, a serial bus duplicated for separating the receive and transmit lines.

The unit is composed by a basic PCB that can be fitted with different optical devices and optical connectors in order to realize the interfaces according to the

ITU–T Recommendations; in the following the different interfaces are listed with the relevant identification code of the units.

- ◆ *second window long haul version with FC/PC connectors*
(ITU–T Rec. G.957 – Section L–1.1) cod. 131–8682/01
- ◆ *second window long haul version with SC/PC connectors*
(ITU–T Rec. G.957 – Section L–1.1) cod. 131–8682/21
- ◆ *third window long haul version with FC/PC connectors*
(to be also used with dispersion shifted optical fibre)
(ITU–T Rec. G.957 – Section L–1.2/1.3) cod. 131–8682/02
- ◆ *third window long haul version with SC/PC connectors*
(to be also used with dispersion shifted optical fibre)
(ITU–T Rec. G.957 – Section L–1.2/1.3) cod. 131–8682/22
- ◆ *second window short haul version with FC/PC connectors*
(ITU–T Rec. G.957 – Section S–1.1) cod. 131–8286/03
- ◆ *second window short haul version with SC/PC connectors*
(ITU–T Rec. G.957 – Section S–1.1) cod. 131–8286/23

Functions

The Unit performs the following functions:

Transmit Side

- ◆ *Acceptance of one STM–1 equivalent streams incoming both from the Switch Unit A (main) and the Switch Unit B (stand-by);*
- ◆ *Automatic selection between the two groups of streams A and B by means of quality check or software command;*
- ◆ *Conversion of the STM–1 equivalent stream from the 38.88Mbit/s four wires format to 19.44Mbit/s on eight wires;*
- ◆ *Processing of the High Order POH for the STM–1 equivalent stream;*
- ◆ *Generation of a pointer for the Administrative Unit of the STM–1 equivalent stream;*
- ◆ *Reconverting from 19.44Mbit/s to 38.88Mbit/s four wires format;*
- ◆ *Calculation of the BIP–8 and insertion of the B1 byte in the frame;*
- ◆ *Scrambling of the resulting signal;*
- ◆ *Parallel/serial conversion of the four 38.88Mbit/s streams into one 155.520Mbit/s;*
- ◆ *Conversion of the 155Mbit/s electrical NRZ signal by means of a diode laser into an optical signal;*

- ◆ *Internal regulation of laser emitted power.*

Receive Side

- ◆ *Conversion of incoming 155Mbit/s optical signal into an electrical NRZ signal via an PIN-FET;*
- ◆ *Checking the received power with consequent PIN driving voltage adjustment;*
- ◆ *Detection of missing received pulses;*
- ◆ *Check of incoming signal power;*
- ◆ *Parallel/serial conversion of the incoming 155Mbit/s into four 38.88Mbit/s parallel streams;*
- ◆ *Realignment of the frame with reference to the A1 and A2 word;*
- ◆ *Descrambling of the frame;*
- ◆ *BIP-8 error calculation on B1 byte;*
- ◆ *Calculation and processing of the bytes B2 (BIP-24), J0 (Regenerator Section Trace), J1 (High Order Path Trace), F1 (User Service Channel), K1 and K2 (Automatic Protection Switching Protocol);*
- ◆ *Processing of the pointer for the Administrative Unit of the STM-1 equivalent stream;*
- ◆ *Rejustification of the individual Tributary Units (TU-1-2-3);*
- ◆ *Duplication of the resulting signal to be sent to both Switch Units A and B as four STM-1 equivalent streams at 38.88Mbit/s on four wire format.*

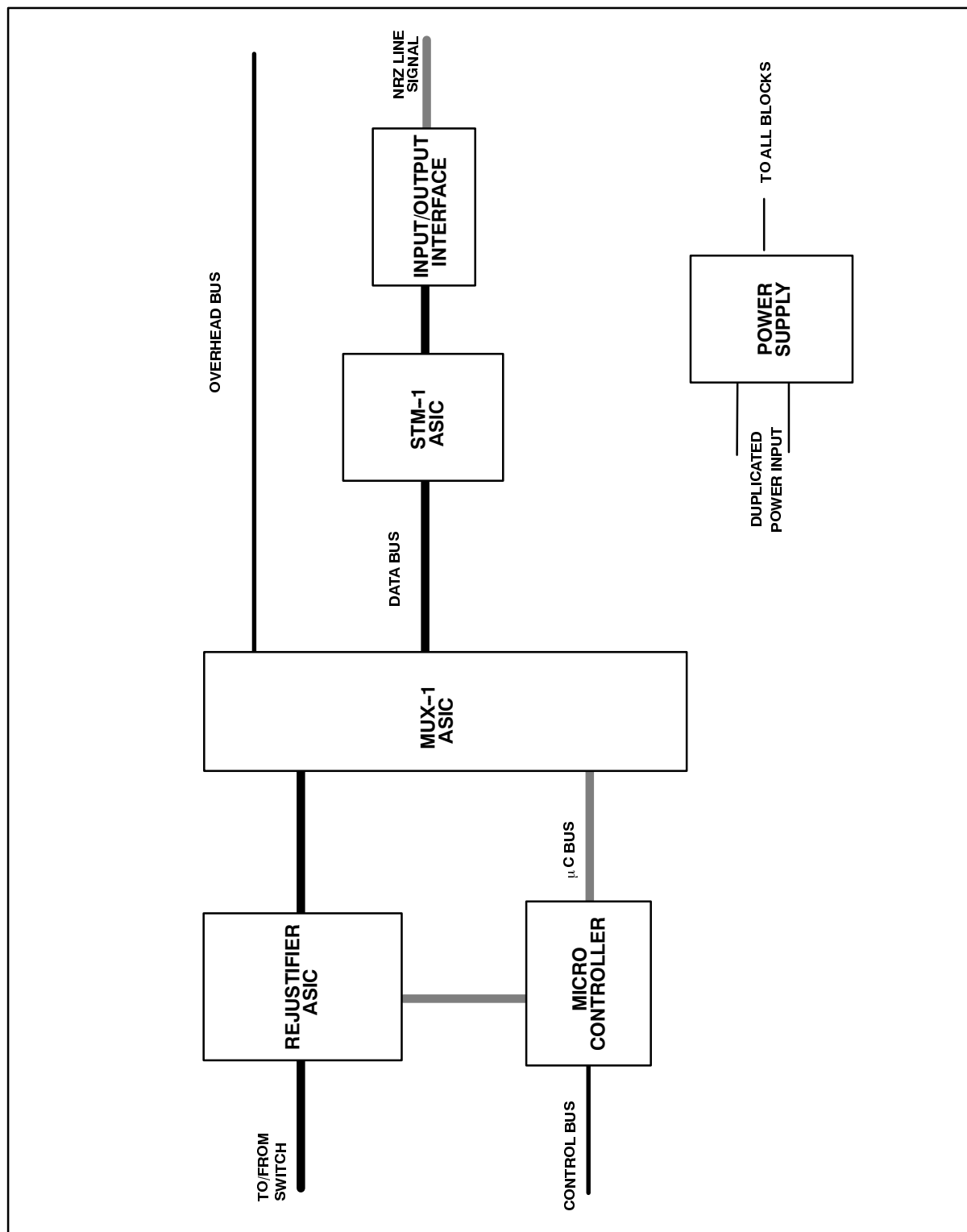


Fig. 5.6-1 Simplified block diagram of STM-1 Optical Mux Unit Type 2

Functional Description

In this paragraph reference will be made to the following block diagrams.

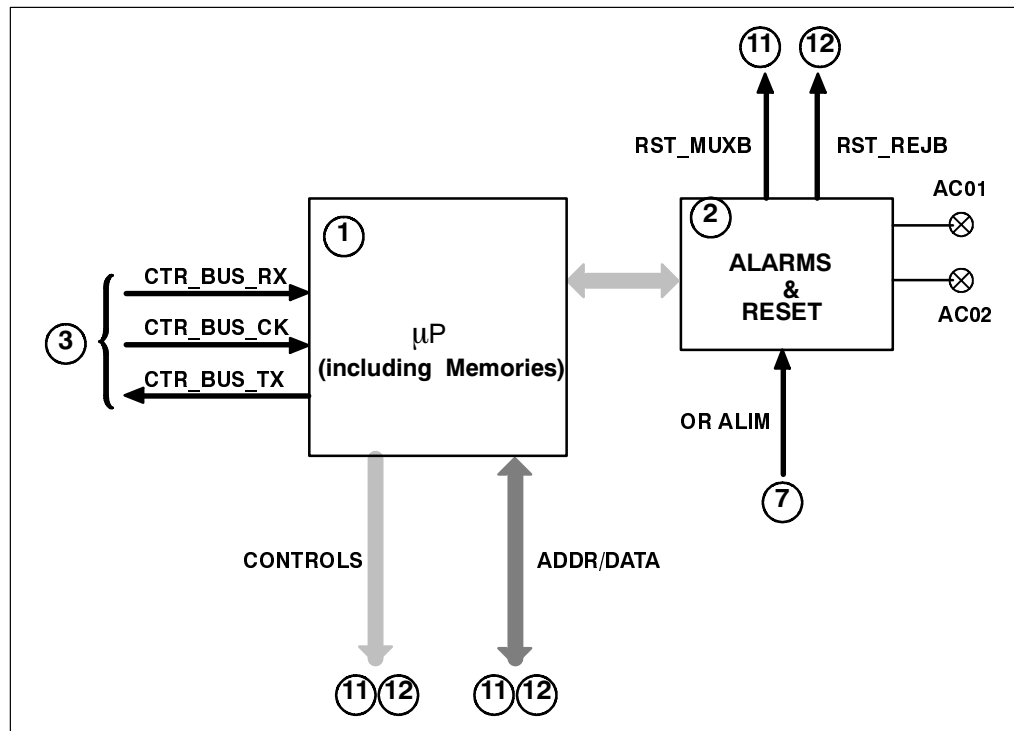


Fig. 5.6-2 Central microprocessor and alarms

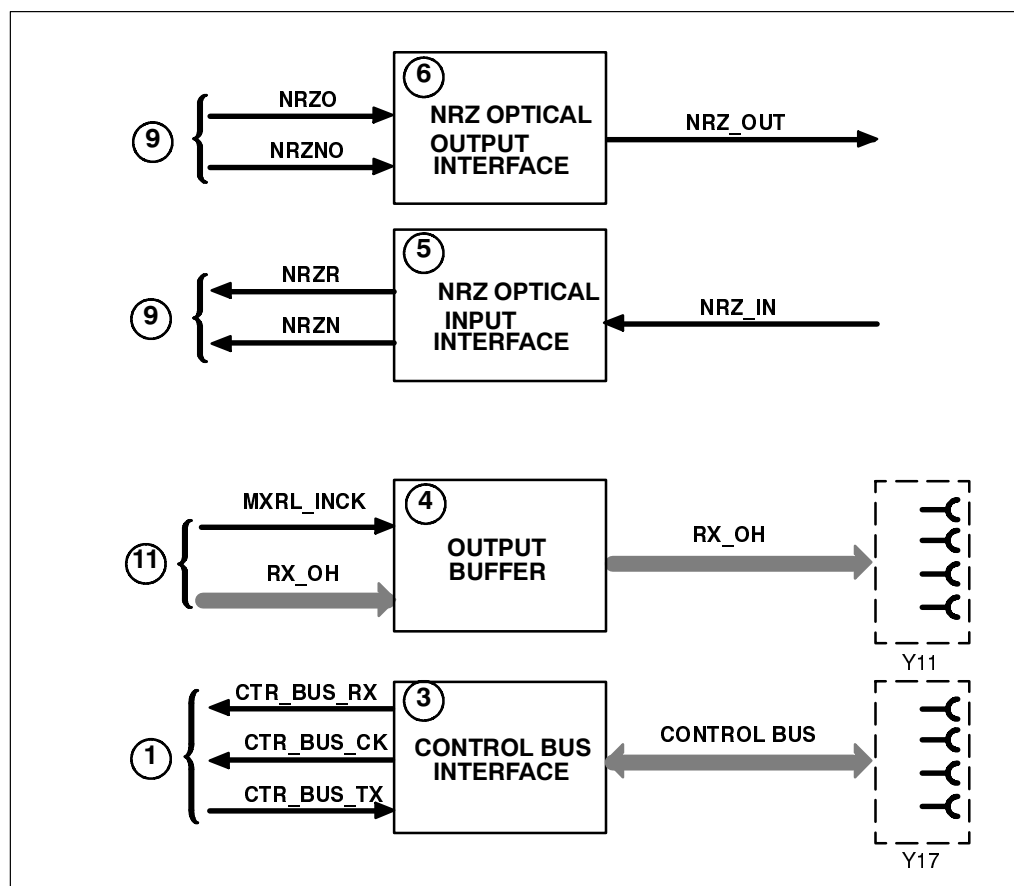


Fig. 5.6-3 Input/output interfaces

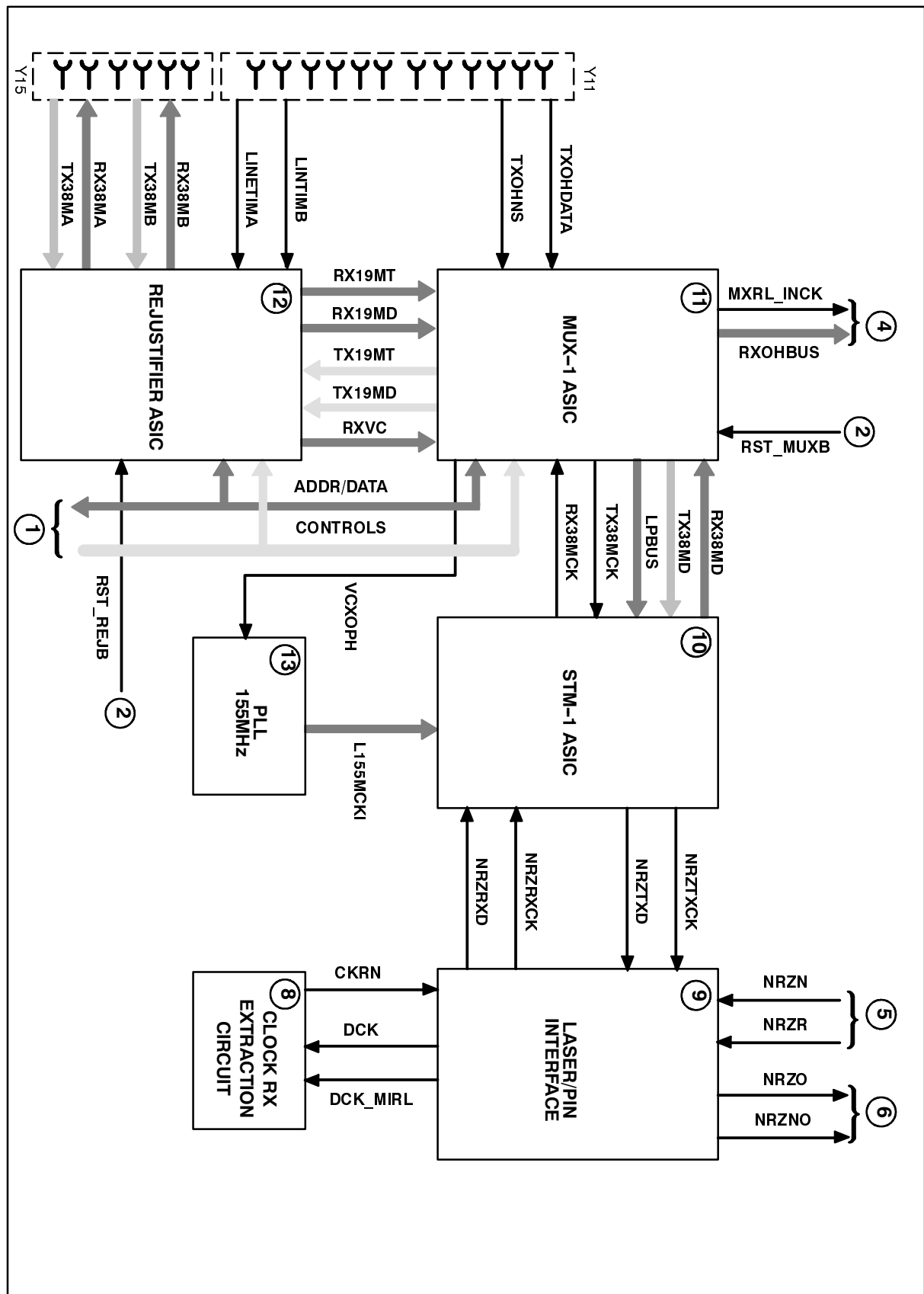


Fig. 5.6-4 Signal processing

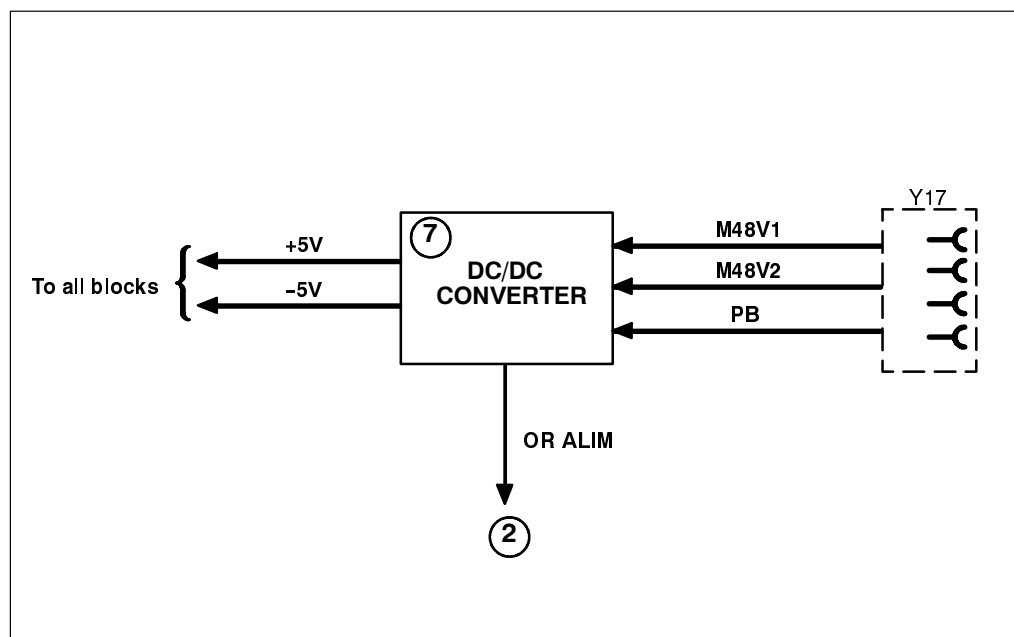


Fig. 5.6-5 *Power supply*

Reception Functions

The incoming STM-1 NRZ optical signal is received on block 6, which converts it from optical to electrical. The NRZ signal is sent towards block 9, by means of signals **NRZN** and **NRZR**.

On block 9 preforms the clock extraction from the incoming NRZ signal and sends it towards block 10, by means of signals **NRZRXD** for the data and **NRZRXCK** for the timing.

In addition, block 9 sends the signals **DCK** and **DCK_MIRL** towards block 8, which extracts clock and reveals an eventual loss of pulses.

The informations about clock are sent towards block 10 by means of signal **NRZRXCK**.

On block 10 the NRZ signal is converted from a serial to a parallel format, sending a 38.88Mbit/s data signal (**RX38MD**) and a 38.88Mhz clock signal (**RX38MCK**) towards block 11.

On block 11 the first operation is the extraction and check of alignment word (bytes A1 and A2 of SOH).

Then a descrambling operation is performed and the SOH bytes are extracted.

The following operation are performed on these bytes:

- ◆ *Bytes B1 and B2 are directly processed by the Optical Mux Unit, which emits any possible alarm indication*

- ◆ *Bytes for MSP signalling (K1 and K2), are sent, via the internal STM-1 streams, towards the switch circuits of the equipment.*
- ◆ *Byte J0 (Section Trace Identifier) is extracted and elaborated in order to detect any eventual mismatch between received and expected values*
- ◆ *The remaining bytes are issued to the OVERHEAD BUS*

After the SOH processing, the MUX ASIC processes the Administrative Unit pointer and, eventually, performs an Administrative Unit rejustification, in order to synchronize the STM-1 payload with the clock signal received from the synchronization circuit of the equipment.

Once the payload is synchronized, the MUX ASIC extracts the POH of the higher order Virtual Container. The content of this POH is then elaborated and issued on the CONTROL BUS and on the OVERHEAD BUS.

The payload of higher order Virtual Container is passed into a 8-bit format and it is sent towards block 12 (REJUSTIFIER ASIC) by means of **TX19MD** bus (at a 19.44Mbit/s bit rate).

On the REJUSTIFIER ASIC the TU POH and pointer are processed. The overhead informations are sent on the OVERHEAD BUS (on the **RXOHBUS**) and, after pointer interpretation, the TU payload is rejustified, in order to ensure a synchronization of incoming signal with the clock used by the switch.

From block 12 the signal is issued towards the two switch circuits of the equipment on 4-bit buses (**RX38MA** and **RX38MB**), at a bit rate of 38.88Mbit/s.

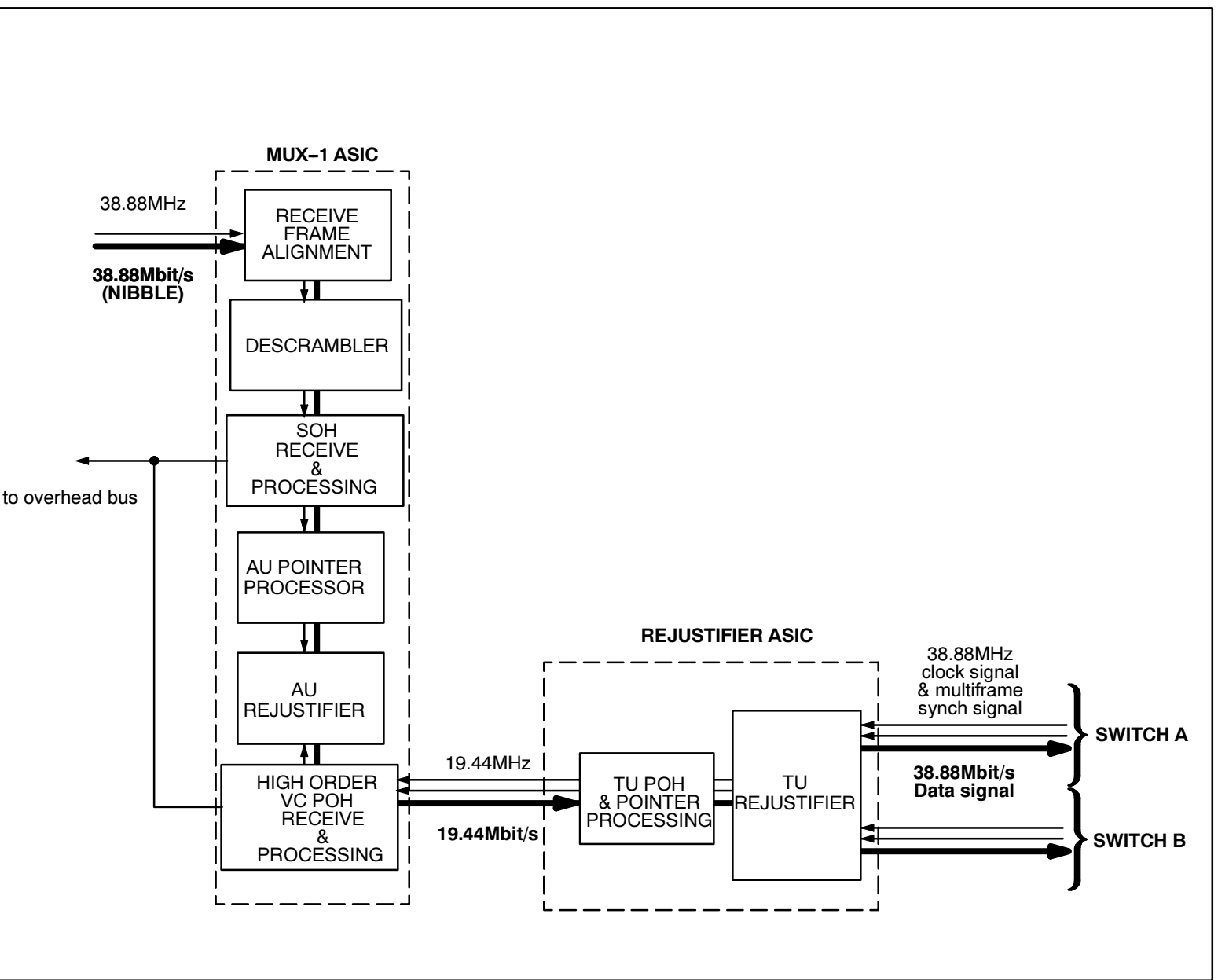


Fig. 5.6-6

Simplified block diagram of MUX-1 ASIC and REJUSTIFIER ASIC – Receive side

Transmission Functions

On block 12 are received two 8-bit buses (**RX38MA** and **RX38MB**) at a bit rate of 38.88Mbit/s, from the two switch circuits of the equipment. To each data signal are paired a multi-frame synchronization signal and a 38.88MHz clock signal.

The REJUSTIFIER ASIC performs a check to determine which signal has to be used, the one from the switch circuit A or the one from switch circuit B. The results of this check is issued on the CONTROL BUS, to the working controller circuit of the equipment, which makes this information available to NMC and Local Controller.

The transmit signal has not to be rejustified, so the REJUSTIFIER ASIC only adds the Tributary Unit POH, and issues a 8-bit bus (with a bit rate of 19.44 Mbit/s) towards block 11 (MUX ASIC).

The MUX ASIC adds the Higher Order VC Overhead, to the TU (the Overhead bytes come from the OVERHEAD BUS on **TXOHDATA**), then adds the AU pointer and the SOH.

The obtained signal is sent towards block 10 (STM-1 ASIC), on **TX38MD**, a 4-bit bus (at a bit rate of 38.88MHz). The STM-1 ASIC converts the signal from a parallel to a serial format and sends it towards the block 9.

Block 9 converts the serial signal **NRZTXD** to the current for driving the laser module and issues it to the output interface (block 4), by means of the signals **NRZO** and **NRZNO**.

The output interface converts the incoming electrical signal into the optical signal using a laser diode.

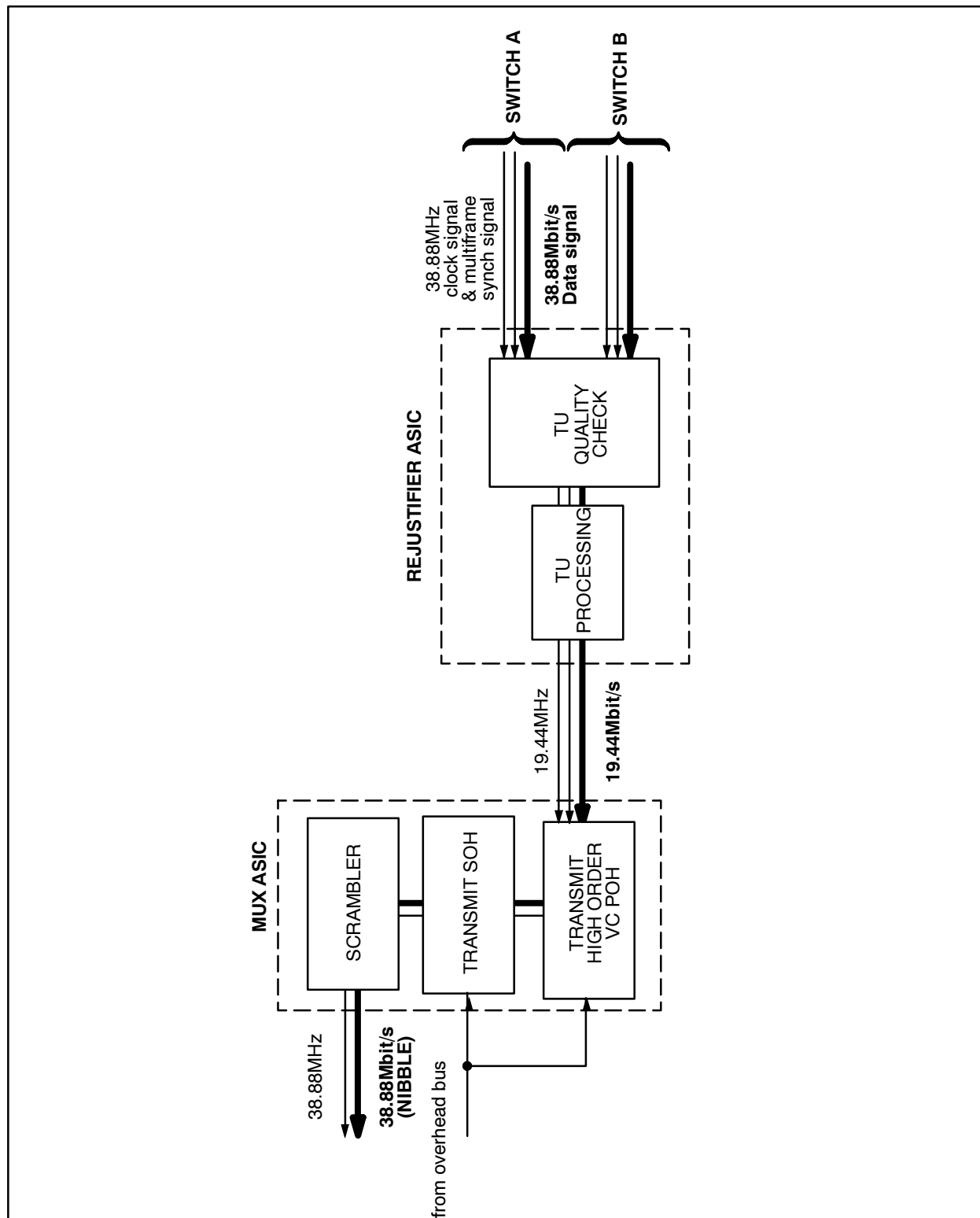


Fig. 5.6-7 Simplified block diagram of MUX ASIC and REJUSTIFIER ASIC- Transmit side

Common Functions

Switch Unit Diagnostic Analysis

The Optical/Mux Unit is provided with a Switch diagnostic analysis function, which is developed in the Tributary Unit Rejustifier ASIC.

This function involves checking the information contained in a control byte present in the path-information (POH – Path Overhead) of each individual Virtual Container. Any discrepancies between the expected and received values is reported to the working controller circuit of the equipment.

DC/DC Converter

The Optical/Mux Unit is provided with a on-board DC/DC converter. This converter accepts an incoming –48V supply voltage and provides +5V and –5.2V supply voltages to all the components on the card.

Timing Functions

The Optical/Mux Unit is provided with a 19.44MHz VCXO and a 155.52MHz VCO.

Technical Characteristics

Microprocessor And Memories

Microprocessor: Motorola 68302

Data Memory: 2 x 128kbyte RAM

Program Memory: 2 x 512kbyte FLASH

Bootstrap Memory: 1 x 128kbyte EPROM

Inventory Memory: 1 x 8kbit EPROM

Back-up Memory: 1 x 8kbyte EEPROM