

# STM-1 G.703 Electrical Unit-Type 2

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## General Information

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The Electrical/Mux Unit operates as an Electrical (CMI code) tributary and processor (multiplexing/demultiplexing) for the 155.520Mbit/s STM-1 first level synchronous transport module.

The treated signal is compliant with ITU-T Recommendation G.703.

————— *For the further details about the STM-1 signal characteristics refer to chapter "Information for the System Engineer"*

————— *The Electrical/Mux Unit can be fitted both into ADM-1 and ADM-4/1 equipment; therefore in this description the terms MOST Unit for the ADM-1 (main and stand-by when the protection is provided) and Communication and Control Unit or Switch Unit for the ADM-4/1 will be used. The proper correspondence will be specified with notes.*

# Functions

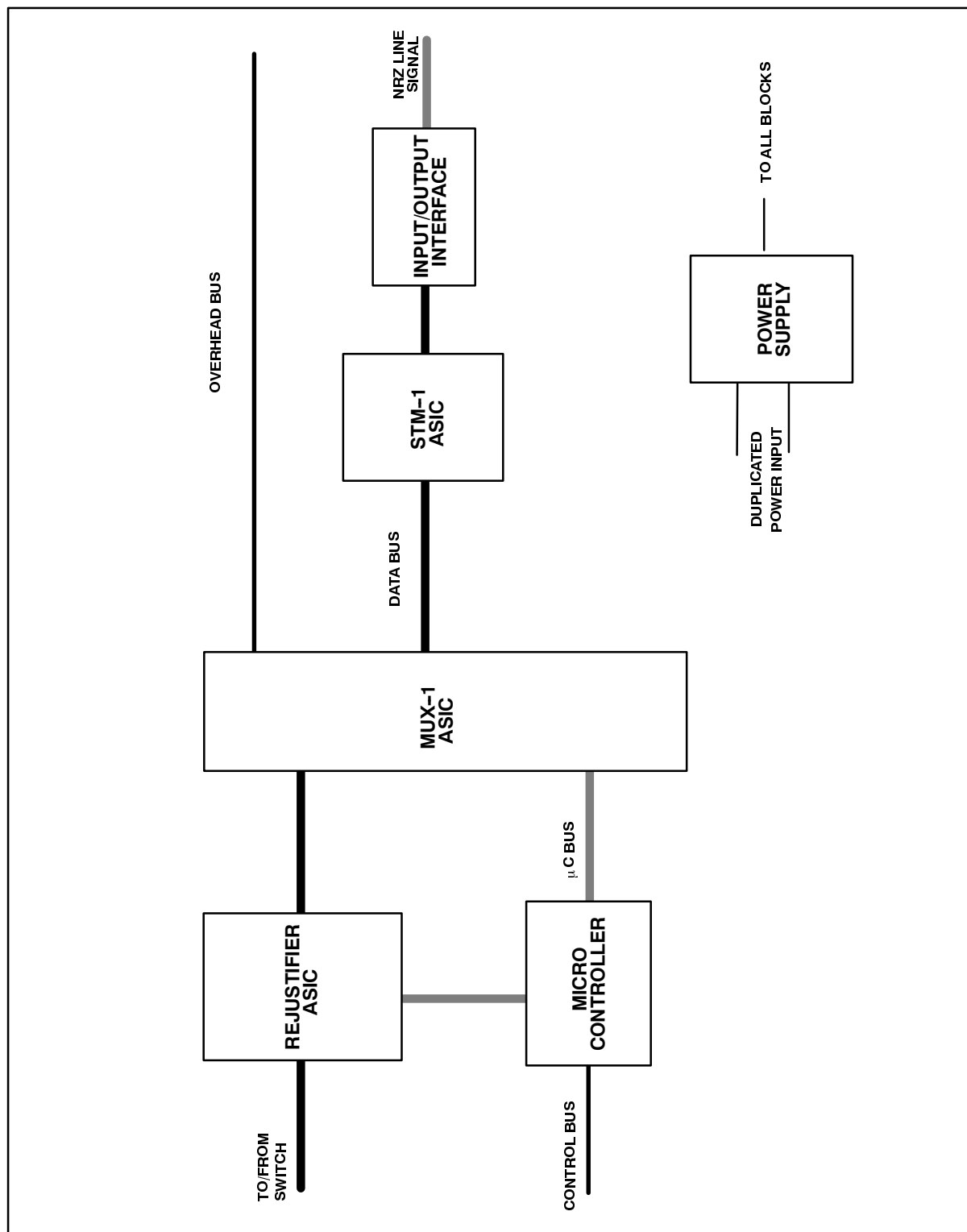
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The Electrical/Mux Unit supports the following functions:

- ◆ *Reception/Transmission of an electrical 155Mbit/s CMI signal*
- ◆ *Conversion of incoming 155Mbit/s signal from CMI to NRZ code*
- ◆ *Conversion of outgoing 155Mbit/s signal from NRZ to CMI code*
- ◆ *Processing from STM-1 level to VC-4.*
- ◆ *Processing from VC-4 level to TU-12, including rejustification and TU control.*
- ◆ *Processing from TU-12 level to VC-4, with insertion of control and justification bits.*
- ◆ *Processing from VC-4 level to STM-1.*
- ◆ *Unit supervision by means of a microprocessor communicating with the working controller circuit of the equipment (\*)*
- ◆ *Card Power Supply by means of a DC/DC converter, present on the card itself.*
- ◆ *Management of interfaces towards the Control Bus and the switch circuits of the equipment (\*\*)*
- ◆ *Internal clock generation*

**NOTE (\*)** *MOST Units (main and stand-by) for the ADM-1 – Communication and Control Unit for the ADM-4/1.*

**NOTE (\*\*)** *MOST Units (Main and Stand-by) for the ADM-1 – Switch Units (Main and Stand-by) for the ADM-4/1.*



**Fig. 5.5-1** Simplified block diagram of STM-1 Electrical Mux Unit Type 2

# Functional Description

In this paragraph reference will be made to the following block diagrams.

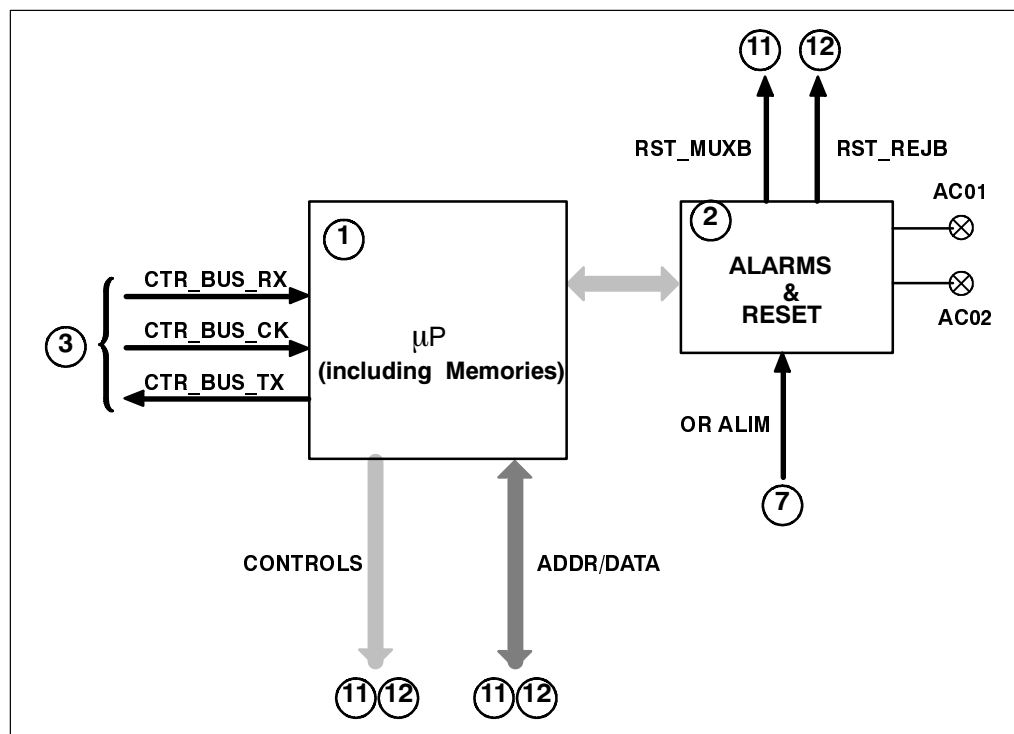


Fig. 5.5-2 Central microprocessor and alarms

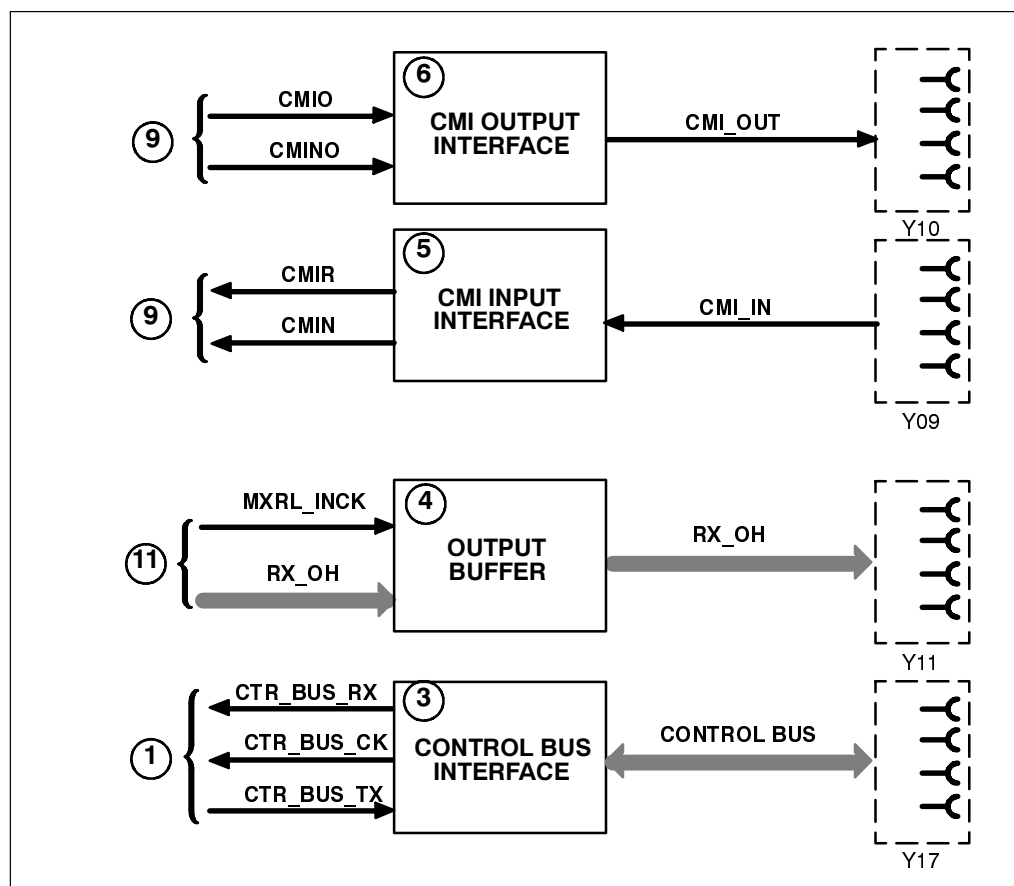


Fig. 5.5-3 Input/output interfaces

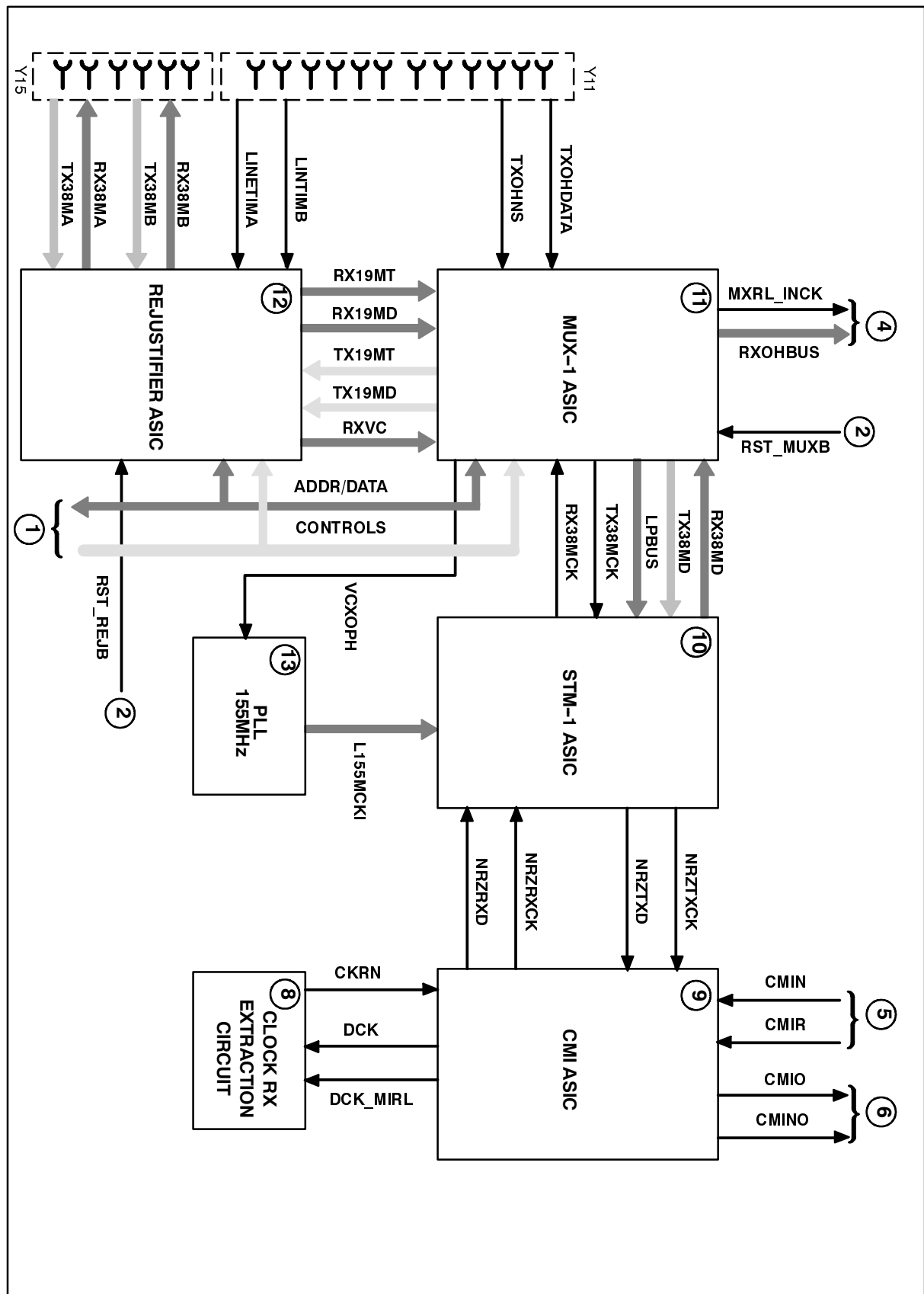


Fig. 5.5-4 Signal processing

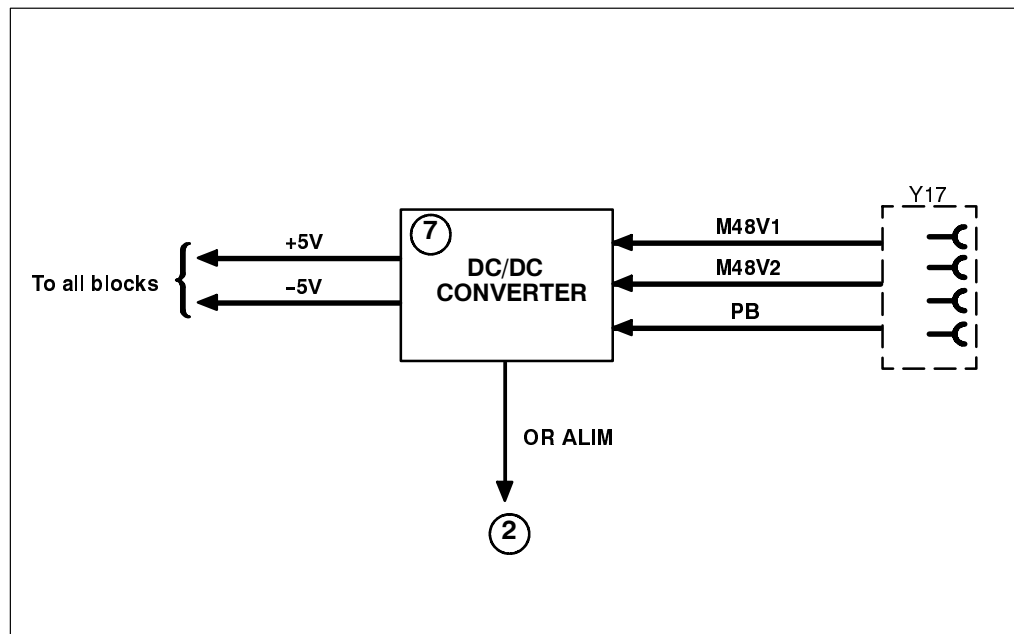


Fig. 5.5-5 Power supply

## Reception Functions

The incoming STM-1 CMI signal is received on block 6, which ensures an impedance matching. The CMI signal is sent towards block 9, by means of signals **CMIN** and **CMIR**.

On block 9 the CMI signal is converted into NRZ code and it is sent towards block 10, by means of signals **NRZRXD**.

In addition, block 9 sends the signals **DCK** and **DCK\_MIRL** towards block 8, which extracts clock and reveals an eventual loss of pulses.

The informations about clock are sent towards block 10 by means of signal **NRZRXCK**.

On block 10 the NRZ signal is converted from a serial to a parallel format, sending a 38.88Mbit/s data signal (**RX38MD**) and a 38.88Mhz clock signal (**RX38MCK**) towards block 11.

On block 11 the first operation is the extraction and check of alignment word (bytes A1 and A2 of SOH).

Then a descrambling operation is performed and the SOH bytes are extracted.

The following operation are performed on these bytes:

- ◆ Bytes *B1* and *B2* are directly processed by the Electrical Mux Unit, which emits any possible alarm indication
- ◆ Bytes for MSP signalling (*K1* and *K2*), are sent, via the internal STM-1 streams, towards the switch circuits of the equipment (\*\*)

- ◆ *ByteJ0 (Section Trace Identifier) is extracted and elaborated in order to detect any eventual mismatch between received and expected values*
- ◆ *The remaining bytes are issued to the OVERHEAD BUS*

After the SOH processing, the MUX ASIC processes the Administrative Unit pointer and, eventually, performs an Administrative Unit rejustification, in order to synchronize the STM-1 payload with the clock signal received from the synchronization circuit of the equipment (\*\*).

Once the payload is synchronized, the MUX ASIC extracts the POH of the higher order Virtual Container. The content of this POH is then elaborated and issued on the CONTROL BUS and on the OVERHEAD BUS.

The payload of higher order Virtual Container is passed into a 8-bit format and it is sent towards block 12 (REJUSTIFIER ASIC) by means of **TX19MD** bus (at a 19.44Mbit/s bit rate).

On the REJUSTIFIER ASIC the TU POH and pointer are processed. The overhead informations are sent on the OVERHEAD BUS (on the **RXOHBUS**) and, after pointer interpretation, the TU payload is rejustified, in order to ensure a synchronization of incoming signal with the clock used by the switch.

From block 12 the signal is issued towards the two switch circuits of the equipment (\*\*) on 4-bit buses (**RX38MA** and **RX38MB**), at a bit rate of 38.88Mbit/s.

*NOTE (\*) MOST Units (main and stand-by) for the ADM-1 - Communication and Control Unit for the ADM-4/1.*

*NOTE (\*\*) MOST Units (Main and Stand-by) for the ADM-1 - Switch Units (Main and Stand-by) for the ADM-4/1.*

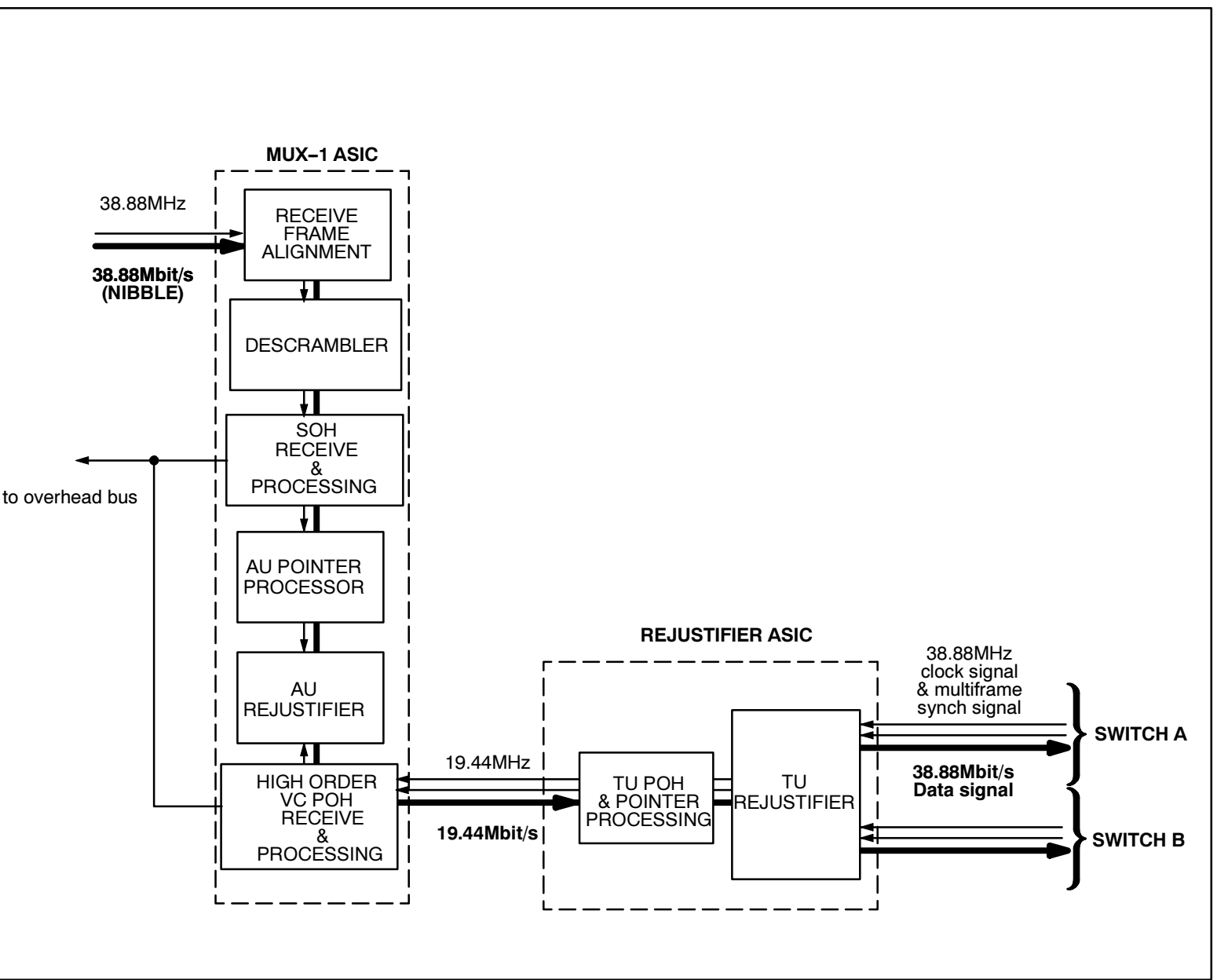


Fig. 5.5-6

Simplified block diagram of MUX-1 ASIC and REJUSTIFIER ASIC - Receive side



## Transmission Functions

On block 12 are received two 8-bit buses (**RX38MA** and **RX38MB**) at a bit rate of 38.88Mbit/s, from the two switch circuits of the equipment (\*\*). To each data signal are paired a multi-frame synchronization signal and a 38.88MHz clock signal.

The REJUSTIFIER ASIC performs a check to determine which signal has to be used, the one from the switch circuit A or the one from switch circuit B (\*\*). The results of this check is issued on the CONTROL BUS, to the working controller circuit of the equipment (\*), which makes this information available to NMC and Local Controller.

The transmit signal has not to be rejustified, so the REJUSTIFIER ASIC only adds the Tributary Unit POH, and issues a 8-bit bus (with a bit rate of 19.44 Mbit/s) towards block 11 (MUX ASIC).

The MUX ASIC adds the Higher Order VC Overhead, to the TU (the Overhead bytes come from the OVERHEAD BUS on **TXOHDATA**), then adds the AU pointer and the SOH.

The obtained signal is sent towards block 10 (STM-1 ASIC), on **TX38MD**, a 4-bit bus (at a bit rate of 38.88MHz). The STM-1 ASIC converts the signal from a parallel to a serial format and sends it towards the CMI ASIC (block 9).

CMI ASIC converts the serial signal **NRZTXD** from NRZ code to CMI code and issues it to the output interface (block 4), by means of the signals **CMIO** and **CMINO**.

The output interface issues the signal **CMI\_OUT** on the electrical STM-1 line.

*NOTE (\*) MOST Units (main and stand-by) for the ADM-1 – Communication and Control Unit for the ADM-4/1.*

*NOTE (\*\*) MOST Units (Main and Stand-by) for the ADM-1 – Switch Units (Main and Stand-by) for the ADM-4/1.*

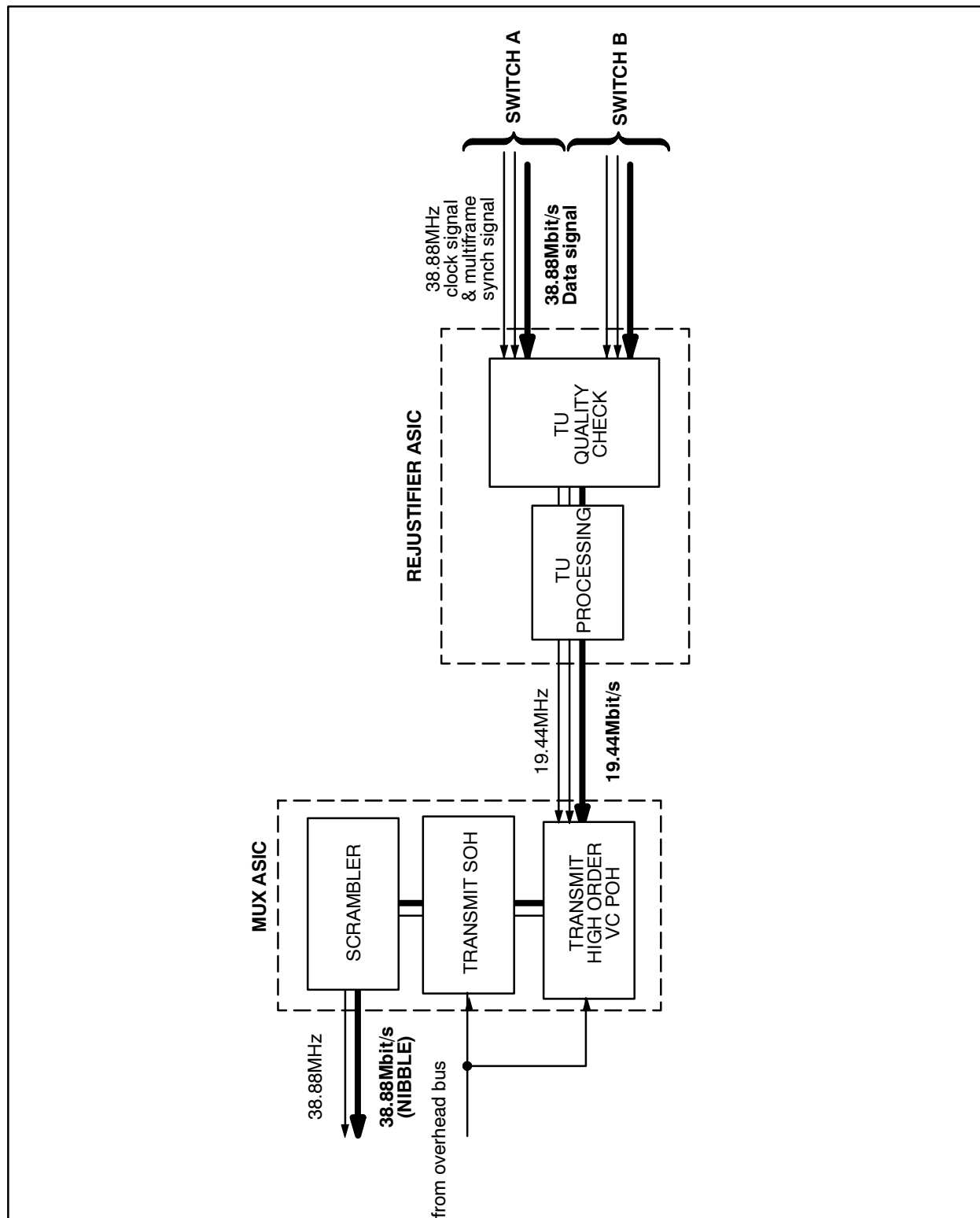


Fig. 5.5-7 Simplified block diagram of MUX ASIC and REJUSTIFIER ASIC- Transmit side

## Common Functions

### Switch Unit Diagnostic Analysis

The Electrical/Mux Unit is provided with a Switch diagnostic analysis function, which is developed in the Tributary Unit Rejustifier ASIC.

This function involves checking the information contained in a control byte present in the path-information (POH – Path Overhead) of each individual Virtual Container. Any discrepancies between the expected and received values is reported to the working controller circuit of the equipment (\*).

**NOTE (\*)** *MOST Units (main and stand-by) for the MSH11C – Communication and Control Unit for the MSH41C.*

### DC/DC Converter

The Electrical/Mux Unit is provided with a on-board DC/DC converter. This converter accepts an incoming –48V supply voltage and provides +5V and –5.2V supply voltages to all the components on the card.

### Timing Functions

The Electrical/Mux Unit is provided with a 19.44MHz VCXO and a 155.52MHz VCO.

## Technical Characteristics

### Microprocessor And Memories

*Microprocessor: Motorola 68302*

*Data Memory: 2 x 128kbyte RAM*

*Program Memory: 2 x 512kbyte FLASH*

*Bootstrap Memory: 1 x 128kbyte EPROM*

*Inventory Memory: 1 x 8kbit EPROM*

*Back-up Memory: 1 x 8kbyte EEPROM*

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