

# 3x34Mbit/s Tributary Unit 131–8685/01

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## General Information

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The description refers to the unit block diagram. The numbers shown in the block diagram identify the circuit blocks in the circuit diagram.

The setting devices for the unit are shown in the chapter "Setting Up".

## Function

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The 3x34Mbit/s Tributary Unit performs the function of interfacing, coding and processing 34Mbit/s tributary streams on the receive and transmit sides, on the tributary side it accepts up to 3 34368kbit/s  $\pm 20$ ppm. HDB3 coded channels.

After an NRZ converter this signals are processed and allocated in C3 containers of the STM–1 synchronous module. The POH (Path Information Overhead) is then added, thus obtaining the virtual containers (VC–3), which are issued to the output connector.

The unit alarm and information control functions are managed by an 68302 microprocessor which interfaces with Central Controller Unit of the equipment via a serial bus.

Loop–back circuits for the local, and remote, activation tributaries are included for diagnostic operations.

The 3x34Mbit/s Tributary Unit can manage a 1 + 1 tributary unit protection scheme.

## Transmission

- ◆ *Acceptance, equalization and regeneration of the three 34368kbit/s  $\pm 20$ ppm HDB tributary streams*
- ◆ *extraction of the 34368kHz clock signal from each tributary stream*
- ◆ *monitoring for loss of 34Mbit/s received pulses at the input interface and issue LOSS OF SIGNAL 1 to 3 alarm*
- ◆ *code conversion of 34368kbit/s stream from HDB3 to NRZ*
- ◆ *generation of a 38880kHz clock signal, using a phase locked oscillator circuit, for managing of TRIB34ASIC gate array internal stream processing*

- ◆ *allocation of 34Mbit/s signals to the STM-1 synchronous frame C-3 containers*
- ◆ *insertion of the path-information (POH – Path Overhead) of the VC-3 virtual containers*
- ◆ *issuing of the three 34Mbit/s tributary streams as four duplicated (A – main and B – protection) 38.88Mbit/s data signals to the unit connector*

## Reception

- ◆ *reception of four duplicated (A – main and B – protection) 38.88Mbit/s data signals from the unit connector*
- ◆ *switching between the incoming A and B data signals according with the internal processing of the alarms and commands incoming from the serial bus*
- ◆ *generation of a 34368kHz  $\pm$  20ppm de-jittered clock signal for each of the three streams, using a phase locked oscillator circuit*
- ◆ *extraction of the path-information (POH – Path Overhead) of the VC-3 virtual containers*
- ◆ *extraction of 34Mbit/s signals from the STM-1 synchronous frame C-3 containers*
- ◆ *code conversion of the 34368kbit/s from NRZ to HDB3, and issue of the streams to the output interfaces*
- ◆ *monitoring for loss of 34368kbit/s pulses transmitted to the tributary interfaces and generation of PDH Tx Fail (Loss Of Transmitted Signal) 1 to 3 alarm*

## Common Functions

- ◆ *Unit supervision by means of a microprocessor communicating with the controller circuits of the equipment.*
- ◆ *unit power supply by means of a DC/DC converter, present on the unit itself.*
- ◆ *management of interfaces towards the Control Bus and the two switch matrix circuits of the equipment*

# Functional Description

(See block diagram in Fig. 5.8–5)

## Transmit Side

The 34368kbit/s  $\pm 20$ ppm HDB3 streams, attenuated in the range 0 thru 12dB at 17184kbit/s  $-A \cdot \sqrt{f}$  – are applied to the input interface circuit, respectively blocks 1, 3 and 5, via unit connector.

The incoming signal transits through a variable equalizer which recovers attenuation  $\sqrt{f}$  and generates an equalized signal with controlled amplitude.

Two threshold detectors detect the positive and negative pulses in the HDB3 signal. This pulses are converted to NRZ code on two separate wires (positive and negative pulses) and translated to CMOS levels in order to make them compatible with the TRIB34 ASIC, block 7.

Both the signal pulse sequences contribute in the extraction of the 34MHz clock signal by means of a phase locked oscillator, respectively blocks 2, 4 and 6.

The signal is clipped and converted to CMOS level by a conversion circuit, and applied to the TRIB34 ASIC, block 7.

NRZ signals made available to the block 7, are allocated to a C–3 type container using a justification process.

### Asynchronous mapping of 34368kbit/s tributary into C–3

One 34368kbit/s signal can be mapped into C–3 as shown in NO TAG.

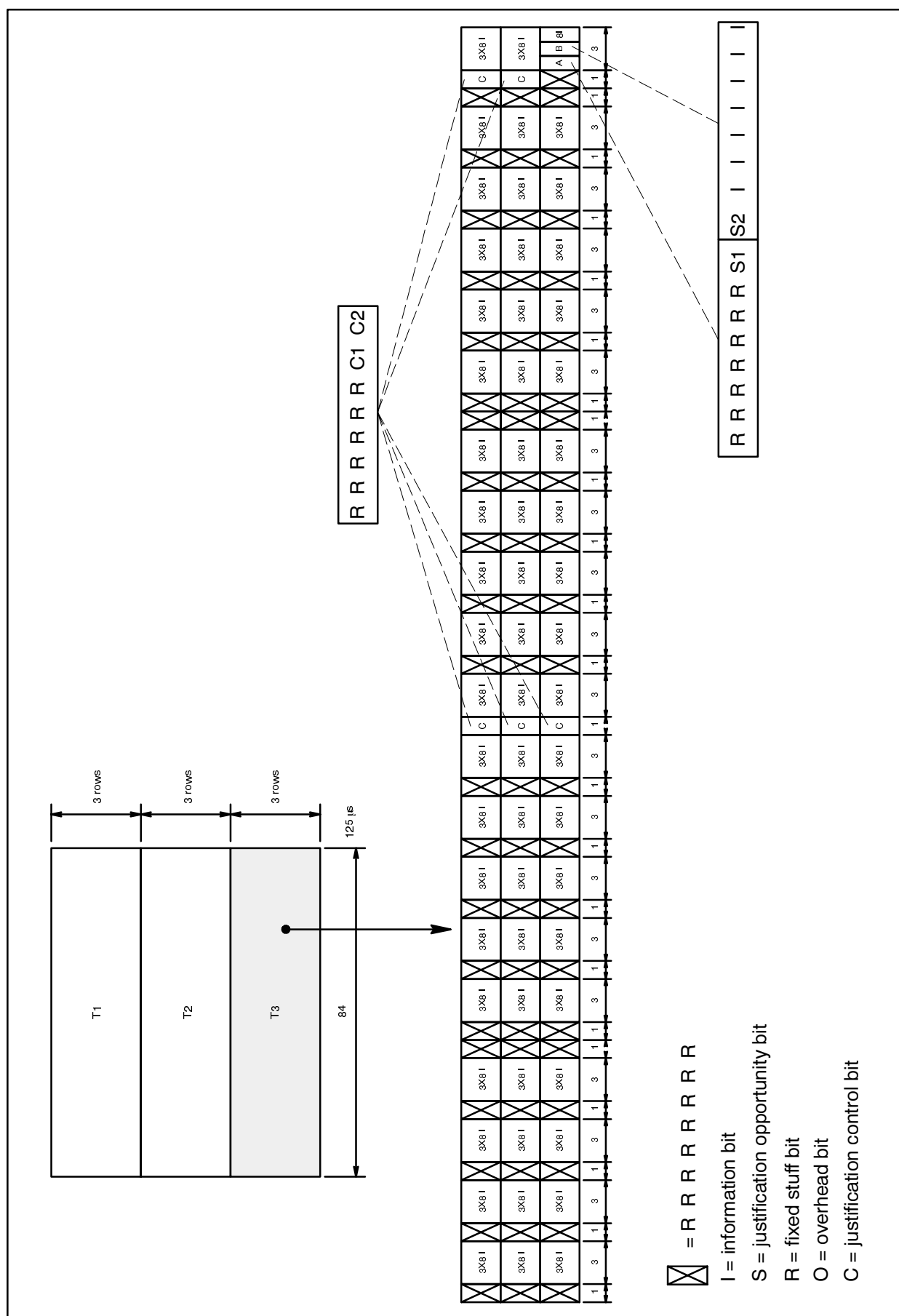
C3 consists of a payload of 9 X 84 bytes every 125 $\mu$ s. This payload is divided in three sub–frames, each sub–frame consisting of:

- 1431 information bits ( $I$ );
- two sets of five justification control bits ( $C_1$ ,  $C_2$ );
- two justification opportunity bits ( $S_1$ ,  $S_2$ );
- 573 fixed stuff bits ( $R$ ).

Two sets of five justification control bits  $C_1$  and  $C_2$  are used to control the two justification opportunity bits  $S_1$  and  $S_2$  respectively.

$C_1C_1C_1C_1C_1 = 00000$  indicates that  $S_1$  is a data bit while  $C_1C_1C_1C_1C_1 = 11111$  indicates that  $S_1$  is a justification bit.  $C_2$  bits control  $S_2$  in the same way. Majority vote should be used to make the justification decision in the de–synchronizer for protection against single and double bit errors in the C bits.

The receive side ignores the value contained in  $S_1$  and  $S_2$  bits whenever they are used as a justification bits.



**Fig. 5.8-1** Allocation of a 34368kbit/s asynchronous tributary to a C-3 .

## VC–3 POH

The path-information (POH), formed of the bits shown in Fig. 5.8–2, is added to each C–3 container to produce a VC–3 Virtual Container and is located in the first column of 9–row by 85–column VC–3 structure.

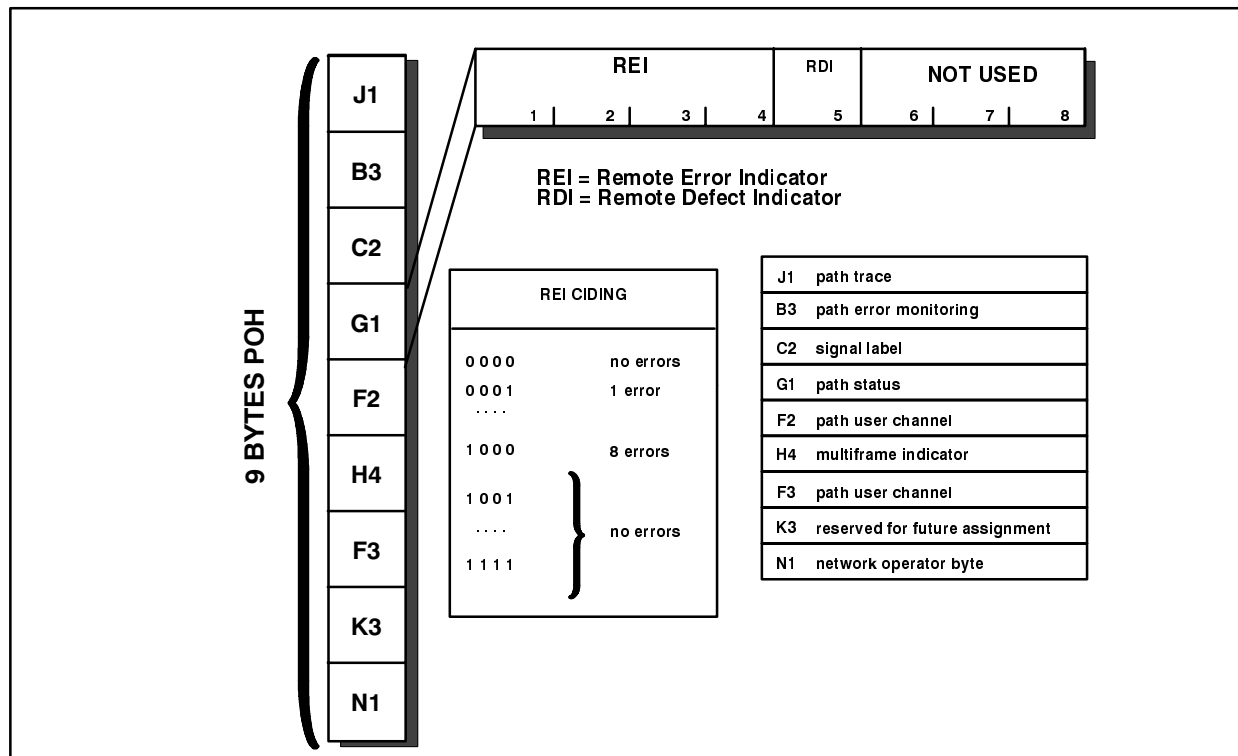


Fig. 5.8–2 Level 3/4 POH – Path Overhead

## TU–3 pointer

A pointer is then added to each VC–3 in order to obtain a TU–3 Tributary Unit.

This pointer allows flexible and dynamic allocation of the VC inside the frame, indicating the shift in bytes between the pointer itself (with a fixed position) and the first VC byte, and also supplies information about the Tributary Unit and any load change.

The positioning and development of the pointer is shown in Fig. 5.8–3.

The TU–3 pointer value contained in H1 and H2 designates the location of the byte where the VC–3 begins. The two bytes allocated to the pointer function can be viewed as one word as shown in Fig. 5.8–3. The last ten bits (bits 7 – 16) of the pointer word carry the pointer value.

The TU–3 pointer value is a binary number with a range of 0 – 764 which indicates the offset between the pointer and the first byte of the VC–3.

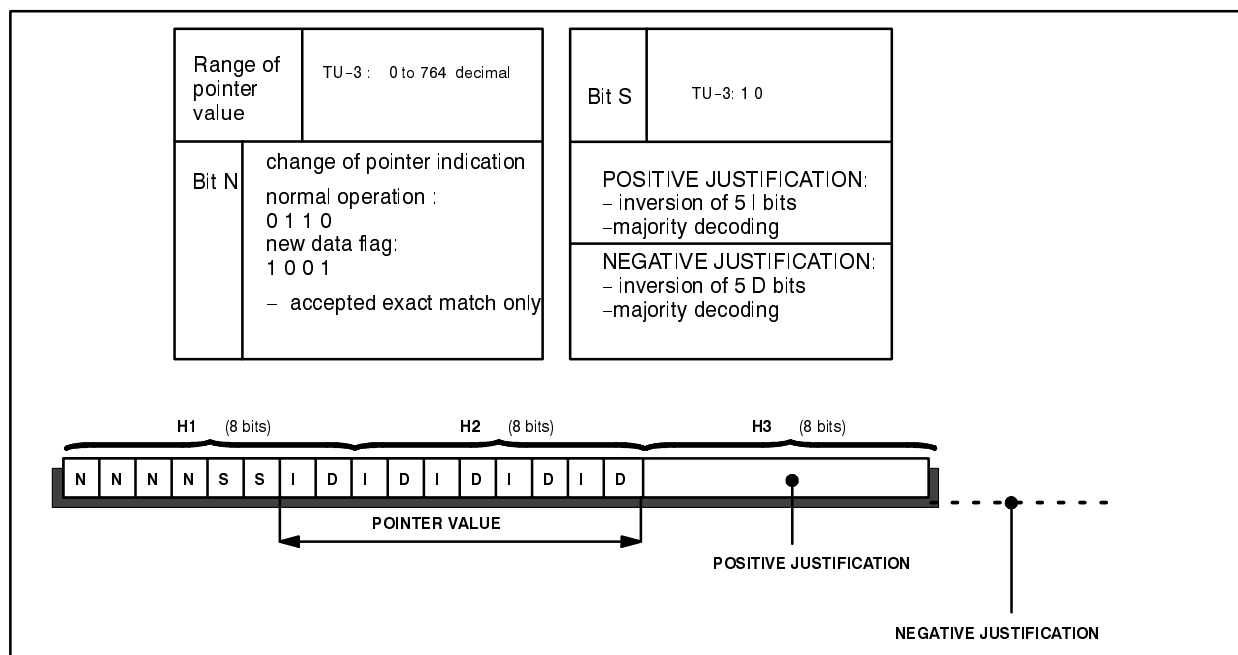


Fig. 5.8-3 TU-3 pointer (H1, H2, H3) coding

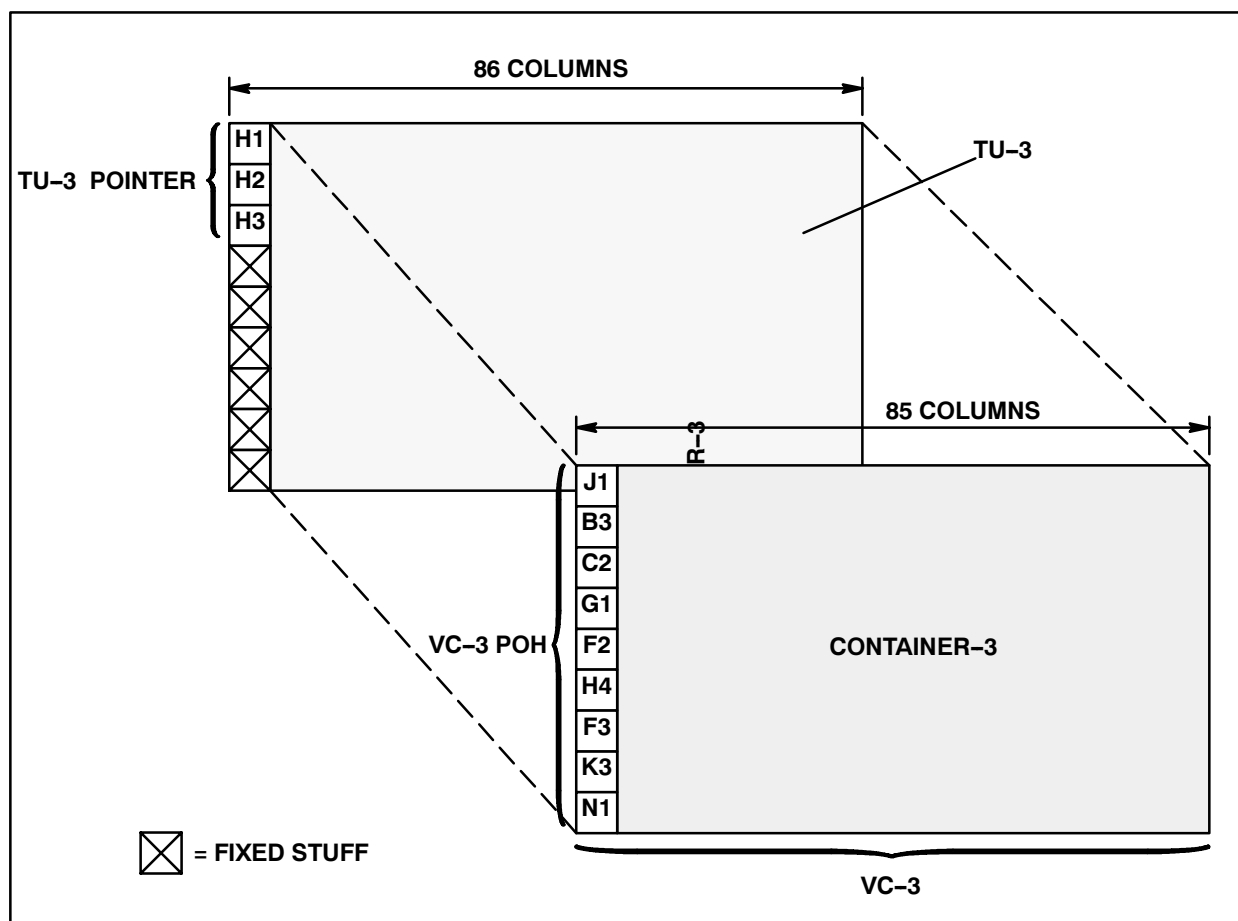


Fig. 5.8-4 TU-3 pointer

### 38Mbit/s outgoing signals

The three TU–3 Tributary Unit data thus obtained are converted in four outgoing 38.88Mbit/s signals in half-bytes (4 bits); such signals are duplicated and transmitted to the unit connector as TX38DATA 1 – 4 A and TX38DATA 1 – 4 B.

The A signals will be used as main while B signals will be used as protection.

## **Receive side**

The 3X34Mbit/s Tributary Unit has 2 38.88Mbit/s data signals received in half-bytes (4 bits) incoming from the path A (main) and path B (protection), an internal diagnostic analysis logic circuit selects between the data signal in service and the one on stand-by.

The data signal in service is then converted to 19.44Mbit/s transmitted in whole bytes. It is demultiplexed at individual TU–3 Tributary Unit level.

The contents of the Tributary Unit pointer are processed to locate the position of the individual VC–3s inside the frame.

The first byte of every VC–3, which contains the virtual container path-information (POH – Path Overhead), is extracted. The information read are processed and sent to the microprocessor interface.

The C–3 containers obtained after the extraction of the POH must then be "de-synchronized" by extracting the padding, justification control and justification opportunity bytes.

A PLL (Phase Locked Loop) is used to stabilize the de-synchronized data clock signal phase shifts, to perform this function, the data is written in a buffer memory using its clock signal and re-read using the signal deriving from the PLL.

The data are then coded from NRZ into HDB3 and duplicated into a negative and positive signal (levels 0 and +5) in order to reduce any disturbance.

The three tributary signals are sent respectively to the blocks 8, 10 and 12, where they are buffered, re-composed on the three levels and sent to the outgoing interfaces.

If the signals incoming to these blocks is lost, the LOTS alarm signal is issued to the block 7 to be processed.

## Common Functions

### DC/DC Converter

The 3x34Mbit/s Tributary Unit is provided with a on-board DC/DC converter (Block 14). This converter accepts an incoming –48V supply voltage and provides +5V and –5.2V supply voltages to all the components on the unit.

### Alarms

Block 13 is able to communicate via a serial line to the centralized controller of the subrack, furthermore it can drive the two leds on the front panel, the red Led indicates internal failure of the unit, the green one is on when the unit is configured and providing service (in case of 1 + 1 unit protection).

### Diagnostic Functions

The 3x34Mbit/s Tributary Unit receives indications from the (LTU) Connection Unit, about its condition (missing, present, malfunctioning, etc.) on Block 15 and processes them on the microprocessor (Block 13).

Another check performed by the 3x34Mbit/s Tributary Unit is the detection of missing TX pulses, on Blocks 8, 10 and 12.

From DC/DC converter (Block 14) the power supply voltages are also issued towards Block 16, which checks an eventual power failure and communicates it to microprocessor (Block 13).



# Technical Characteristics

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## Microprocessor And Memories

*Microprocessor: Motorola 68302*

*Data Memory: 2 x 128kbyte RAM*

*Program Memory: 2 x 128kbyte FLASH*

*Bootstrap Memory: 1 x 128kbyte EPROM*

*Inventory Memory: 1 x 8kbyte EPROM*

*Back-up Memory: 1 x 8kbyte EEPROM*

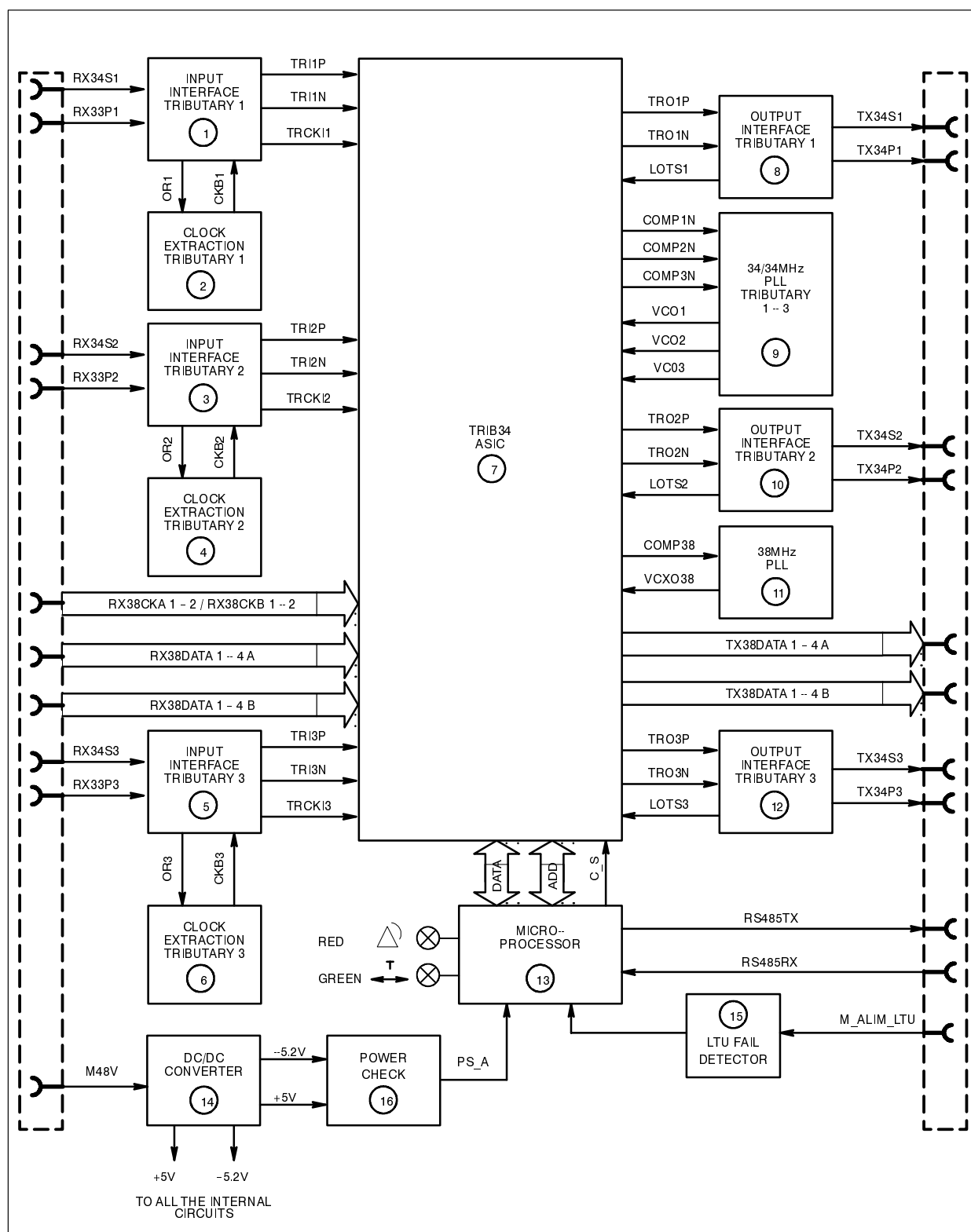


Fig. 5.8-5 3 x 34Mbit/s Tributary Unit – Block Diagram