

Communication Unit 131–8924/01

General Information

The Communication Unit operates as a processor for the SOH and for V11, Q and X.25 interfaces.

The SOH is compliant with ITU–T Recommendations G.70x, G.782, G.783.

————— *For the further details about the SOH management in the ADM–1 refer to chapter "Information for the System Engineer"*

Functions

The Communication Unit supports the following functions:

- ◆ *Reception/Transmission of DCC and data channel bytes from/to SOH buses*
- ◆ *Reception/Transmission of DCC and data channels from/to external interfaces*
- ◆ *Management of V11 interfaces.*
- ◆ *Management of Q interface*
- ◆ *Management of X.25 interface*
- ◆ *Management of a serial interface towards MOST Units*
- ◆ *Unit supervision by means of a microprocessor communicating with the MOST Units.*
- ◆ *Card Power Supply by means of a DC/DC converter, present on the card itself.*
- ◆ *Internal clock generation*

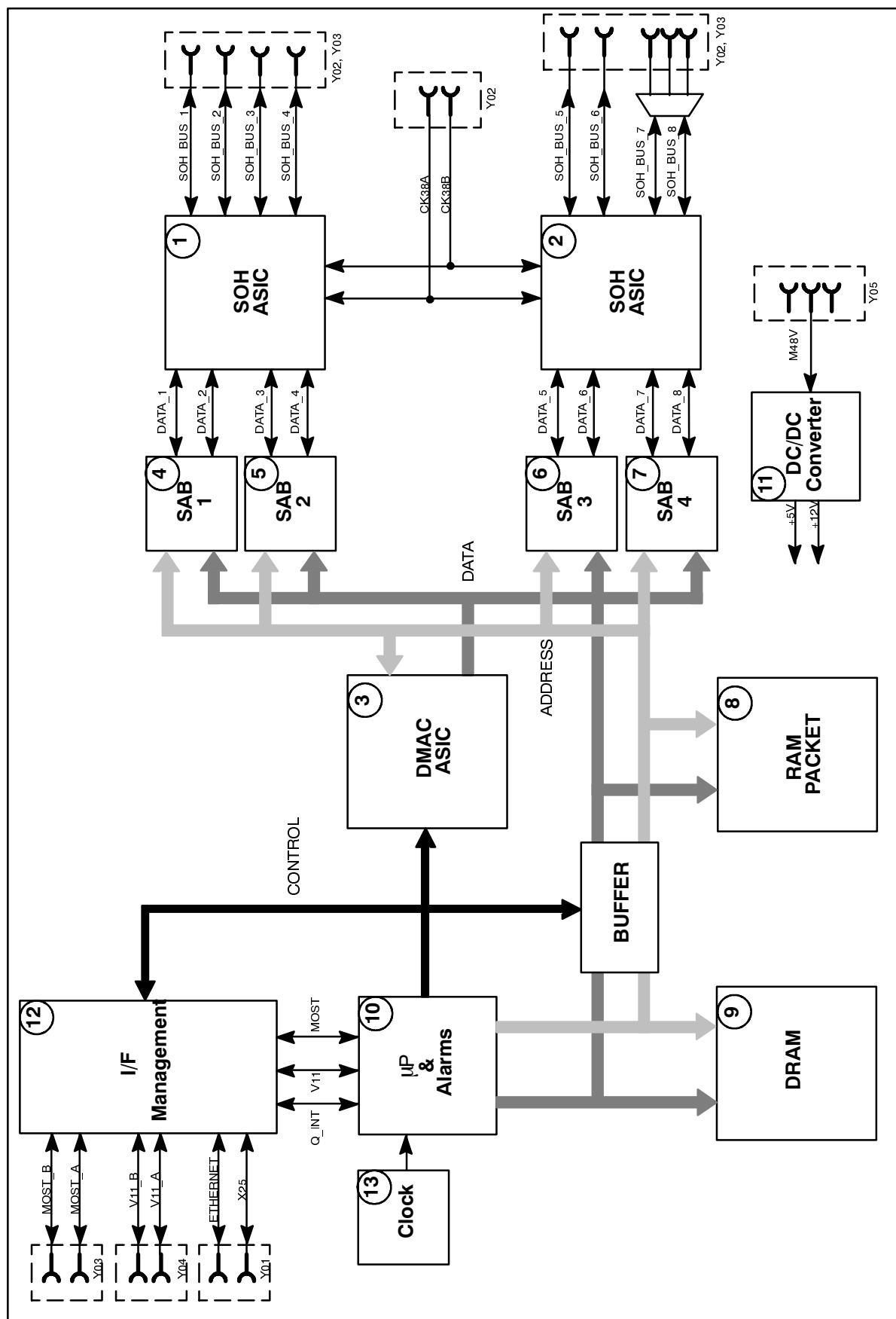


Fig. 5.4–20 Simplified block diagram of Communication Unit

In the following reference will be made to the previous block diagram.

Functional Description

Management of SOH

Reception Functions

The Communication Unit receives the following nine SOH buses:

- ◆ *four SOH buses from the lines*
- ◆ *two SOH buses from the STM–1 tributary modules*
- ◆ *three SOH buses from the STM–1 tributary units (from these three channels only two can be managed together)*

The SOH buses are received by two SOH ASICs (**Blocks 1 and 2**) from a serial line at a 6.48Mbit/s bitrate.

The serial SOH signal is converted into a parallel format (8-bit). Then the SOH ASIC determines which frame timeslots have to be extracted and performs a rejustification of POH timeslots). The extracted data are written into a data channel store.

Each OH channel is associated to an outgoing data channel. Each data channel can be configured as:

- ◆ *DCCm – 576 kbit/s (bytes D4–D12 of SOH)*
- ◆ *DCCr – 192 kbit/s (bytes D1–D3 of SOH)*
- ◆ *64 kbit/s (bytes from SOH)*
- ◆ *64 kbit/s (bytes from POH)*

The relevant bytes previously stored are converted into a serial format and sent in the selected data channel.

The 64kbit/s timing reference is extracted from one of the two 38.88MHz clock references incoming from the MOST Units.

The eighth data channels are managed by four SAB components (**Blocks 4–7**), which convert them into a parallel 8-bit format. These components manages also the data transfer to RAM PACKET memory (**Block 8**), under the supervision of DMAC ASIC (**Block 3**).

The data stored in the RAM PACKET memory (**Block 8**) are periodically extracted by the microprocessor (**Block 10**) which retransmits them towards the relevant interfaces (i.e. D1–D12 bytes towards Q interface and F1–F3 bytes towards V11 interface).

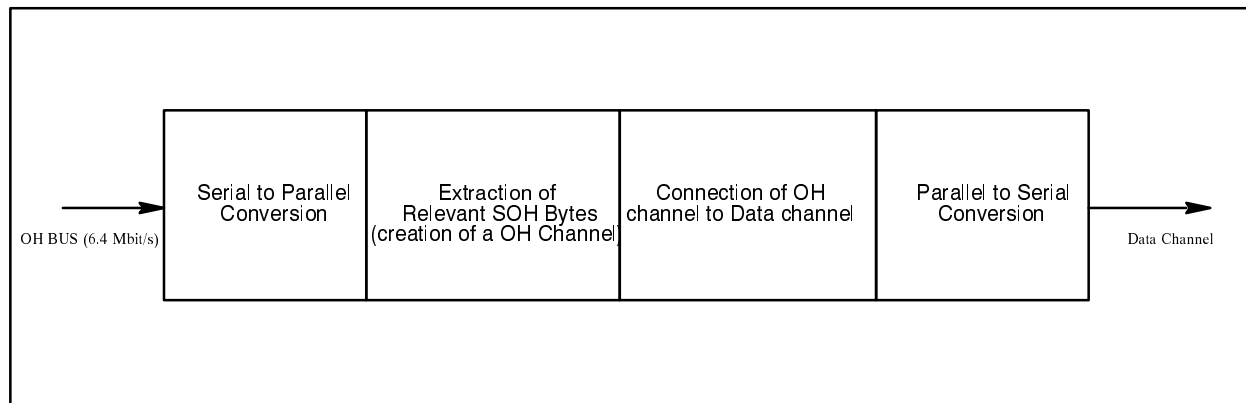


Fig. 5.4–21 Functional block diagram of SOH ASIC: Receive side

Transmission Functions

The data received from V11, Q and serial interfaces are periodically stored, by the microprocessor (**Block 10**), RAM PACKET memory (**Block 8**).

The DMAC ASIC (**Block 3**) transfers the data from the RAM PACKET memory (**Block 8**) towards the SAB components (**Blocks 4–7**). Each of these components manages two data channel.

The SAB converts the data from a parallel 8-bit format to a serial format and sends them to SOH ASICs (**Block 1–2**).

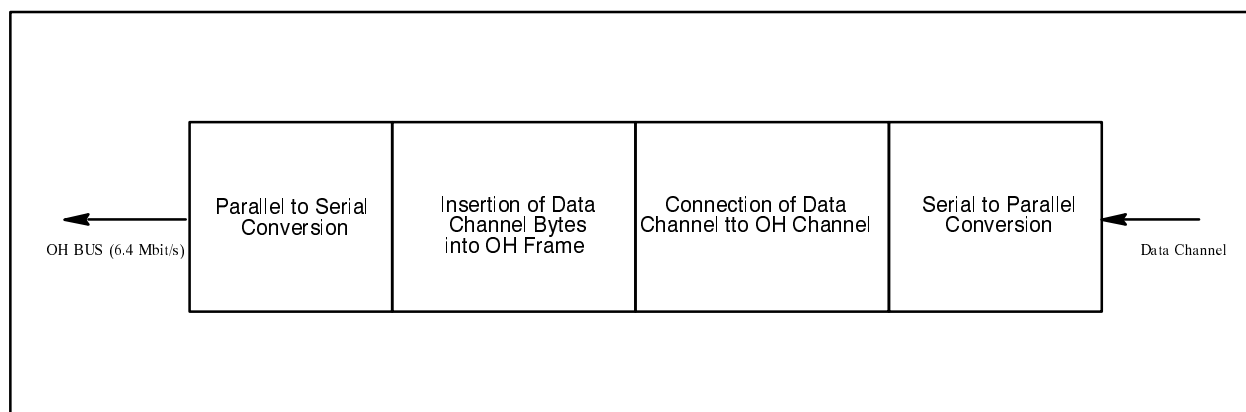


Fig. 5.4–22 Functional block diagram of SOH ASIC: Transmit side

The SOH ASIC connects a data channel to a SOH bus and converts the incoming data from a serial to a parallel format (8-bit). This data stream is written into a transmit store.

Using one of the two 38.88MHz clock references incoming from the MOST Units, is generated a 6.48MHz clock reference.

The transmit store is read at appropriate timeslots by the OH channel, which uses the 6.48MHz clock reference. The bytes from OH channel are inserted in the appropriate timeslots in the OH frame, considering also stuffing due to POH justification.

The OH channel is then converted from a parallel to a serial format and sent, on the relevant SOH bus, towards the different cards.

Interface Management Functions

Serial Interface (MOST)

The Communication Unit manages a serial interface towards MOST Units. A selection of the MOST Unit connected to this serial interface is performed in **Block 12**, under control of microprocessor (which elaborates configuration messages coming from MOST Units).

This serial interface is used to transfer data related to configuration and operation of Communication Unit towards the Local Controller (the Local Controller interface is managed by MOST Units) and to transfer data related to the equipment configuration and operation towards the NMC (the Q interface is managed by the Communication Unit).

Q Interface

The Communication Unit manages a Q interface, in order to allow the MSH11C to act as a Gateway, in a connection with a NMC.

The data related to the equipment operation are transferred/received to/from the MOST Units, by using the serial interface. The microprocessor (**Block 10**) sends these data on Q interface, following the Ethernet protocol.

This interface is also used to redirect the DCC channels, present on SOH, towards the NMC. The microprocessor extracts the data incoming from SOH buses from the packet memory (**Block 8**) and sends them towards the NMC, by using the Q interface.

Common Functions

DC/DC Converter

The Communication Unit is provided with a on-board DC/DC converter. This converter accepts an incoming –48V supply voltage and provides +5V and +12V supply voltages to all the components on the card.

Diagnostic and Service Functions

The microprocessor (**Block 10**) present on Communication Unit performs the supervision of the whole unit. It receives indication about failures or malfunctioning on the different components fitted on the card

There is also a logic circuitry which elaborates messages incoming from the two MOST Units and which manages the selection of connected interfaces (i.e V11_A or V11_B, serial interface towards MOST A or MOST B, etc.).

Internal clock

The Communication Unit is provided with an internal 25MHz clock generator (**Block 13**).

Technical Characteristics

Microprocessor And Memories

<i>Microprocessor:</i>	Motorola 68EN360
<i>Data Memory:</i>	1 x 4Mbyte DRAM
<i>Bootstrap Memory:</i>	1 x 128 Kbyte EPROM
<i>Program Memory:</i>	1 x 512 Kbyte FLASH
<i>Packet Memory:</i>	2 x 128 Kbyte RAM