

# **63x2Mbit/s Tributary Unit 131–8977/01**

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## **General Information**

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The 63x2Mbit/s Tributary Unit operates as a 1.5/2Mbit/s signal tributary and processor (multiplexing/demultiplexing).

The treated signal is compliant with ITU–T Recommendation G.703.

————— *For the further details about the 1.5/2Mbit/s signal characteristics refer to chapter **"Information for the System Engineer"***

# Functions

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The 63x2Mbit/s Tributary Unit supports the following functions:

- ◆ *Reception/Transmission of an electrical 1.5/2Mbit/s signal (HDB3, AMI, B8ZS, NRZ)*
- ◆ *Conversion of incoming 1.5/2Mbit/s signal into NRZ code*
- ◆ *Conversion of outgoing 1.5/2Mbit/s signal from NRZ to tributary line code (HDB3, AMI, B8ZS)*
- ◆ *Mapping of 2Mbit/s signal into TU-12, with insertion of control and justification bits.*
- ◆ *Mapping of TU-12s into a pseudo-STM-1 structure.*
- ◆ *Mapping of four pseudo-STM-1 structures into a STM-1*
- ◆ *Mapping of a STM-1 into four pseudo-STM-1 structures.*
- ◆ *Mapping of a pseudo-STM-1 structure into TU-12s.*
- ◆ *Mapping of TU-12 into 2Mbit/s signal.*
- ◆ *Unit supervision by means of a microprocessor communicating with the MOST Units.*
- ◆ *Card Power Supply by means of a DC/DC converter, present on the card itself.*
- ◆ *Management of interfaces towards the Control Bus and the switches on the MOST Units.*
- ◆ *Internal clock generation.*
- ◆ *Clock reference generation*

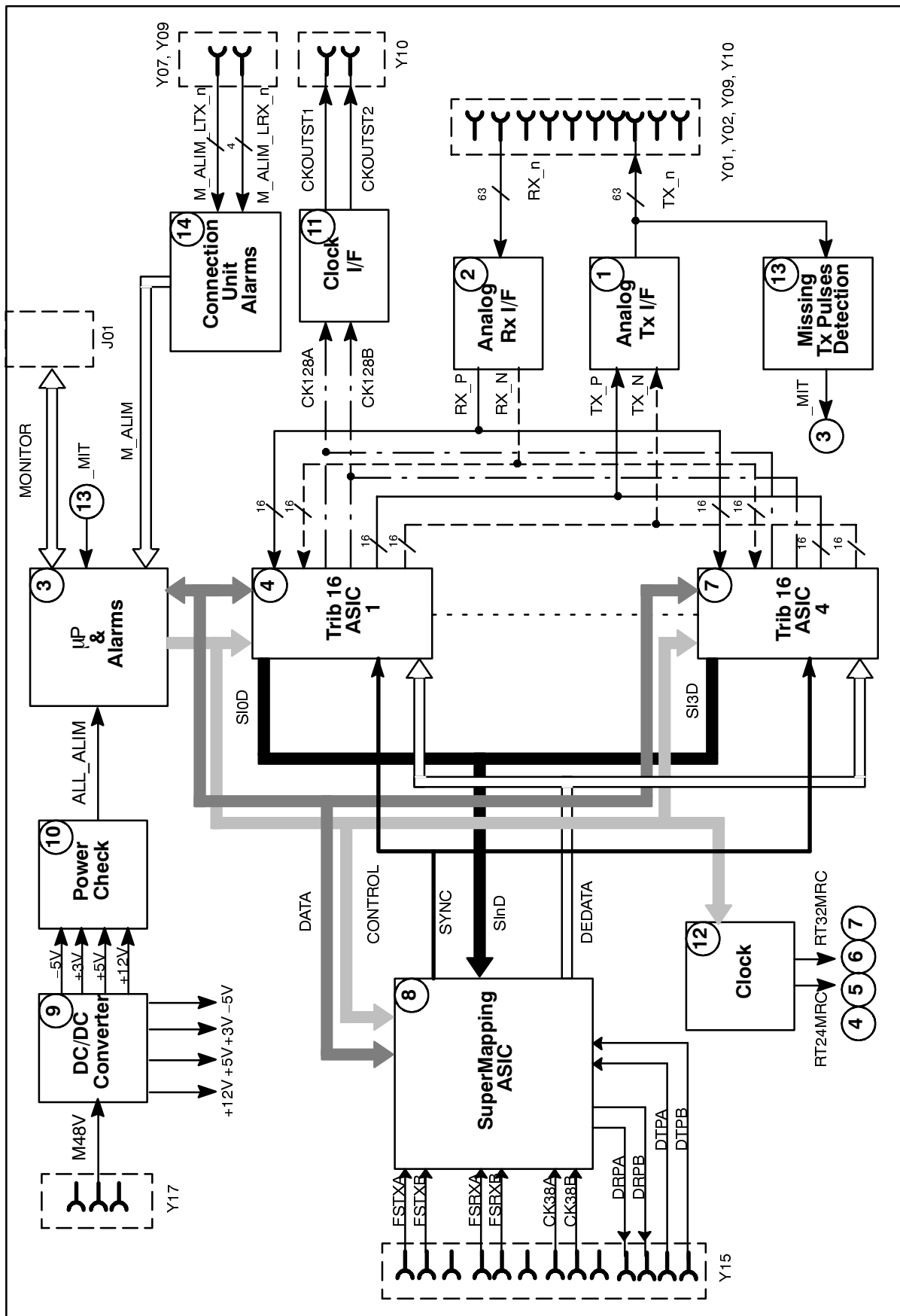


Fig. 5.3–17 Simplified block diagram of 63x2Mbit/s Tributary Unit

In the following reference will be made to the previous block diagram.

# Functional Description

## Reception Functions

The sixty-three incoming PDH signals (RX\_n with n from 1 to 63) are received by the analog RX interface (**Block 2**) which ensures an impedance match and sends the signals RX\_P and RX\_N towards each TRIB16 ASIC (thirty-two).

The analog signals are converted from the line code (HDB3, AMI, B8ZS) into NRZ code. In this step is also checked the presence of incoming AIS or LOS indications.

The NRZ PDH signals are inserted into SDH C12/C11 containers, defined in ITU-T Rec. G.707 (the clock reference is derived by the 19.44MHz issued by SUPERMAPPING ASIC). In this operation justification takes place, in order to recover eventual frequencies offsets (a maximum offset of  $\pm 50$  p.p.m. is allowed).

The sixteen C12/C11s are converted into VC12s, by adding fixed stuff and the following bytes: V5 (POH), N2 (tandem connection monitoring), J2 (path trace identifier) and K4 (user defined).

The VC-12s are inserted in as many TU-12s with an offset defined by the pointer made of V1 and V2 bytes. This offset is introduced in order to minimize the jitter.

The sixteen TU-12s are inserted into a proprietary STM-1 signal. The position of TU-12s inside the proprietary STM-1 is given by a clock (CK4SI) issued by the SUPERMAPPING ASIC towards each TRIB16 ASIC. also the 19.44MHz timing signal (CK19SI) used to generate the parallel proprietary STM-1 is issued by SUPERMAPPING ASIC.

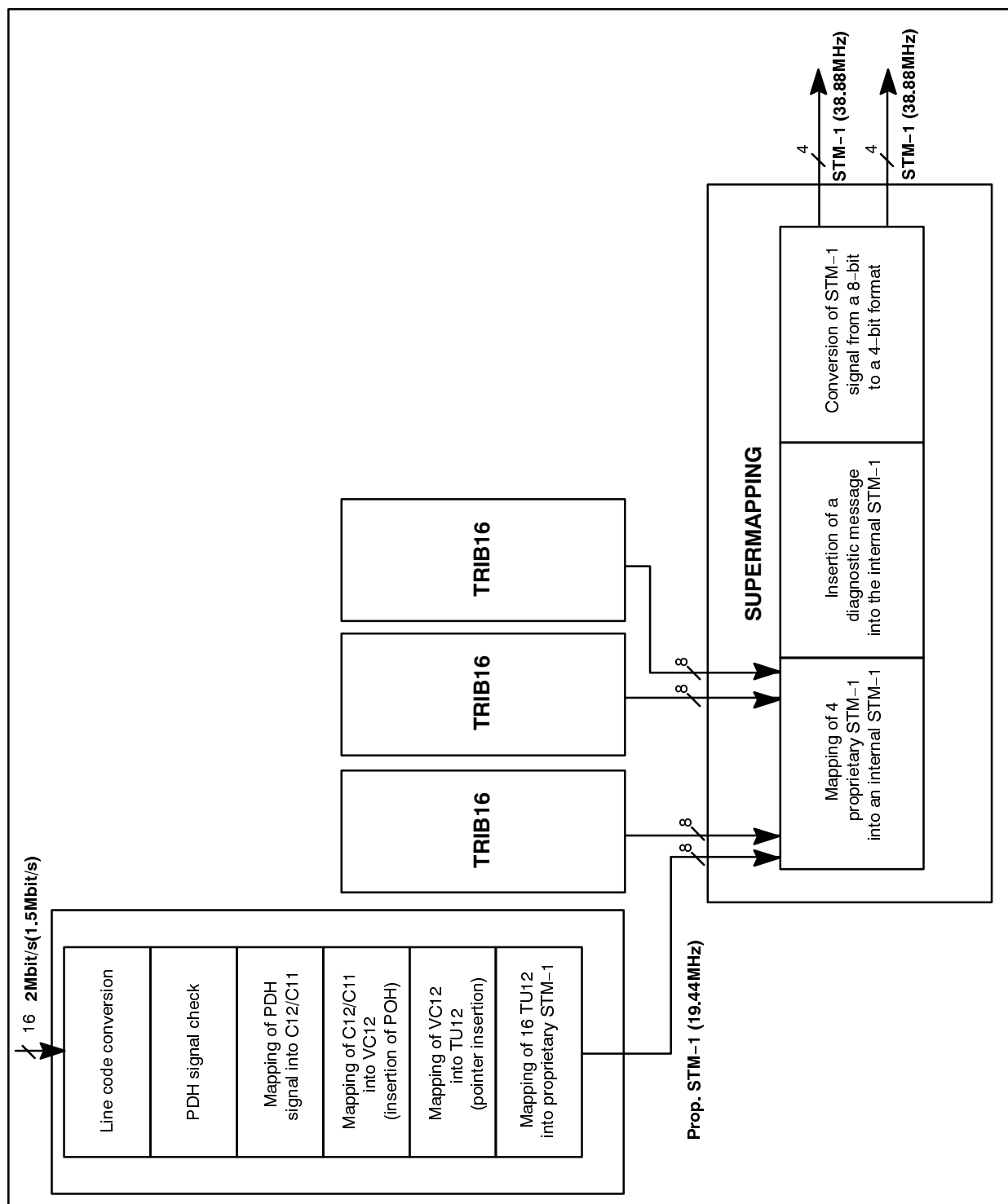
Each TRIB16 ASIC issues an 8-bit proprietary STM-1 (SInD) towards the SUPERMAPPING ASIC. These four proprietary STM-1 are mapped into the payload of a single STM-1 proprietary signal.

The SUPERMAPPING ASIC adds the alignment word and a diagnostic message to the overhead of this STM-1 signal (the diagnostic message includes informations as the equipment number, the channel number, the unit type, etc.).

The STM-1 signal is then converted into a nibble format (at a frequency of 38.88MHz) and sent duplicated towards the two switches, by using the signals DRPA and DRPB.

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*Either blocks 4–5 or blocks 6–7 can be used to protect 32 streams managed by 32x2Mbit/s modules (or cards). For this reason the available 2Mbit/s channels are sixty-four instead of sixty-three.*



**Fig. 5.3-18** Functional block diagram of SUPERMAPPING and TRIB16 ASICs: Receive side

## Transmission Functions

The SUPERMAPPING ASIC (**Block 8**) receives two STM–1 signals from the two switches (DTPA and DTPB) together with two 38.88MHz clock signal (CK38A and CK38B).

On the two STM–1 streams is checked the V4 diagnostic message. This check includes the detection of the alignment word, the parity check and the check of equipment type, equipment number, channel number, etc.

One of the two STM–1 streams is selected in order to be sent towards the four TRIB16 ASICs (**Blocks 4–7**). The selection is made strategy depends on the V4 check, on microprocessor messages and can be forced when the relevant clock signal is missing.

The selected signal is converted into a parallel 8–bit format (at a frequency of 19.44 MHz) and is sent towards every TRIB16 ASIC. To each TRIB16 ASIC are also sent two clock signals: CK4DEn which is used by each TRIB16 ASIC to extract its relevant sixteen TU–12s; CK19DE which is used by the TRIB16s to read the 19.44MHz signal.

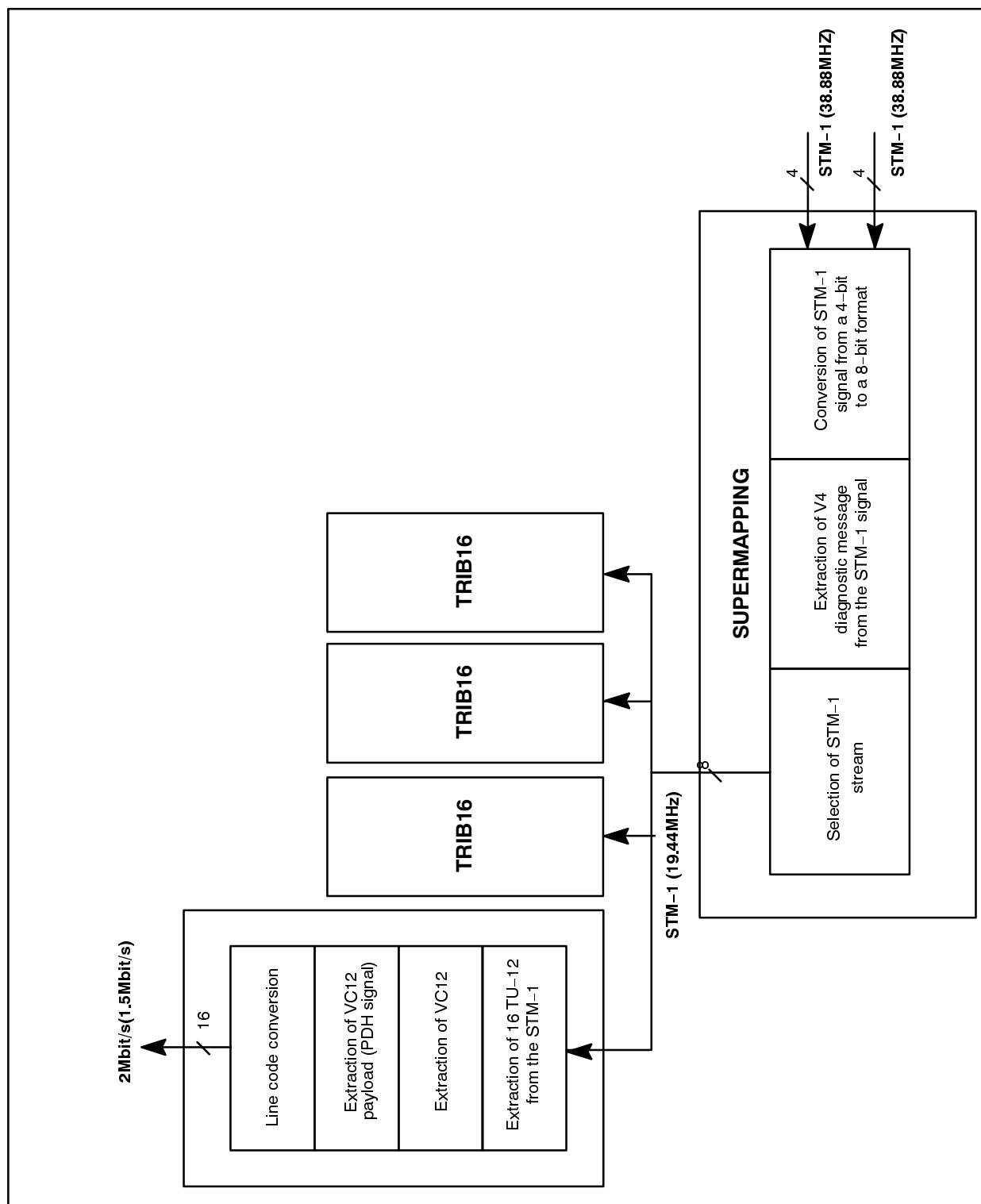
For each TU–12 are extracted the V1 and V2 bytes and is determined the location of each VC12. Once the V5 byte is found all the other bytes of POH are determined (N2, J2 and K4). These bytes are used to check the signal label match, the path trace match, the signal parity, etc.

From each VC12 is extracted the PDH payload which is then converted from NRZ code into the line code (HDB3, AMI, B8ZS).

From each TRIB16 ASIC thirty–two analog signals (TX\_P and TX\_N) are sent towards the analog TX interface (**Block 1**). On **Block 1** an impedance match is performed, then the sixty–three TX\_n signals (with n from 1 to 63) are sent towards the backpanel connector.

The TX\_n signals are used, on **Block 13**, to detect eventual missing Tx pulses. The indication of eventual missing pulses is sent to the microprocessor (**Block 3**).

The 2Mbit/s lines outgoing from this card can be set to high impedance, when the card is used as a protection one (when a switch to the protection has to be performed, the connection units extract the signals from these lines).



**Fig. 5.3-19** Functional block diagram of SUPERMAPPING and TRIB16 ASICs: Transmit side

## Common Functions

### DC/DC Converter

The 63x2Mbit/s Tributary Unit is provided with a on-board DC/DC converter (**Block 9**). This converter accepts an incoming –48V supply voltage and provides +5V, –5V, +3V and +12V supply voltages to all the components on the card.

### Timing Functions

The 63x2Mbit/s Tributary Unit is equipped with a two VCO, working at 49.908MHz and 65.586MHz. These clock references are used by TRIB16 ASICs (**Blocks 4–7**) to read and write the 1.5 and 2Mbit/s signals.

### Reference Clock

The 63x2Mbit/s Tributary Unit issues two 128 kHz clock signals (CK128A and CK128B), towards the two Switches. These signals are generated by each TRIB16 ASIC (**Blocks 4–7**) selecting two extracted 2Mbit/s (1.5Mbit/s) clock references.

### Diagnostic Functions

The 63x2Mbit/s Tributary Unit receives indications from the Connection Units, about their condition (missing, present, malfunctioning, etc.) on **Block 14** and elaborates them on the microprocessor (**Block 3**).

Another check performed by the 63x2Mbit/s Tributary Unit is the detection of missing TX pulses, on **Block 13**.

From DC/DC converter (**Block 9**) the power supply voltages are also issued towards **Block 10**, which checks an eventual power failure and communicates it to microprocessor (**Block 3**).



# Technical Characteristics

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## Microprocessor And Memories

*Microprocessor: Motorola 68302*

*Data Memory: 2 x 128 Kbyte RAM*

*Program Memory: 2 x 512 Kbyte FLASH*

*Bootstrap Memory: 1 x 128 Kbyte EPROM*

*Inventory Memory: 1 x 8 Kbit EPROM*

*Back-up Memory: 1 x 8 Kbyte EEPROM*

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