

MOST Unit 131-9141/xx

Introduction

The possible MOST configurations are based on the following sub-units:

Description	Reference	Q.ty
MOST Common Parts Sub-unit Type 2	130-3492/01	1
MOST Common Parts Sub-unit Type 2s	130-3492/03	1
STM-1 Electrical Line Sub-Unit	130-3558/01	1/2
S-1.1 Optical Sub-unit with SC Connectors	130-3493/01	1/2
S-1.1 Optical Sub-unit with FC Connectors	130-3493/02	1/2
L-1.1 Optical Sub-unit with SC Connectors	130-3494/01	1/2
L-1.1 Optical Sub-unit with FC Connectors	130-3494/02	1/2
L-1.2/L-1.3 Optical Sub-unit with SC Connectors	130-3495/01	1/2
L-1.2/L-1.3 Optical Sub-unit with FC Connectors	130-3495/02	1/2
16x1.5/2Mbit/s Tributary Sub-unit	130-3496/06	0/1
32x1.5/2Mbit/s Tributary Sub-unit	130-3496/05	0/1
8x2Mbit/s + 1x34Mbit/s Tributary Sub-Unit (*)	130-3545/02	0/1
1x34Mbit/s G.703 Tributary Sub-unit	130-3545/01	0/1

NOTE (*) This sub-unit is the only tributary available for ADM-1

General

The following block diagram gives a simplified explanation of the MOST Unit functions.

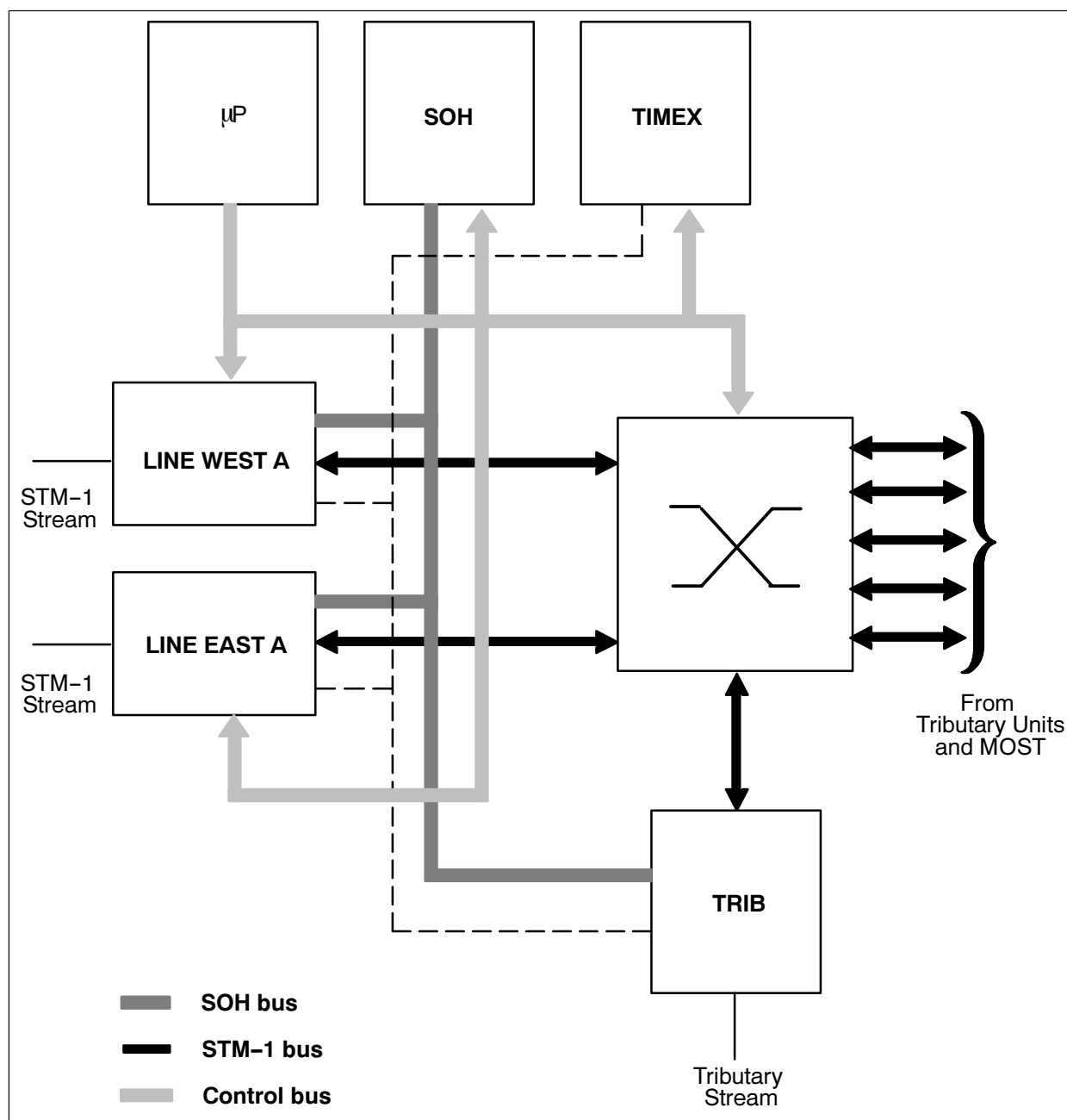


Fig. 5.2-1 Simplified block diagram of MOST Unit

A MOST Unit ensures the following functions:

- ◆ reception / Transmission of two STM-1 electrical / optical streams;
- ◆ optional management of a Tributary Module;
- ◆ management of cross connections;
- ◆ management of all card alarms;;

- ◆ *extraction of a timing reference;*
- ◆ *management of F interface;*
- ◆ *partial management of SOH;*
- ◆ *MSP protection management;*
- ◆ *card protection management;*
- ◆ *SNCP protection management.*

On the MOST Unit are fitted two STM-1 Modules (electrical or optical). The signal incoming on these lines is converted into a NRZ code and, after the extraction of POH and SOH, is sent towards the switch, as a 38.88MHz nibble signal.

The switch, also fitted on the MOST Unit, is able to cross connect up to eight STM-1 equivalent streams (represented by 38.88MHz nibble signals).

The microprocessor on the MOST Unit, in addition to the supervision of the card itself, collects the alarms incoming from all the other units. When two MOST Units are fitted, only one acts as master (the two MOST communicate by means of the X-MOST bus). As soon as a failure on the master MOST Unit is detected, the other one switches from a stand-by condition to a fully operational state.

The microprocessor allows also the management of a F interface, which is used to connect the MSH11C to a LC.

The Timex component, fitted on the MOST Unit, can extract a timing reference, by selecting one of the following sources (each source is represented by a 128KHz signal):

- ◆ *Four STM-1 line signals (represented by 128KHz signals)*
- ◆ *Seven Tributary ports (one on Tributary 1, Tributary 2 and MOST Tributary Modules, two on Tributary 3 and one selected among Tributary 1, Tributary 2 and MOST Tributary Modules) (represented by 128KHz signals)*
- ◆ *Two external sources (2048Kbit/s or 2048KHz)*

On the MOST Unit is included a SOH ASIC, which allows the partial management of SOH and POH. This function is used to support a maximum of four DCC channels, when a Communication Unit is not available.

The MSP protection (line 1+1 protection) is managed by MOST Unit by handling K1 and K2 bytes of SOH.

The MOST Unit allows also the management of tributary unit protection and of SNC protection.

STM-1 Optical Line Sub-Unit (130-3493/** and 130-3494/**)

General Information

The STM-1 Optical Line Sub-Unit operates as an Optical line interface for the 155.520Mbit/s STM-1 first level synchronous transport module.

The treated signal is compliant with ITU-T Recommendation G.957.

————— *For the further details about the STM-1 signal characteristics refer to chapter "Information for the System Engineer"*

Functions

The STM-1 Optical Line Sub-Unit supports the following functions:

- ◆ *reception/Transmission of an optical 155Mbit/s signal;*
- ◆ *conversion of incoming 155Mbit/s optical signal into an electrical NRZ signal;*
- ◆ *conversion of outgoing 155Mbit/s electrical NRZ signal into an optical signal;*
- ◆ *conversion of a serial 155.520MHz signal into a parallel 38.88MHz signal (on 4-bits);*
- ◆ *conversion of a parallel 38.88MHz signal (on 4-bits) into a serial 155.520MHz signal;*
- ◆ *internal clock generation;;*
- ◆ *detection of missing pulses in reception;*
- ◆ *check of incoming signal power;*
- ◆ *internal regulation of laser emitted power.*

Functional Description

In this paragraph reference will be made to the following block diagram.

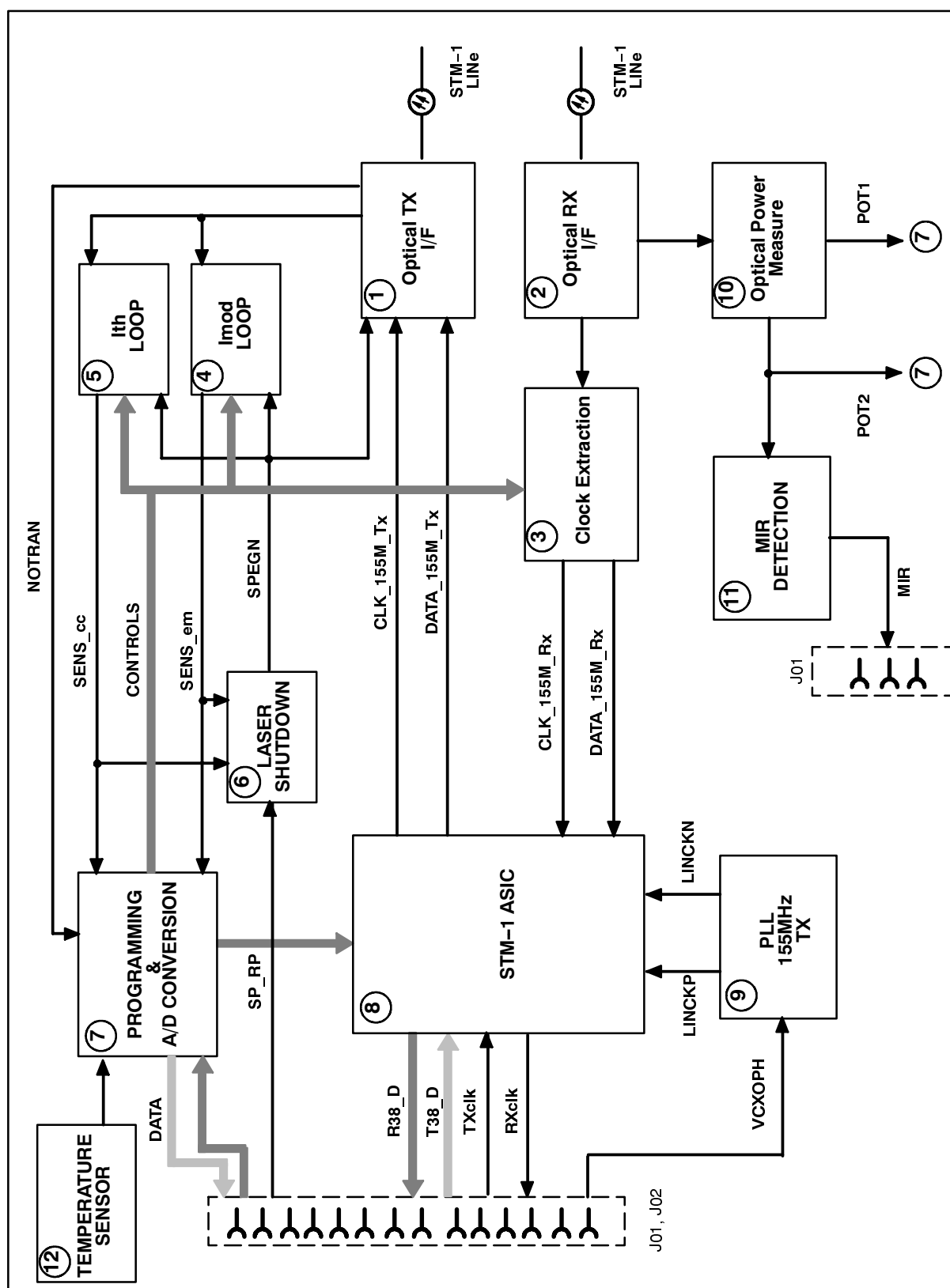


Fig. 5.2-2 *STM-1 Optical Line Sub-Unit Block Diagram*

Reception Functions

The optical STM-1 line signal is converted into an electrical NRZ signal, by an integrated PIN-FET component (including a photo diode and an amplifier) (**Block 2**).

From **Block 2** the NRZ signal is sent towards **Block 3**, which provides the clock recovery. The received NRZ signal is also used to measure the received optical power (**Block 10**).

The measured value of the optical power is converted into a digital format (**Block 7**) and then is sent towards the microprocessor. The value **POT2** is also used by **Block 11** in order to detect any eventual missing received pulse. This condition is communicated to the microprocessor, issuing the signal **MIR**.

The STM-1 NRZ signal is sent to the STM-1 ASIC (**Block 8**) by means of signal **DATA_155M_Rx**, together with the clock indication, **CLK_155M_Rx**.

The STM-1 ASIC converts the NRZ signal from a serial to a parallel format, sending a 38.88Mbit/s data signal (**R38_D**), in a four bits format, and a 38.88MHz clock signal (**RXclk**) towards the board connectors (J01 and J02). These signals are received and elaborated by the MUX-1 ASIC on the Common Parts Sub-Unit.

Transmission Functions

The STM-1 ASIC (**Block 8**) receives a four bits signal, at a bitrate of 38.88Mbit/s, (**TX38_D**) from the board connectors (J01 and J02). These signals are read using the clock signal issued on **TXclk**.

Block 9 includes a 19.44MHz VCO, controlled by the signal **VCXOPH**, and generates a 155.52MHz clock signal, used by STM-1 ASIC to transfer data towards the Optical TX Interface (**Block 1**).

STM-1 ASIC converts the data from a parallel to a serial format and sends them towards **Block 1** on the line **DATA_155M_Tx**, together with the clock signal **CLK_155M_Tx**.

Block 1 includes all the circuitry necessary to convert the electrical NRZ signal into an optical one. The electrical/optical transducer is a II window laser.

The power emitted by the laser must be tuned in order to maintain constant its mean value. For this purpose the BIAS current and the modulating current are tuned by two control loops (**Blocks 4 and 5**).

Block 5 ensures an optical signal with a constant mean value. **Block 4** acts to limitate possible peak of BIAS current outside the acceptable range.

The global effect of the joined action of **Block 4** and **5** is an emitted optical signal with constant mean value and without peaks outside the range acceptable for the receiver.

Supervision Functions

In **Block 7** is implemented the Analog/Digital conversion of the following measured values:

- ◆ *Ith: threshold current of the laser (from **Block 5**);*
- ◆ *Imod: modulating current of the laser (from **Block 4**);*
- ◆ *Ipot: current proportional to the emitted average power (from **Block 1**);*
- ◆ *POT1-POT2: measured received power (from **Block 10**);*
- ◆ *NOTRAN: indication of missing transmitted pulses;*
- ◆ *Temperature.*

All these values are converted into a digital format and transmitted to the microprocessor on the Common Parts Sub-Unit, which elaborates them in order to detect eventual malfunctioning or faults.

Block 7 ensures also the tuning of the sub-unit, under the control of the microprocessor.

Block 6 can force the laser shutdown, either when the BIAS current reaches a value not acceptable for the component or when the microprocessor sends a message to disable the laser transmitter. This laser shutdown allows to implement the optical protection.

Timing Functions

The STM-1 Optical Line Sub-Unit is provided with a 19.44MHz VCO and a 155.52MHz VCO.

STM-1 El. Line Sub-unit (130-3558/01)

General Information

The STM-1 Electrical Line Sub-Unit operates as an Electrical (CMI code) line interface for the 155.520Mbit/s STM-1 first level synchronous transport module.

The treated signal is compliant with ITU-T Recommendation G.703.

For the further details about the STM-1 signal characteristics refer to chapter "Information for the System Engineer"

Functions

The STM-1 Electrical Line Sub-Unit supports the following functions:

- ◆ *reception/Transmission of an electrical 155Mbit/s CMI signal;*
- ◆ *conversion of incoming 155Mbit/s signal from CMI to NRZ code;*
- ◆ *conversion of outgoing 155Mbit/s signal from NRZ to CMI code;*
- ◆ *conversion of a serial 155.520MHz signal into a parallel 38.88MHz signal (on 4-bits);*
- ◆ *conversion of a parallel 38.88MHz signal (on 4-bits) into a serial 155.520MHz signal;*
- ◆ *internal clock generation.*

Functional Description

In this paragraph reference will be made to the following block diagram.

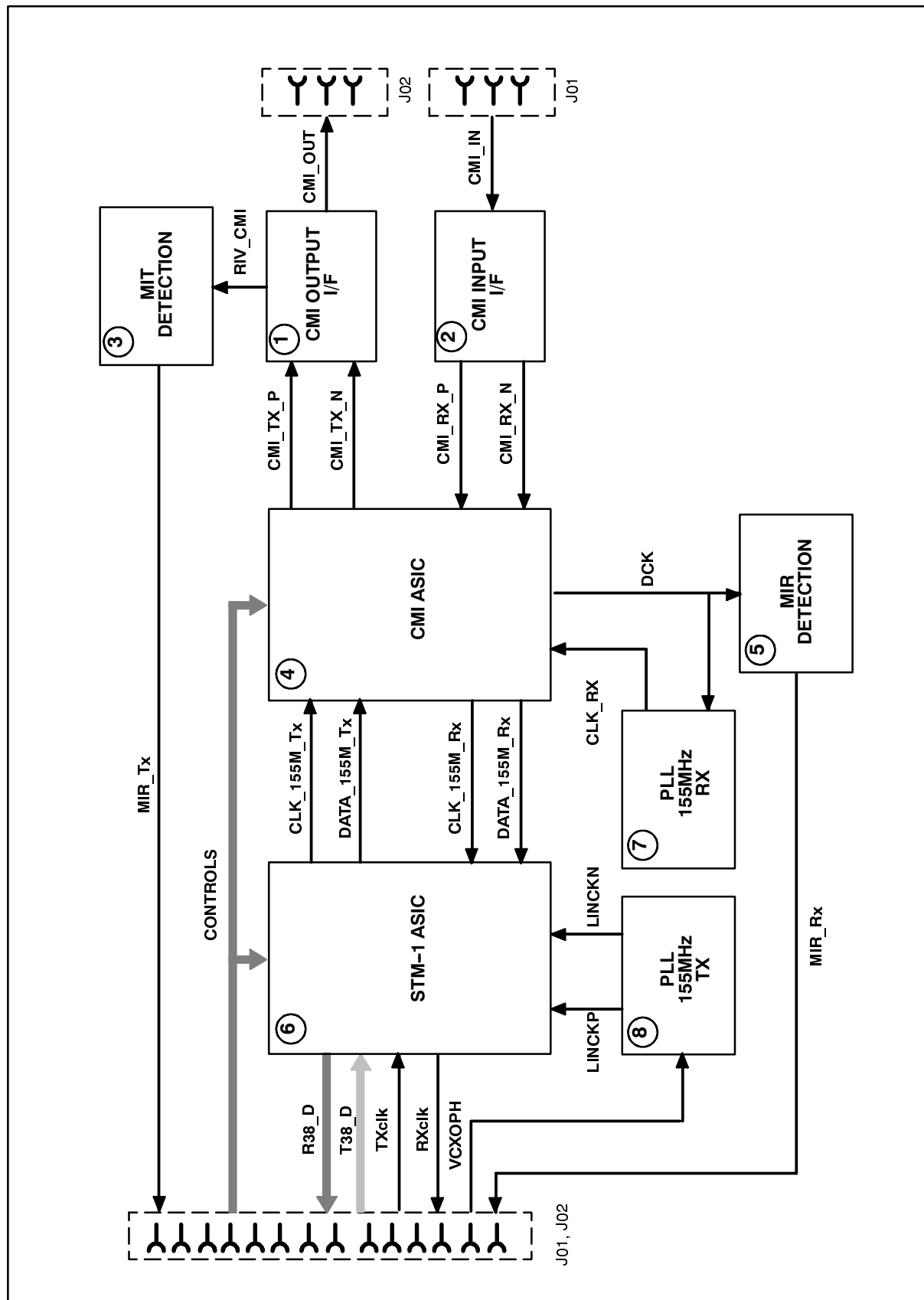


Fig. 5.2-3 Simplified block diagram of STM-1 el. Line Sub-Unit

Reception Functions

The incoming STM-1 CMI signal is received on CMI INPUT Interface (**Block 2**), which ensures an impedance matching. The signal is sent towards CMI ASIC (**Block 4**) by means of signals **CMI_RX_P** and **CMI_RX_N**.

The CMI ASIC the CMI signal is converted into NRZ code and it is sent towards STM-1 ASIC (**Block 6**), by means of signal **DATA_155M_Rx**.

In addition, the CMI ASIC sends the signal **DCK** towards **Block 5**, which reveals any eventual absence of received pulses and towards **Block 7**, which extracts a 155MHz clock signal from the received CMI stream.

The information about extracted clock are sent towards STM-1 ASIC by means of signal **CLK_155M_Rx**.

The STM-1 ASIC converts the NRZ signal from a serial to a parallel format, sending a 38.88Mbit/s data signal (**R38_D**), in a four bits format, and a 38.88MHz clock signal (**RXclk**) towards the board connectors (J01 and J02). These signals are received and elaborated by the MUX-1 ASIC on the Common Parts Sub-Unit.

Transmission Functions

The STM-1 ASIC (**Block 6**) receives a four bits signal, at a bitrate of 38.88Mbit/s, (**TX38_D**) from the board connectors (J01 and J02). These signals are read using the clock signal issued on **TXclk**.

Block 8 includes a 19.44MHz VCO, controlled by the signal **VCXOPH**, and generates a 155.52MHz clock signal, used by STM-1 ASIC to transfer data towards CMI ASIC (**Block 4**).

STM-1 ASIC converts the data from a parallel to a serial format and sends them towards CMI ASIC on the line **DATA_155M_Tx**, together with the clock signal **CLK_155M_Tx**.

The CMI ASIC converts the STM-1 signal from NRZ to CMI code and sends it towards the CMI OUTPUT Interface (**Block 1**), by means of signals **CMI_TX_P** and **CMI_TX_N**.

Block 1 ensures an impedance matching, before transmitting **CMI_OUT** signal and enables the check performed by **Block 3**, in order to detect eventual missing transmitted pulses.

Supervision Functions

The functions of CMI and STM-1 ASICs (**Blocks 4 and 6**) are controlled by the microprocessor on the master MOST Unit.

Timing Functions

The STM-1 Electrical Line Sub-Unit is provided with a 19.44MHz VCO and a 155.52MHz VCO.

32x1.5/2Mbit/s Tributary Sub-unit (130-3496/05)

General Information

The 32x2Mbit/s Tributary Sub-Unit operates as a 1.5/2Mbit/s signal tributary and processor (multiplexing/demultiplexing).

The treated signal is compliant with ITU-T Recommendation G.703.

————— For the further details about the 1.5/2Mbit/s signal characteristics refer to chapter *”Information for the System Engineer”*

Functions

The 32x2Mbit/s Tributary Sub-Unit supports the following functions:

- ◆ *reception/Transmission of an electrical 1.5/2Mbit/s signal (HDB3, AMI, B8ZS, NRZ);*
- ◆ *conversion of incoming 1.5/2Mbit/s signal into NRZ code;*
- ◆ *conversion of outgoing 1.5/2Mbit/s signal from NRZ to tributary line code (HDB3, AMI, B8ZS);*
- ◆ *mapping of 2Mbit/s signal into TU-12, with insertion of control and justification bits;*
- ◆ *mapping of TU-12s into a pseudo-STM-1 structure;*
- ◆ *mapping of two pseudo-STM-1 structures into a STM-1;*
- ◆ *mapping of a STM-1 into two pseudo-STM-1 structures;*
- ◆ *mapping of a pseudo-STM-1 structure into TU-12s;*
- ◆ *mapping of TU-12 into 2Mbit/s signal;*
- ◆ *internal clock generation;*
- ◆ *clock reference generation.*

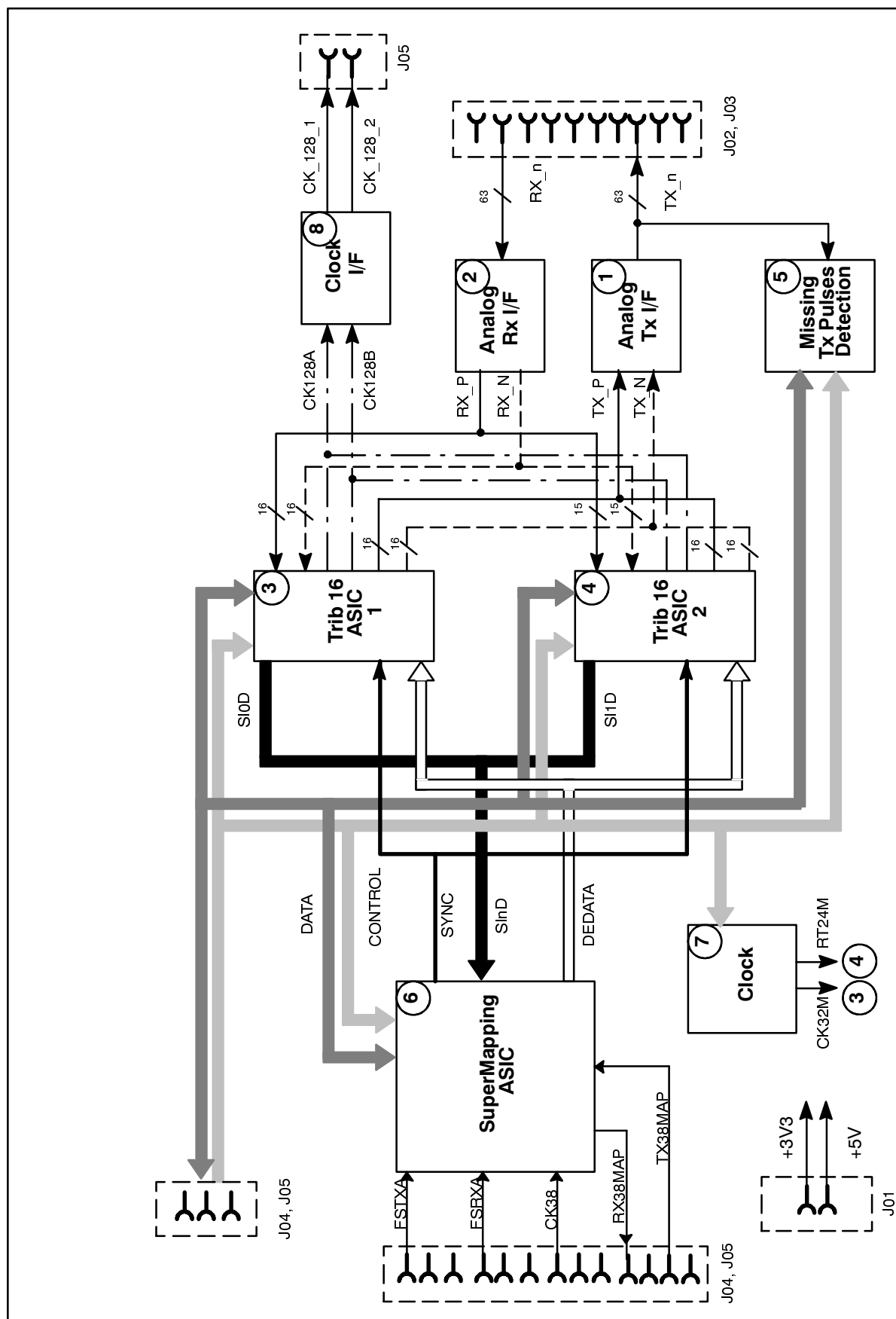


Fig. 5.2-4 Simplified block diagram of 32x2Mbit/s Tributary Sub-Unit

In the following reference will be made to the previous block diagram.

Functional Description

Reception Functions

The thirty-two incoming PDH signals (RX_n with n from 1 to 32) are received by the analog RX interface (**Block 2**) which ensures an impedance match and sends the signals RX_P and RX_N towards each TRIB16 ASIC (thirty-two towards **Blocks 1-2**).

The analog signals are converted from the line code (HDB3, AMI, B8ZS) into NRZ code. In this step is also checked the presence of incoming AIS or LOS indications.

The NRZ PDH signals are inserted into SDH C12/C11 containers, defined in ITU-T Rec. G.707 (the clock reference is derived by the 19.44MHz clock issued by SUPERMAPPING ASIC). In this operation justification takes place, in order to recover any eventual frequency offset (a maximum offset of ± 50 p.p.m. is allowed).

The sixteen C12/C11s are converted into VC12s, by adding fixed stuff and the following bytes: V5 (POH), N2 (tandem connection monitoring), J2 (path trace identifier) and K4 (user defined).

The VC-12s are inserted in TU-12s with an offset defined by the pointer made of V1 and V2 bytes. This offset is introduced in order to minimize the jitter.

The sixteen TU-12s are inserted into a proprietary STM-1 signal. The position of TU-12s inside the proprietary STM-1 is given by a clock (CK4SI) issued by the SUPERMAPPING ASIC towards each TRIB16 ASIC. Also the 19.44MHz timing signal (CK19SI) used to generate the parallel proprietary STM-1 is issued by SUPERMAPPING ASIC.

Each TRIB16 ASIC issues an 8-bit proprietary STM-1 (SInD) towards the SUPERMAPPING ASIC. These two proprietary STM-1 are mapped in the payload of a single STM-1 signal.

The SUPERMAPPING ASIC adds the alignment word and a diagnostic message to the overhead of this STM-1 signal (the diagnostic message includes informations as the equipment number, the channel number, the unit type, etc.).

The STM-1 signal is then converted into a nibble format (at a frequency of 38.88MHz) and sent towards the switch, by using the signals RX38MAP.

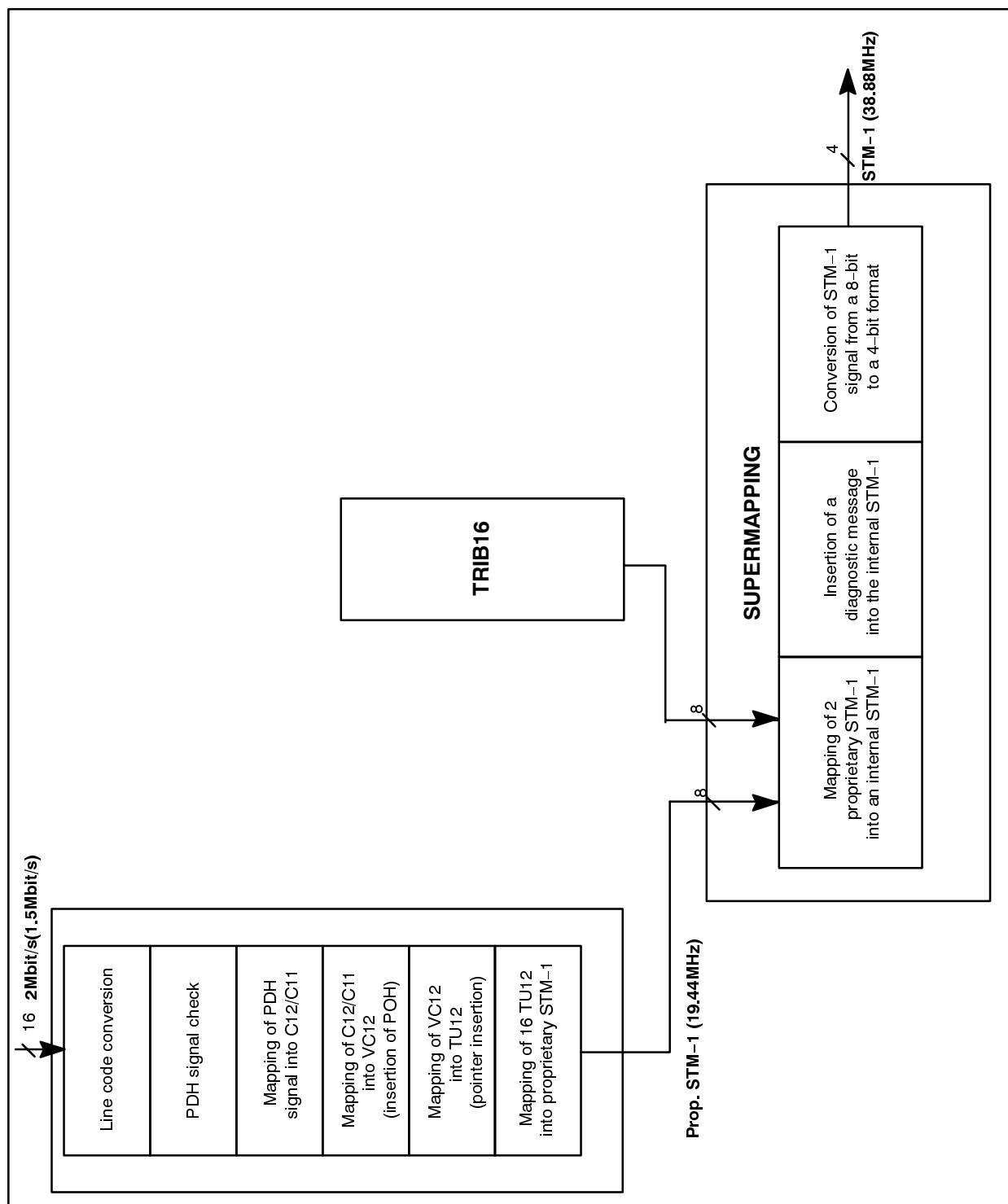


Fig. 5.2-5 Functional block diagram of SUPERMAPPING and TRIB16 ASICs: Receive side

Transmission Functions

The SUPERMAPPING ASIC (**Block 8**) receives a STM-1 signal from the switch (TX38MAP) together with a 38.88MHz clock signal (CK38).

On the STM-1 stream is checked the V4 diagnostic message. This check includes the detection of the alignment word, the parity check and the check of equipment type, equipment number, channel number, etc.

The STM-1 signal is converted into a parallel 8-bit format (at a frequency of 19.44 MHz) and is sent towards every TRIB16 ASIC. To each TRIB16 ASIC are also sent two clock signals: CK4D_{En} which is used by each TRIB16 ASIC to extract its relevant sixteen TU-12s; CK19DE which is used by the TRIB16s to read the 19.44MHz signal.

For each TU-12 are extracted the V1 and V2 bytes and is determined the location of each VC12. Once the V5 byte is found all the other bytes of POH are determined (N2, J2 and K4). These bytes are used to check the signal label match, the path trace match, the signal parity, etc.

From each VC12 is extracted the PDH payload which is then converted from NRZ code into the line code (HDB3, AMI, B8ZS).

From each TRIB16 ASIC thirty-two analog signals (TX_P and TX_N) are sent towards the analog TX interface (**Block 1**). On **Block 1** an impedance match is performed, then the sixty-three TX_n signals (with n from 1 to 32) are sent towards the backpanel connector.

The TX_n signals are used, on **Block 5**, to detect any eventual missing Tx pulse. The indication of eventual missing pulses is stored on a register and can be recovered by the microprocessor of master MOST Unit.

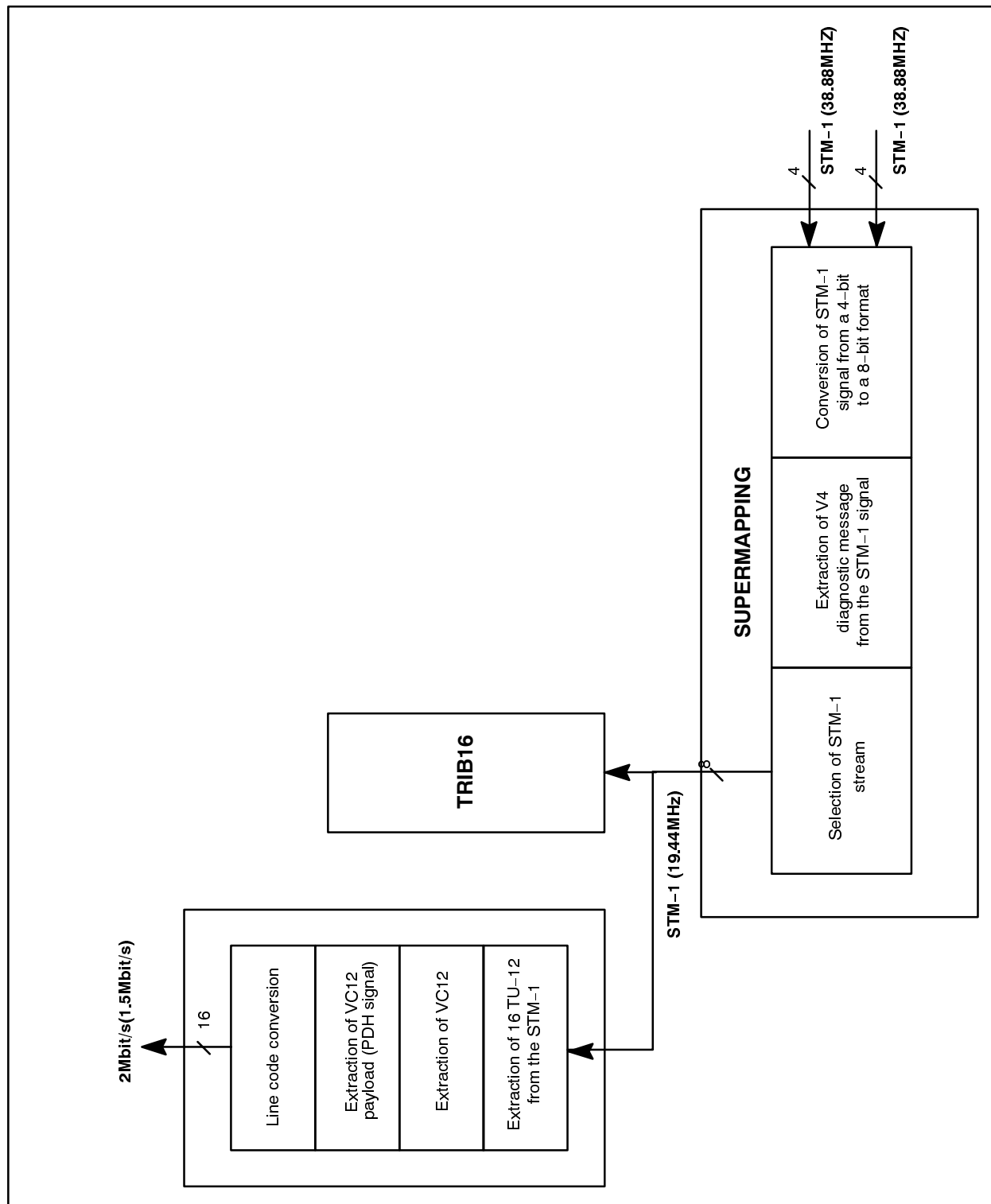


Fig. 5.2-6 Functional block diagram of SUPERMAPPING and TRIB16 ASICs: Transmit side

Common Functions

Timing Functions

The 32x2Mbit/s Tributary Unit is equipped with a VCO, working at 65.586MHz. This clock reference is used by TRIB16 ASICs (**Blocks 1-2**) to read and write the 2Mbit/s signals.

Reference Clock

The 32x2Mbit/s Tributary Unit issues two 128 kHz clock signals (CK_128_1 and CK_128_2), towards the two Switches. These signals are generated by each TRIB16 ASIC (**Blocks 1-2**) selecting two extracted 2Mbit/s (1.5Mbit/s) clock references.

16x1.5/2Mbit/s Tributary Sub-unit (130–3496/06)

General Information

The 16x2Mbit/s Tributary Sub-Unit operates as a 1.5/2Mbit/s signal tributary and processor (multiplexing/demultiplexing).

The treated signal is compliant with ITU-T Recommendation G.703.

For the further details about the 1.5/2Mbit/s signal characteristics refer to chapter "Information for the System Engineer"

Functions

The 16x2Mbit/s Tributary Sub-Unit supports the following functions:

- ◆ *reception/Transmission of an electrical 1.5/2Mbit/s signal (HDB3, AMI, B8ZS, NRZ);*
- ◆ *conversion of incoming 1.5/2Mbit/s signal into NRZ code;*
- ◆ *conversion of outgoing 1.5/2Mbit/s signal from NRZ to tributary line code (HDB3, AMI, B8ZS);*
- ◆ *mapping of 2Mbit/s signal into TU-12, with insertion of control and justification bits;*
- ◆ *mapping of TU-12s into a pseudo-STM-1 structure;*
- ◆ *mapping of a pseudo-STM-1 structure into TU-12s;*
- ◆ *mapping of TU-12 into 2Mbit/s signal;*
- ◆ *internal clock generation;*
- ◆ *clock reference generation.*

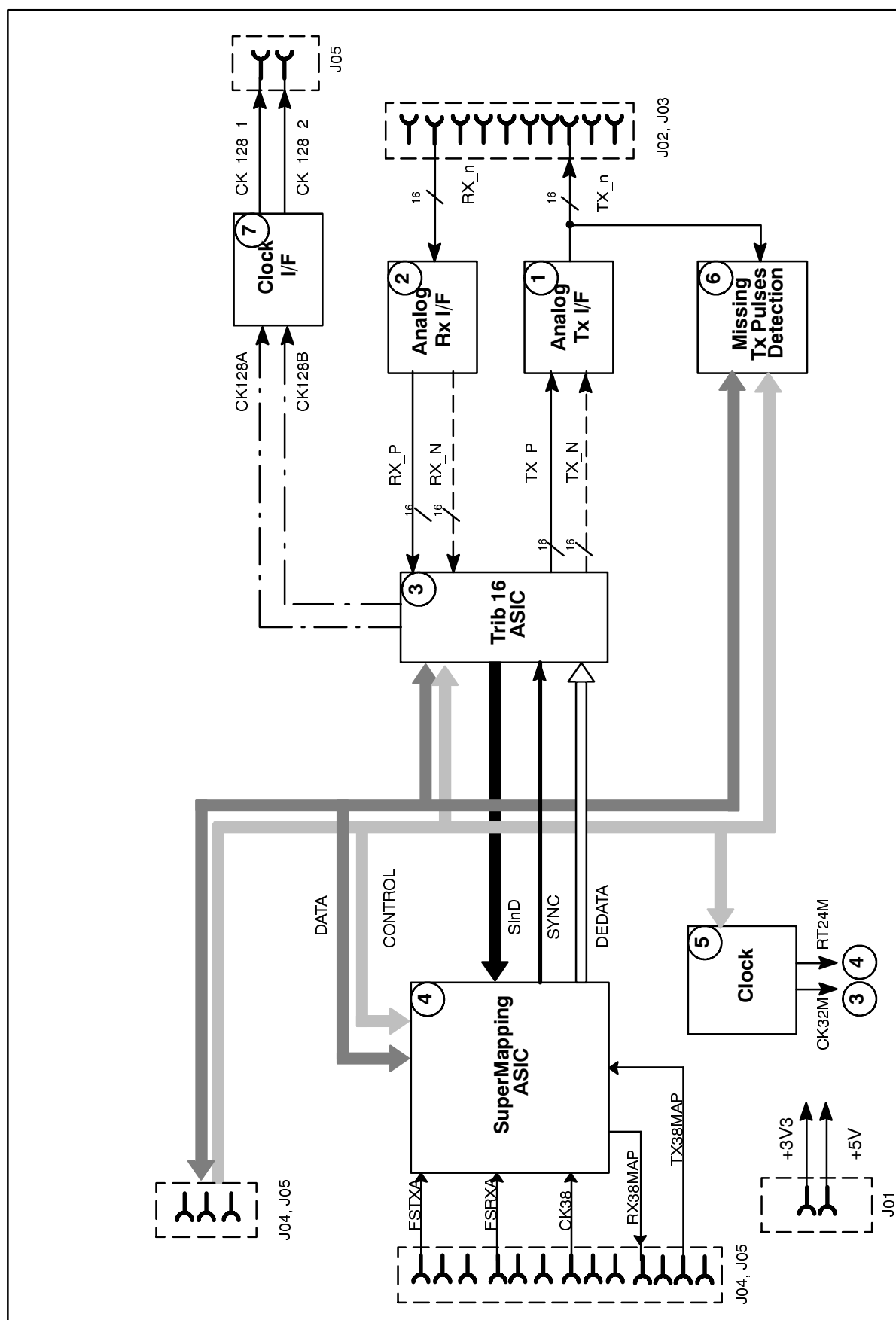


Fig. 5.2-7 Simplified block diagram of 16x2Mbit/s Tributary Sub-Unit

In the following reference will be made to the previous block diagram.

Functional Description

Reception Functions

The sixteen incoming PDH signals (RX_n with n from 1 to 16) are received by the analog RX interface (**Block 2**) which ensures an impedance match and sends the signals RX_P and RX_N towards the TRIB16 ASIC (**Block 3**).

The analog signals are converted from the line code (HDB3, AMI, B8ZS) into NRZ code. In this step is also checked the presence of incoming AIS or LOS indications.

The NRZ PDH signals are inserted into SDH C12/C11 containers, defined in ITU-T Rec. G.707 (the clock reference is derived by the 19.44MHz clock issued by SUPERMAPPING ASIC). In this operation justification takes place, in order to recover any eventual frequency offset (a maximum offset of ± 50 p.p.m. is allowed).

The sixteen C12/C11s are converted into VC12s, by adding fixed stuff and the following bytes: V5 (POH), N2 (tandem connection monitoring), J2 (path trace identifier) and K4 (user defined).

The VC-12s are inserted in TU-12s with an offset defined by the pointer made of V1 and V2 bytes. This offset is introduced in order to minimize the jitter.

The sixteen TU-12s are inserted into a proprietary STM-1 signal. The position of TU-12s inside the proprietary STM-1 is given by a clock (CK4SI) issued by the SUPERMAPPING ASIC towards the TRIB16 ASIC. Also the 19.44MHz timing signal (CK19SI) used to generate the parallel proprietary STM-1 is issued by SUPERMAPPING ASIC.

The TRIB16 ASIC issues an 8-bit proprietary STM-1 (SInD) towards the SUPERMAPPING ASIC. This proprietary STM-1 is mapped into the payload of another STM-1 signal.

The SUPERMAPPING ASIC adds the alignment word and a diagnostic message to the overhead of this STM-1 signal (the diagnostic message includes informations as the equipment number, the channel number, the unit type, etc.).

The STM-1 signal is then converted into a nibble format (at a frequency of 38.88MHz) and sent towards the switch, by using the signals RX38MAP.

Transmission Functions

The SUPERMAPPING ASIC (**Block 4**) receives a STM-1 signal from the switch (TX38MAP) together with a 38.88MHz clock signal (CK38).

On the STM-1 stream is checked the V4 diagnostic message. This check includes the detection of the alignment word, the parity check and the check of equipment type, equipment number, channel number, etc.

The STM-1 signal is converted into a parallel 8-bit format (at a frequency of 19.44 MHz) and is sent towards the TRIB16 ASIC. To TRIB16 ASIC are also sent two clock signals: CK4DEn which is used by TRIB16 ASIC to extract its relevant sixteen TU-12s; CK19DE which is used by TRIB16 ASIC to read the 19.44MHz signal.

For each TU-12 are extracted the V1 and V2 bytes and is determined the location of each VC12. Once the V5 byte is found all the other bytes of POH are determined (N2, J2 and K4). These bytes are used to check the signal label match, the path trace match, the signal parity, etc.

From each VC12 is extracted the PDH payload which is then converted from NRZ code into the line code (HDB3, AMI, B8ZS).

From TRIB16 ASIC sixteen analog signals (TX_P and TX_N) are sent towards the analog TX interface (**Block 1**). On **Block 1** an impedance match is performed, then the TX_n signals (with n from 1 to 16) are sent towards the backpanel connector.

The TX_n signals are used, on **Block 6**, to detect any eventual missing Tx pulse. The indication of eventual missing pulses is stored on a register and can be recovered by the microprocessor of master MOST Unit.

Common Functions

For the description of 16x1.5/2Mbit/s Tributary Sub-unit make reference to the description of 32x1.5/2Mbit/s Tributary Sub-unit.

8x2Mbit/s + 1x34Mbit/s Tributary Sub-Unit (130-3545/02)

General Information

The 8x2Mbit/s + 1x34Mbit/s Tributary Sub-Unit operates as a 1.5/2Mbit/s and 34Mbit/s signal tributary and processor (multiplexing/demultiplexing).

The treated signals are compliant with ITU-T Recommendation G.703.

For the further details about the 1.5/2Mbit/s and 34Mbit/s signal characteristics refer to chapter "Information for the System Engineer"

Functions

The 8x2Mbit/s + 1x34Mbit/s Tributary Sub-Unit supports the following functions:

- ◆ *reception/Transmission of an electrical 1.5/2Mbit/s signal (HDB3, AMI, B8ZS, NRZ);*
- ◆ *reception/Transmission of an electrical 34Mbit/s signal (HDB3);*
- ◆ *conversion of incoming signals into NRZ code;*
- ◆ *conversion of outgoing 1.5/2Mbit/s signal from NRZ to tributary line code (HDB3, AMI, B8ZS);*
- ◆ *conversion of outgoing 34Mbit/s signal from NRZ to tributary line code HDB3;*
- ◆ *mapping of tributary signals into TU-n (2Mbit/s into TU-12, 34Mbit/s into TU-3), with insertion of control and justification bits;*
- ◆ *mapping of TU-n into a pseudo-STM-1 structure;*
- ◆ *extraction of TU-n from a pseudo-STM-1 structure;*
- ◆ *extraction of tributary signals from TU-n (2Mbit/s from TU-12, 34Mbit/s from TU-3);*
- ◆ *internal clock generatio;*
- ◆ *clock reference generatio.*

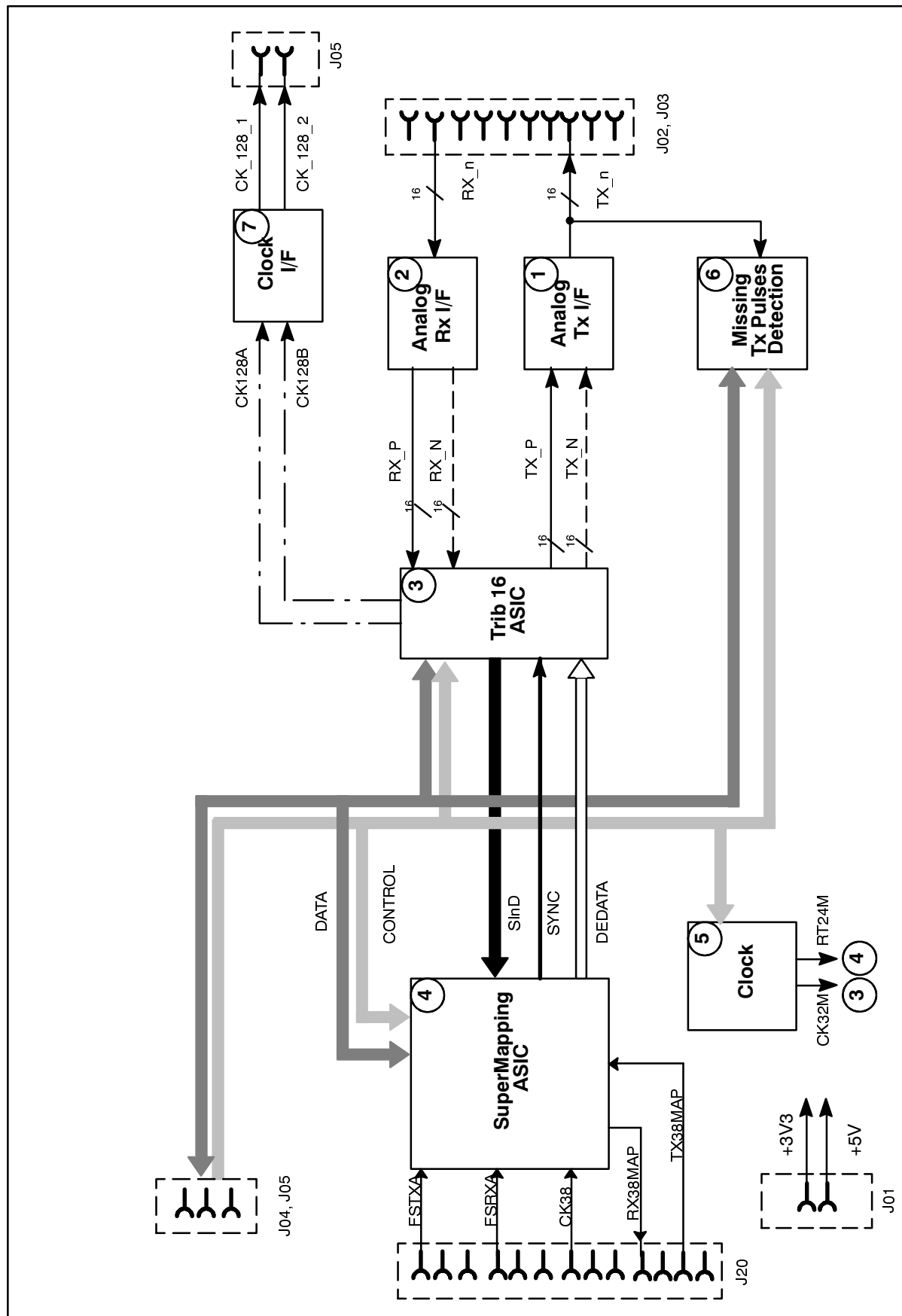


Fig. 5.2-8 Simplified block diagram of 2Mbit/s channel management

Functional Description

2Mbit/s Reception Functions

The eight incoming PDH signals (RX_n with n from 1 to 8) are received by the analog RX interface (**Block 2**) which ensures an impedance match and sends the signals RX_P and RX_N towards the TRIB16 ASIC (**Block 3**).

The analog signals are converted from the line code (HDB3, AMI, B8ZS) into NRZ code. In this step is also checked the presence of incoming AIS or LOS indications.

The NRZ PDH signals are inserted into SDH C12/C11 containers, defined in ITU-T Rec. G.707 (the clock reference is derived by the 19.44MHz clock issued by SUPERMAPPING ASIC). In this operation justification takes place, in order to recover any eventual frequency offset (a maximum offset of ± 50 p.p.m. is allowed).

The sixteen C12/C11s are converted into VC12s, by adding fixed stuff and the following bytes: V5 (POH), N2 (tandem connection monitoring), J2 (path trace identifier) and K4 (user defined).

The VC-12s are inserted in TU-12s with an offset defined by the pointer made of V1 and V2 bytes. This offset is introduced in order to minimize the jitter.

The eight TU-12s are inserted into a proprietary STM-1 signal. The position of TU-12s inside the proprietary STM-1 is given by a clock (CK4SI) issued by the SUPERMAPPING ASIC towards the TRIB16 ASIC. Also the 19.44MHz timing signal (CK19SI) used to generate the parallel proprietary STM-1 is issued by SUPERMAPPING ASIC.

The TRIB16 ASIC issues an 8-bit proprietary STM-1 (SInD) towards the SUPERMAPPING ASIC. This proprietary STM-1 is mapped into the payload of another STM-1 signal.

The SUPERMAPPING ASIC adds the alignment word and a diagnostic message to the overhead of this STM-1 signal (the diagnostic message includes informations as the equipment number, the channel number, the unit type, etc.).

The STM-1 signal is then converted into a nibble format (at a frequency of 38.88MHz) and sent towards the switch, by using the signals RX38MAP.

2Mbit/s Transmission Functions

The SUPERMAPPING ASIC (**Block 4**) receives a STM-1 signal from the switch (TX38MAP) together with a 38.88MHz clock signal (CK38).

On the STM-1 stream is checked the V4 diagnostic message. This check includes the detection of the alignment word, the parity check and the check of equipment type, equipment number, channel number, etc.

The STM-1 signal is converted into a parallel 8-bit format (at a frequency of 19.44 MHz) and is sent towards the TRIB16 ASIC. To TRIB16 ASIC are also sent two clock signals: CK4DEn which is used by TRIB16 ASIC to extract its relevant sixteen TU-12s; CK19DE which is used by TRIB16 ASIC to read the 19.44MHz signal.

For each TU-12 are extracted the V1 and V2 bytes and is determined the location of each VC12. Once the V5 byte is found all the other bytes of POH are determined (N2, J2 and K4). These bytes are used to check the signal label match, the path trace match, the signal parity, etc.

From each VC12 is extracted the PDH payload which is then converted from NRZ code into the line code (HDB3, AMI, B8ZS).

From TRIB16 ASIC eight analog signals (TX_P and TX_N) are sent towards the analog TX interface (**Block 1**). On **Block 1** an impedance match is performed, then the TX_n signals (with n from 1 to 8) are sent towards the backpanel connector.

The TX_n signals are used, on **Block 6**, to detect any eventual missing Tx pulse. The indication of eventual missing pulses is stored on a register and can be recovered by the microprocessor of master MOST Unit.

34Mbit/s Reception Functions

The incoming PDH signal (RX) is received by the analog RX interface which ensures an impedance match and sends the signals RX_P and RX_N towards the TRIB ASIC.

The analog signal is converted from the line code (HDB3) into NRZ code. In this step is also checked the presence of incoming AIS or LOS indications.

The NRZ PDH signal is inserted into SDH C3 container, defined in ITU-T Rec. G.707 (the clock reference is derived by the 19.44MHz clock issued by SUPERMAPPING ASIC). In this operation justification takes place, in order to recover any eventual frequency offset (a maximum offset of ± 30 p.p.m. is allowed).

The container is converted into VC3, by adding fixed stuff and the following bytes.

The VC is inserted in TU with an offset defined by the pointer bytes. This offset is introduced in order to minimize the jitter.

The TU is inserted into a proprietary STM-1 signal. The position of TU inside the proprietary STM-1 is given by a clock (CK4SI) issued by the SUPERMAPPING ASIC towards the TRIB ASIC. Also the 19.44MHz timing signal (CK19SI) used to generate the parallel proprietary STM-1 is issued by SUPERMAPPING ASIC.

The TRIB ASIC issues an 8-bit proprietary STM-1 (SInD) towards the SUPERMAPPING ASIC. This proprietary STM-1 is mapped into the payload of another STM-1 signal.

The SUPERMAPPING ASIC adds the alignment word and a diagnostic message to the overhead of this STM-1 signal (the diagnostic message includes informations as the equipment number, the channel number, the unit type, etc.).

The STM-1 signal is then converted into a nibble format (at a frequency of 38.88MHz) and sent towards the switch, by using the signals RX38MAP.

34Mbit/s Transmission Functions

The SUPERMAPPING ASIC receives a STM-1 signal from the switch (TX38MAP) together with a 38.88MHz clock signal (CK38).

On the STM-1 stream is checked the V4 diagnostic message. This check includes the detection of the alignment word, the parity check and the check of equipment type, equipment number, channel number, etc.

The STM-1 signal is converted into a parallel 8-bit format (at a frequency of 19.44 MHz) and is sent towards the TRIB ASIC. To TRIB16 ASIC are also sent two clock signals: CK4DEn which is used by TRIB16 ASIC to extract its relevant TU; CK19DE which is used by TRIB ASIC to read the 19.44MHz signal.

From the TU the pointer bytes are extracted, and is determined the location of each VC. Once the POH byte are found all the other service bytes are determined. These bytes are used to check the signal label match, the path trace match, the signal parity, etc.

From each VC is extracted the PDH payload which is then converted from NRZ code into the line code (HDB3).

From TRIB ASIC the analog signal (TX_P and TX_N) is sent towards the analog TX interface. An impedance match is performed, then the TX_n signals (with n from 1 to 8) are sent towards the backpanel connector.

The TX_n signals are used to detect any eventual missing Tx pulse. The indication of eventual missing pulses is stored on a register and can be recovered by the microprocessor of master MOST Unit.

Common Functions

Timing Functions

The 16x2Mbit/s Tributary Unit is equipped with a VCO, working at 65.586MHz. This clock reference is used by TRIB16 ASIC (**Blocks 4**) to read and write the 2Mbit/s signals.

Reference Clock

The 16x2Mbit/s Tributary Unit issues two 128 kHz clock signals (CK_128_1 and CK_128_2), towards the two Switches. These signals are generated by TRIB16 ASIC (**Blocks 4**) selecting two extracted 2Mbit/s (1.5Mbit/s) clock references.

1x34Mbit/s G.703 Tributary Sub-unit (130-3545/01)

General Information

The 1x34Mbit/s G.703 Tributary Sub-unit operates as 34Mbit/s signal tributary and processor (multiplexing/demultiplexing).

The treated signals are compliant with ITU-T Recommendation G.703.

————— *Fo further details about the 34Mbit/s signal characteristics refer to chapter "Information for the System Engineer"*

Functions

The 1x34Mbit/s G.703 Tributary Sub-unit supports the following functions:

- ◆ *reception/Transmission of an electrical 34Mbit/s signal (HDB3);*
- ◆ *conversion of incoming signals into NRZ code;*
- ◆ *conversion of outgoing 34Mbit/s signal from NRZ to tributary line code HDB3;*
- ◆ *mapping of 34Mbit/s tributary signals into TU-3 with insertion of control and justification bits;*
- ◆ *mapping of TU-3 into a pseudo-STM-1 structure;*
- ◆ *extraction of TU-3 from a pseudo-STM-1 structure;*
- ◆ *extraction of 34Mbit/s tributary signals from TU-3;*
- ◆ *internal clock generation;*
- ◆ *clock reference generation.*

Functional Description

34Mbit/s Reception Functions

The incoming PDH signal (RX) is received by the analog RX interface which ensures an impedance match and sends the signals RX_P and RX_N towards the TRIB ASIC.

The analog signal is converted from the line code (HDB3) into NRZ code. In this step is also checked the presence of incoming AIS or LOS indications.

The NRZ PDH signal is inserted into SDH C3 container, defined in ITU-T Rec. G.707 (the clock reference is derived by the 19.44MHz clock issued by SUPERMAPPING ASIC). In this operation justification takes place, in order to recover any eventual frequency offset (a maximum offset of ± 30 p.p.m. is allowed).

The container is converted into VC3, by adding fixed stuff and the following bytes.

The VC is inserted in TU with an offset defined by the pointer bytes. This offset is introduced in order to minimize the jitter.

The TU is inserted into a proprietary STM-1 signal. The position of TU inside the proprietary STM-1 is given by a clock (CK4SI) issued by the SUPERMAPPING ASIC towards the TRIB ASIC. Also the 19.44MHz timing signal (CK19SI) used to generate the parallel proprietary STM-1 is issued by SUPERMAPPING ASIC.

The TRIB ASIC issues an 8-bit proprietary STM-1 (SInD) towards the SUPERMAPPING ASIC. This proprietary STM-1 is mapped into the payload of another STM-1 signal.

The SUPERMAPPING ASIC adds the alignment word and a diagnostic message to the overhead of this STM-1 signal (the diagnostic message includes informations as the equipment number, the channel number, the unit type, etc.).

The STM-1 signal is then converted into a nibble format (at a frequency of 38.88MHz) and sent towards the switch, by using the signals RX38MAP.

34Mbit/s Transmission Functions

The SUPERMAPPING ASIC receives a STM-1 signal from the switch (TX38MAP) together with a 38.88MHz clock signal (CK38).

On the STM-1 stream is checked the V4 diagnostic message. This check includes the detection of the alignment word, the parity check and the check of equipment type, equipment number, channel number, etc.

The STM-1 signal is converted into a parallel 8-bit format (at a frequency of 19.44 MHz) and is sent towards the TRIB ASIC. To TRIB16 ASIC are also sent two clock signals: CK4DEn which is used by TRIB16 ASIC to extract its relevant TU; CK19DE which is used by TRIB ASIC to read the 19.44MHz signal.

From the TU the pointer bytes are extracted, and is determined the location of each VC. Once the POH byte are found all the other service bytes are determined. These bytes are used to check the signal label match, the path trace match, the signal parity, etc.

From each VC is extracted the PDH payload which is then converted from NRZ code into the line code (HDB3).

From TRIB ASIC the analog signal (TX_P and TX_N) is sent towards the analog TX interface. An impedance match is performed, then the TX_n signals (with n from 1 to 8) are sent towards the backpanel connector.

The TX_n signals are used to detect any eventual missing Tx pulse. The indication of eventual missing pulses is stored on a register and can be recovered by the microprocessor of master MOST Unit.

Common Functions

Timing Functions

The 16x2Mbit/s Tributary Unit is equipped with a VCO, working at 65.586MHz. This clock reference is used by TRIB16 ASIC (**Blocks 4**) to read and write the 2Mbit/s signals.

Reference Clock

The 16x2Mbit/s Tributary Unit issues two 128 kHz clock signals (CK_128_1 and CK_128_2), towards the two Switches. These signals are generated by TRIB16 ASIC (**Blocks 4**) selecting two extracted 2Mbit/s (1.5Mbit/s) clock references.

Common Parts (130–3492/xx)

General Information

The Common Parts Sub–Unit operates as a Controller for the whole equipment, as a switch, as a timing reference source and, partially, as a SOH manager.

Functions

The Common Parts Sub–Unit supports the following functions:

- ◆ *reception/Transmission of eight STM–1 buses (on four bit) at a 38.88Mbit/s bitrate;*
- ◆ *processing of two STM–1 buses (from the line modules) from STM–1 level to VC–4;*
- ◆ *processing of two STM–1 buses (from the line modules) from VC–4 level to TU–12, including rejustification and TU control;*
- ◆ *processing of two STM–1 buses (from the line modules) from TU–12 level to VC–4, with insertion of control and justification bits;*
- ◆ *processing of two STM–1 buses (from the line modules) from VC–4 level to STM–1;*
- ◆ *management of cross connections;*
- ◆ *management of MSP protection;*
- ◆ *management of tributary unit protection;*
- ◆ *management of SNCP protection;*
- ◆ *unit and equipment supervision;*
- ◆ *management of a maximum of four DCCs;*
- ◆ *internal clock generation;*
- ◆ *management of F interface towards the Local Controller;*
- ◆ *Unit Power Supply by means of a DC/DC converter, present on the unit itself;*
- ◆ *alarm indication (Front Panel LEDs).*

Functional Description

In this paragraph reference will be made to the following block diagram.

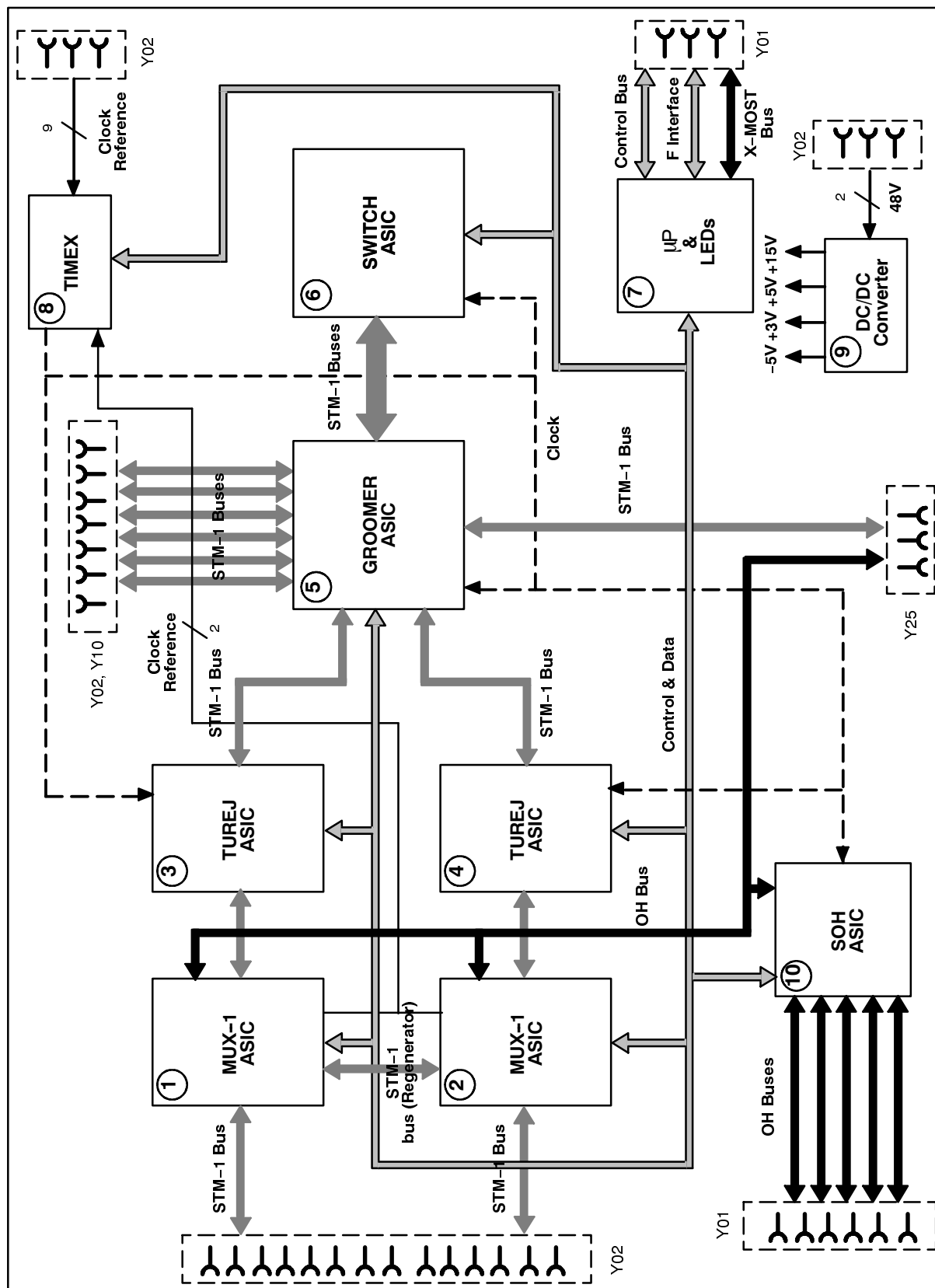


Fig. 5.2-9 Common Parts Sub-Unit Simplified Block Diagram

Reception Functions

The MUX-1 ASICs (**Block 1 and 2**) receive a four-bit bus (at 38.88MHz) with a NRZ STM-1 signal and an indication of the received clock. The first operation is the extraction and check of alignment word (bytes A1 and A2 of SOH).

Then a descrambling operation is performed and the SOH bytes are extracted.

Since the MSH11C can operate either as an Add/Drop (Terminal) or as a Regenerator, there are two different ways to handle the STM-1 stream.

Regenerator

For the Regenerator only the RSOH bytes are extracted:

- ◆ *bytes A1, A2, J0, B1 and B2 are processed directly by MUX-1 ASIC. which emits any possible alarm indication towards the microprocessor;*
- ◆ *all the other bytes of RSOH are issued to the OVERHEAD BUS.*

After the SOH processing, the MUX-1 ASICs send a four-bit STM-1 signal, at 38.88MHz, towards back panel, where it will be recovered by the other line MUX-1 ASIC.

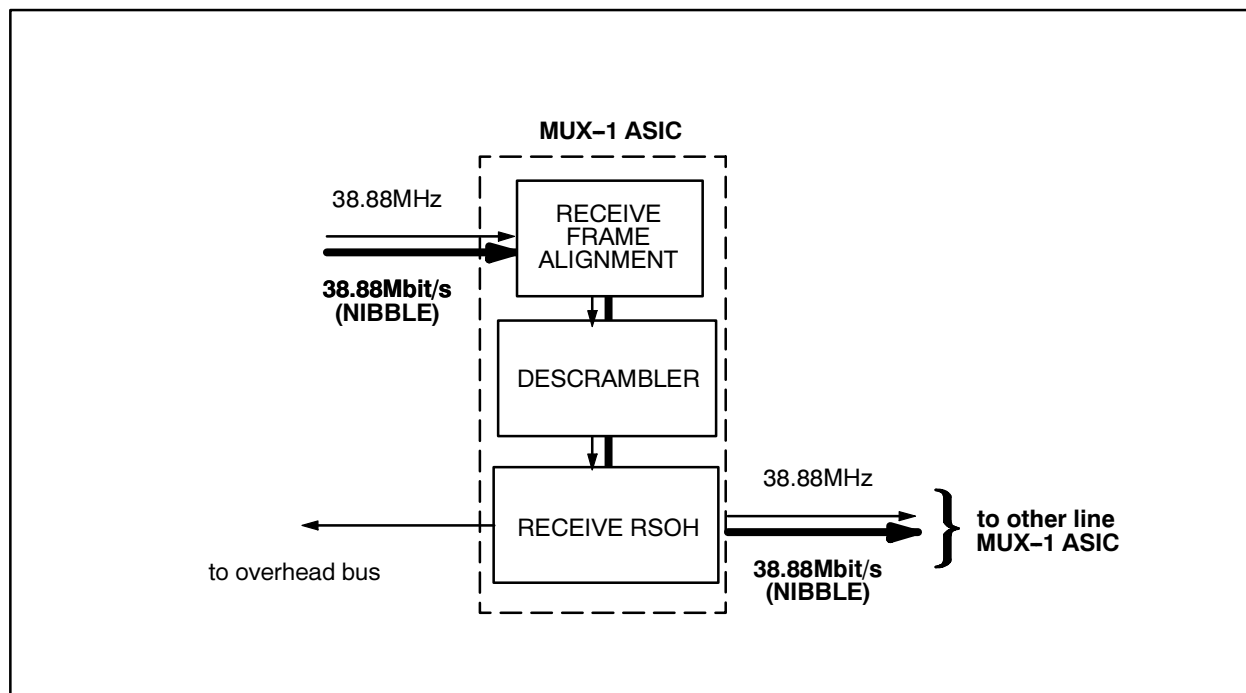


Fig. 5.2-10 Simplified block diagram of MUX -1 ASIC – Receive side: Regenerator

Add/Drop (Terminal)

For the Add/Drop (Terminal) both the RSOH bytes and the MSOH bytes are extracted:

- ◆ *bytes A1, A2, B1 and B2 are processed directly by MUX-1 ASICs. which emit any possible alarm indication towards the microprocessor;*
- ◆ *byte J0 (Section Trace Identifier) is processed to detect any mismatch between the received and the expected values;*
- ◆ *bytes for synchronization quality (S1) and for MSP signalling (K1 and K2), are sent towards the GROOMER ASIC (**Block 5**) on a proprietary STM-1 frame;*
- ◆ *all the other bytes of SOH are issued to the OH BUS.*

After the SOH processing, the MUX-1 ASICs process the Administrative Unit pointer and, eventually, performs an Administrative Unit rejustification, in order to synchronize the STM-1 payload with the clock signal received from the TIMEX (**Block 8**).

Once the payload is synchronized, the MUX-1 ASICs extract the POH of the higher order Virtual Container. From this POH it is extracted the byte J1 (Path Trace Identifier), in order to detect any eventual mismatch between the received and expected values. The content of this POH is then elaborated and issued on the Control Bus and on the OH BUS.

The payload of higher order Virtual Container is passed into a eight-bit format and it is sent towards REJUSTIFIER ASICs (**Blocks 3 and 4**) by means of a eight bits bus (at 19.44MHz).

On the REJUSTIFIER ASICs the TU POH and pointer are processed. Some of the Overhead bytes are directly managed by MUX-1 ASICs, some other are sent, part on the OH bus, part on the proprietary STM-1 stream and, after pointer interpretation, the TU payload is rejustified, in order to ensure a synchronization of incoming signal with the clock used by the switch.

From **Blocks 3 and 4** the signal is issued towards the GROOMER ASIC (**Block 5**) on four-bit buses, at 38.88MHz (these buses are doubled and sent towards either the GROOMER ASIC on the same card or the GROOMER ASIC on the other MOST Unit).

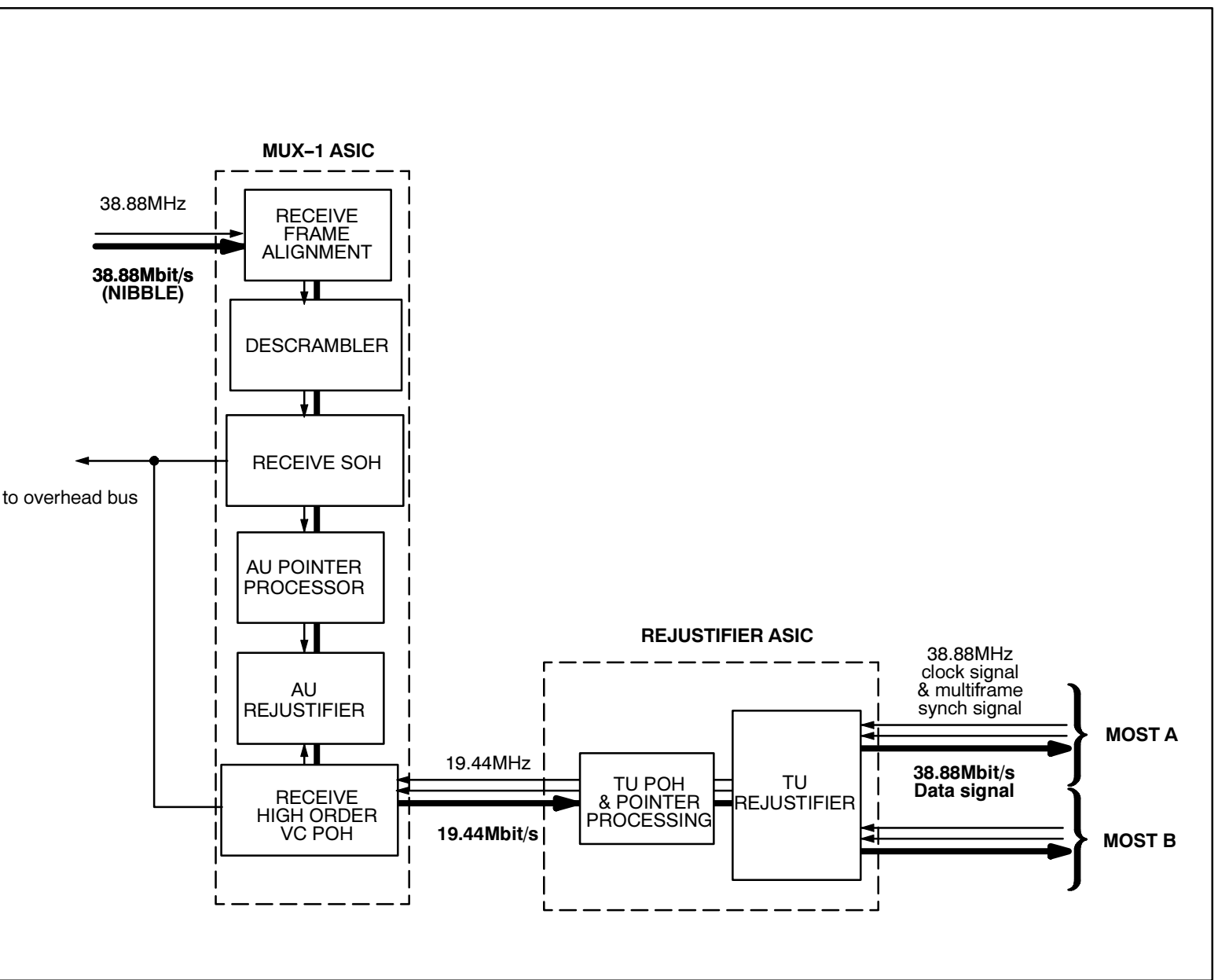


Fig. 5.2-II Simplified block diagram of MUX-1 ASIC and REJUSTIFIER ASIC – Receive side:
Add/Drop (Terminal)

Transmission Functions

As on the receive side, there are two different ways to handle the STM-1 stream.

Regenerator

The MUX-1 ASICs receive a four bit STM-1 signal, at 38.88MHz, from the other line MUX-1 ASICs, through the back panel. Then the RSOH is added to the STM-1 signal.

As on the receive side, some bytes of RSOH are directly managed by MUX-1 ASICs and the other are recovered from the OH bus.

Then the NRZ signal is scrambled and is sent on a four bits bus, at 38.88MHz.

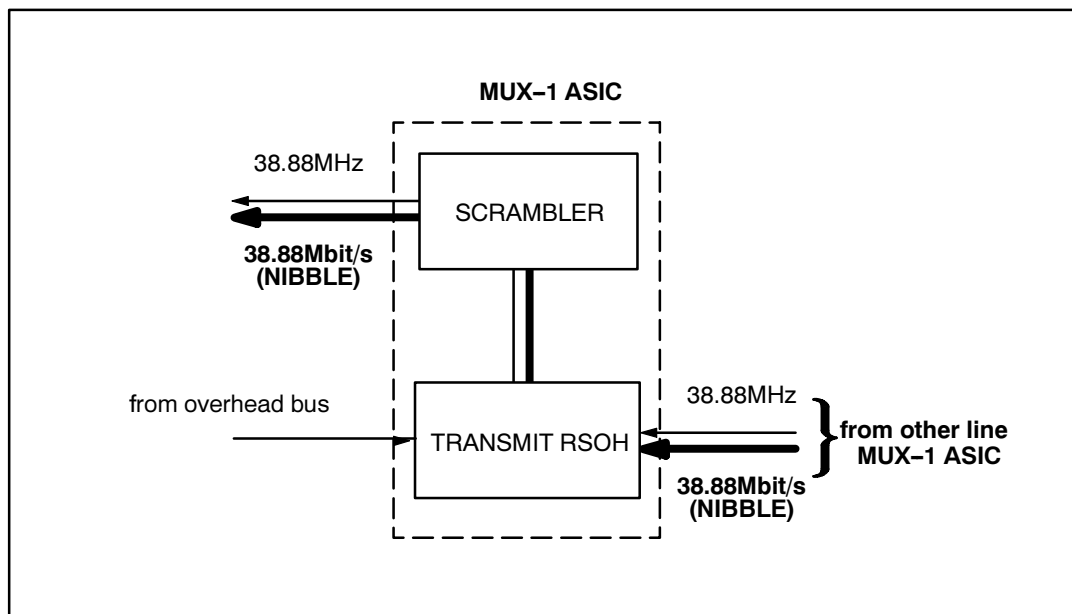


Fig. 5.2-12 Simplified block diagram of MUX ASIC – Transmit side: Regenerator

Add/Drop (Terminal)

On **Blocks 3** and **4** are received two eight-bit buses at a bitrate of 38.88Mbit/s, from the two GROOMER ASICs (if a second MOST Unit is present). To each data signal are paired a multiframe synchronization signal and a 38.88MHz clock signal.

The REJUSTIFIER ASICs perform a check to determine which signal has to be used (the one from MOST A or the one from MOST B). The results of this check is issued on the CONTROL BUS, to the master MOST Controller, which decides the exact signal to be used.

The transmit signal has not to be rejustified, so the REJUSTIFIER ASICs only add the Tributary Unit POH, and issue an eight-bit bus (with a bitrate of 19.44 Mbit/s) towards **Blocks 1** and **2** (MUX-1 ASICs).

The MUX-1 ASICs add the Higher Order VC Overhead, the AU pointer and the SOH. The Overhead bytes come from the GROOMER ASICs on the STM-1 proprietary frame (bytes K1, K2 and S1), are managed directly on the line interface (bytes J0, J1) or come from the OH bus.

The obtained signal is scrambled and sent towards STM-1 line modules, on a four-bit bus (at a bitrate of 38.88Mbit/s).

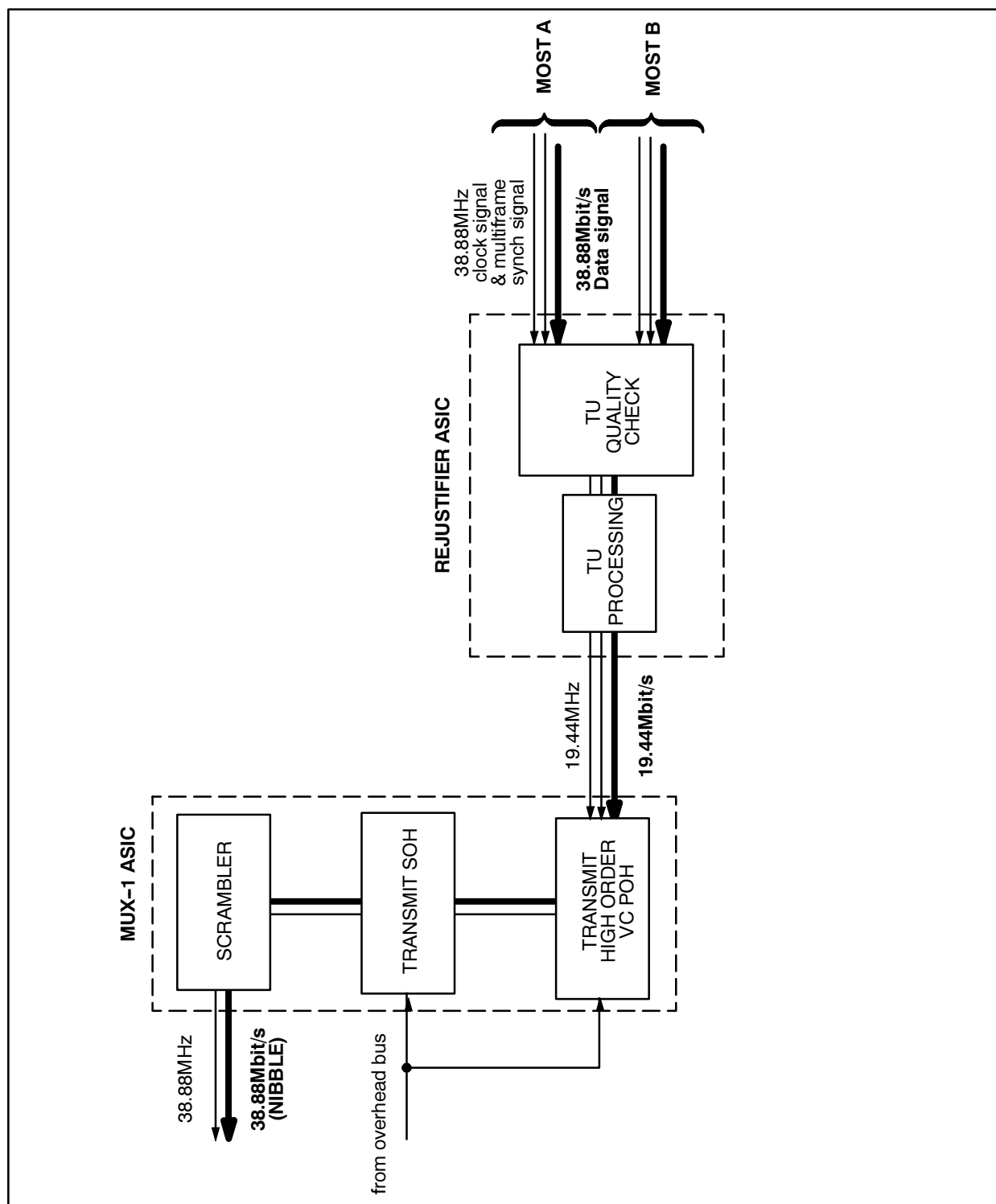


Fig. 5.2-13 Simplified block diagram of MUX ASIC and REJUSTIFIER ASIC- Transmit side: Add/Drop (Terminal)

Cross Connection Functions

The GROOMER ASIC (**Block 5**) receives the following eight STM-1 buses, at 38.88MHz:

- ◆ *two from the TUREJ ASICs on the card itself;*
- ◆ *two from the TUREJ ASICs on the other MOST Unit (if present);*
- ◆ *one from the Tributary Module of the card itself;*
- ◆ *one from the GROOMER ASIC of the other MOST Unit (if present);(*)*
- ◆ *three from the Tributary Units.*

At first the GROOMER ASIC handle the Overhead bytes of the incoming streams. The Overhead bytes handled directly by the GROOMER ASIC or in cooperation with the microprocessor (**Block 7**) are the following:

- ◆ *K1, K2 (bytes fof APS communications);*
- ◆ *S1 (synchronization quality);*
- ◆ *parity check (bits 1 and 2 of byte V5).*

After the Overhead management, **Block 5** is used to associate each incoming STM-1 stream to an STM-1 stream outgoing towards the SWITCH ASIC (**Block 6**). The GROOMER ASIC is used to implement cross connections at an AU-4 level.

The SWITCH ASIC receives eight 38.88MHz STM-1 buses from the GROOMER ASIC. These buses are taken two by two and byte multiplexed, in order to obtain four eight-bit signals, each containing two byte interleaved STM-1 streams.

Each of these signals is sent towards a four DATA RAM bank. These banks are composed by four RAMs and the multiplexed STM-1 stream is sent to all of them.

Each RAM is connected to four 4:1 Multiplexer by a eight-bit line. Cross connections at TU level are implemented by reading the RAM memories and activating the 4:1 Multiplexers, following a scheme defined by the control logic, under the supervision of microprocessor.

NOTE (*) *This STM-1 stream is used for the signal of the Tributary Module of the other MOST Unit. If the GROOMER ASIC on the second MOST Unit gets failed, this Tributary Module becomes unreachable.*

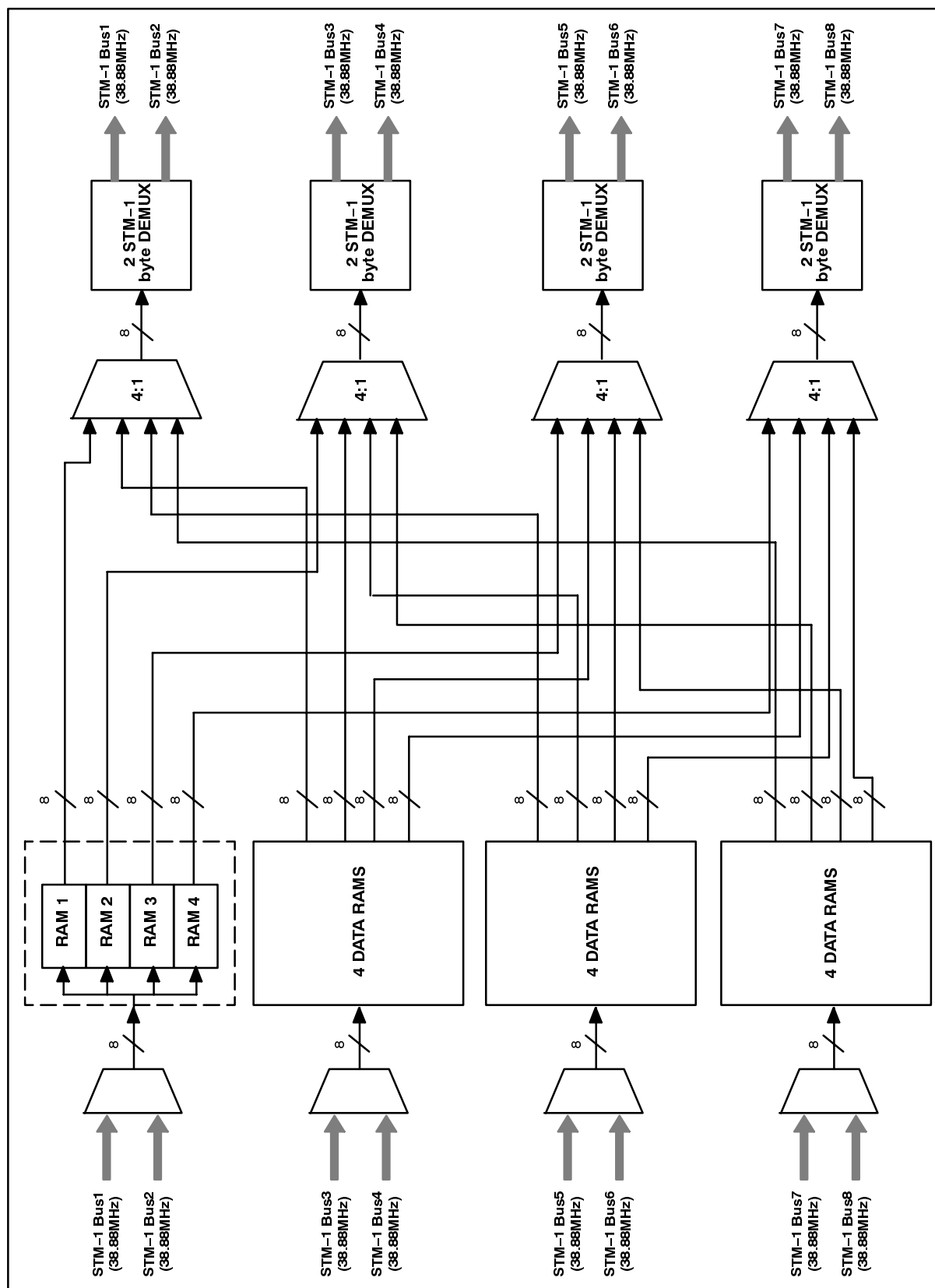


Fig. 5.2-14 Block Diagram of SWITCH 8x8 ASIC

The data outgoing from the 4:1 Multiplexers are sent towards four Demultiplexers which divide the eight-bit signal into two four-bit 38.88MHz signals.

These eight STM-1 streams are sent towards GROOMER ASIC which inserts the following Overhead bytes:

- ◆ *K1, K2 (bytes of APS communications);*
- ◆ *S1 (synchronization quality).*

Then eight STM-1 buses, at 38.88MHz are sent by the GROOMER ASIC:

- ◆ *two towards the TUREJ ASICs on the card itself;*
- ◆ *two towards the TUREJ ASICs on the other MOST Unit (if present);*
- ◆ *one towards the Tributary Module of the card itself;*
- ◆ *one towards the GROOMER ASIC of the other MOST Unit (if present);*
- ◆ *three towards the Tributary Units.*

MSP Protection

The GROOMER ASIC (**Block 5**) handles bytes K1 and K2 of SOH, used to manage MSP protection.

Block 5 extracts these bytes from the SOH of the protection line and send them towards microprocessor, which elaborates them and communicates to the GROOMER ASIC the STM-1 stream to be used as working one.

Other switching criteria can be the detection of a signal degrade or failure on the line (these indication are sent, from the line interfaces, towards the GROOMER ASIC, using the STM-1 internal streams), or a software command.

For further details about MSP Protection refer to chapter "Information for the System Engineer"

Tributary Unit Protection

MSH11C allows a 1+1 Tributary Card Protection.

In the protection scheme the incoming tributary streams are doubled (one from the working unit and the other from the protection one). Therefore the GROOMER ASIC can select between two STM-1 streams, associated to the same tributary input.

The fault detection of a protected tributary unit is performed by the microprocessor (**Block 7**) which communicates to the GROOMER ASIC the STM-1 stream to be used for the protected unit.

On the transmission side the selection between the working and the protection signal is made on the Connection Unit.

For further details about Tributary Unit Protection refer to chapter "Information for the System Engineer"

SNC Protection

Together with cross connections, the SWITCH ASIC (**Block 6**) can handle SNC protection, from AU-4 to TU-12 level.

The control logic for DATA RAM reading, receives, from MUX-1 ASICs or TUREJ ASICs which elaborate SOH and VC POH, the indication of Signal Failure or Signal Degrade.

This indication allows the control logic to select, in a path protected cross connection, the VC to be used on the line side.

For further details about SNC Protection refer to chapter "Information for the System Engineer"

Supervision Functions

The microprocessor (**Block 7**) can detect failures and malfunctioning conditions both on the unit components and on all the units of the equipment. The alarms are issued towards the Local Controller and are displayed on the front panel LEDs.

The microprocessor is also used to send configuration messages to the different components of the equipment. For this purpose it communicates with other units through the Control Bus.

Since only one MOST Unit has the full control of the equipment (MASTER state), there is a communication bus between the two MOST Units (when fitted). Through this bus the stand-by MOST Unit can detect whether the other one is properly operating or not and, if necessary, can switch to MASTER state.

This bus is also used by the MASTER MOST Unit to access information about the state of line and tributary modules on the other MOST Unit.

DCCs Management

If a Communication Unit is not present, the MOST Unit can manage up to four DCC channels. This operation is performed by SOH ASIC (**Block 10**) together with the microprocessor (**Block 7**).

The SOH ASIC can handle a maximum of four OH buses that are selected from the four lines and four tributaries (two tributary units and two tributary modules). The selection is made on the Local Controller, using the following alternatives:

- ◆ *Line West A or Line West B*
- ◆ *Line East A or Line East B*
- ◆ *Line West B or Tributary Unit 2 or Tributary Module A*
- ◆ *Line East B or Tributary Unit 1 or Tributary Module B*

The serial OH signal is converted into a parallel format (8-bit). Then the SOH ASIC determines which frame timeslots have to be extracted and performs a rejustification of POH timeslots). The extracted data are written into a data channel store.

Each OH channel is associated to an outgoing data channel. Each data channel can be configured as:

- ◆ *DCCm* – 576 kbit/s (bytes D4–D12 of SOH);
- ◆ *DCCr* – 192 kbit/s (bytes D1–D3 of SOH);
- ◆ 64 kbit/s (bytes from SOH);
- ◆ 64 kbit/s (bytes from POH).

The relevant bytes previously stored are converted into a serial format and sent on the selected data channel towards the microprocessor.

The 64kbit/s timing reference is extracted from a 38.88MHz clock reference incoming from the TIMEX (**Block 8**).

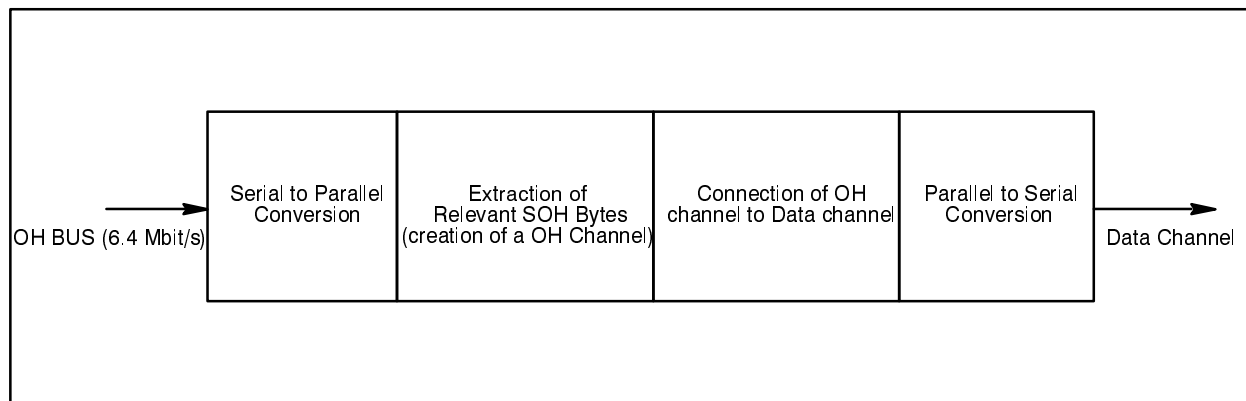


Fig. 5.2-15 Functional block diagram of SOH ASIC: Receive side

The SOH ASIC connects a data channel to a SOH bus and converts the incoming data from a serial to a parallel format (8-bit). This data stream is written into a transmit store.

Using one the 38.88MHz clock reference incoming from the TIMEX, is generated a 6.48MHz clock reference.

The transmit store is read at appropriate timeslots by the OH channel, which uses the 6.48MHz clock reference. The bytes from OH channel are inserted in the appropriate timeslots in the OH frame, considering also stuffing due to POH justification.

The OH channel is then converted from a parallel to a serial format and sent, on the relevant SOH bus, towards the different cards or modules.

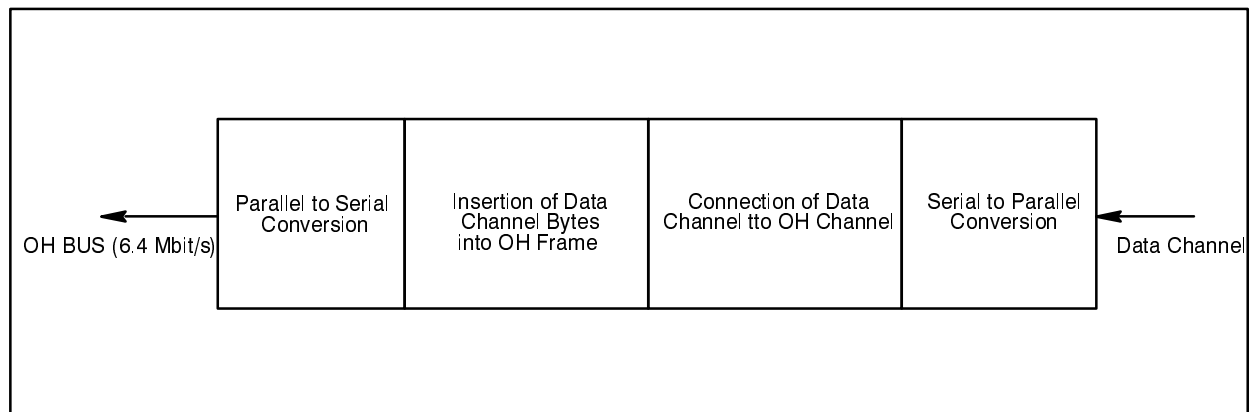


Fig. 5.2-16 Functional block diagram of SOH ASIC: Transmit side

Timing Functions

The MOST Unit is provided with the TIMEX component (**Block 8**) which can extract a clock for the whole equipment, selecting among eleven timing references. These timing reference are represented by 128KHz signals, incoming from the four lines and from five tributary ports, and by 2048Hz signals from two external sources.

The TIMEX component can select one of these sources or can operate in Free running or Holdover modes. The resulting clock signal is used to synchronize the outgoing signals (tributary and line) and to provide external timing references.

A 38.88MHz VCXO is used to provide the timing reference for TU REJUSTIFIER ASICs (on the card itself and on other line and STM-1 tributary cards), for SUPERMAPPING ASICs (for 2Mbit/s tributary cards) and for GROOMER and SWITCH ASICs.

The outgoing 2048Hz timing reference is extracted by a 2048Hz VCXO, controlled by the TIMEX.

The internal clock source is a 32MHz oscillator.

F Interface Management

The microprocessor (**Block 7**) is connected, through the back panel, to the F interface for the connection to the Local Controller. Through the DCC channels a connection to a remote equipment is also possible.

Power Supply

On the Common Parts Sub-Unit is fitted a DC/DC converter (**Block 9**), which provides the supply voltages to all the components on the card itself and on the line and tributary sub-units.

The DC/DC converter receives a doubled –48V supply voltage and gives back –5V, +3V, +5V and +15V supply voltages.

The Common Parts Sub-Unit receives also a service voltage, in order to ensure the operation of front panel LEDs even in absence of main supply voltage.

Alarm Indication (Front Panel LEDs)

The Common Parts Sub-Unit is equipped with the following LEDs:

- ◆ Δ **red LED**: lights on when an internal fault is detected on the MOST;
- ◆ **CONF green LED**: lights on when the unit is configured;
- ◆ **VS green LED**: lights on to indicate the presence of a service voltage;
- ◆ **URG red LED**: lights on when an urgent alarm is detected;
- ◆ **NURG red LED**: lights on when a not-urgent alarm is detected;
- ◆ **INT red LED**: lights on when an internal alarm is detected;
- ◆ **EXT red LED**: lights on when an external alarm is detected;
- ◆ **IND yellow LED**: lights on when an indication alarm is detected;
- ◆ **ABN yellow LED**: lights on when an abnormal operation is detected;
- ◆ **MEM yellow LED**: lights on after an alarm acknowledgement operation.

The **ABN** (Abnormal) LED lights-on when:

- ◆ *the optical protection device is disabled;*
- ◆ *an internal loopback for test is activated;*

The **MEM** LED can also be enabled by a Local Controller action.

Technical Characteristic

Microprocessor and Memories

<i>Microprocessor:</i>	Motorola 68360
<i>Data Memory:</i>	1 x 4Mbyte DRAM
<i>Bootstrap Memory:</i>	1 x 512kbyte EPROM
<i>Program Memory:</i>	1 x 2Mbyte FLASH
<i>Inventory Memory:</i>	1 x 128kbyte EEPROM
<i>Configuration Memory:</i>	1 x 512kbyte FLASH
<i>Quality Inventory Memory:</i>	1 x 128kbyte SRAM

PAGE INTENTIONALLY LEFT BLANK