

1x140Mbit/s / STM-1 G.703 Tributary Unit

131–9310/11

General Information

The unit operates as STM-1 or 140Mbit/s tributary with processing at VC-12 Virtual Container level for one channel.

The SDH or the PDH standard is accepted independently by the section.

All the signal processing operations are basically performed by the E4 T, TUREJ and CMIX ASICs.

The unit also carries out diagnosis of the switching matrix circuits by inserting and verifying check bytes into the internal frame.

The unit supervision functions are managed by a microcontroller which communicates with the central controller of the equipment by means of the Control Bus.

The power supply of the unit is realized by an on-board DC/DC converter which provides the proper voltages to the internal unit circuits.

Composition

The unit is made up of one printed circuit board where are placed the circuits for the tributary channel, the on-board power supply and the microprocessor with the memories.

The physical structure of the unit and the position of the circuits on it is shown in Fig. 5.11–1.

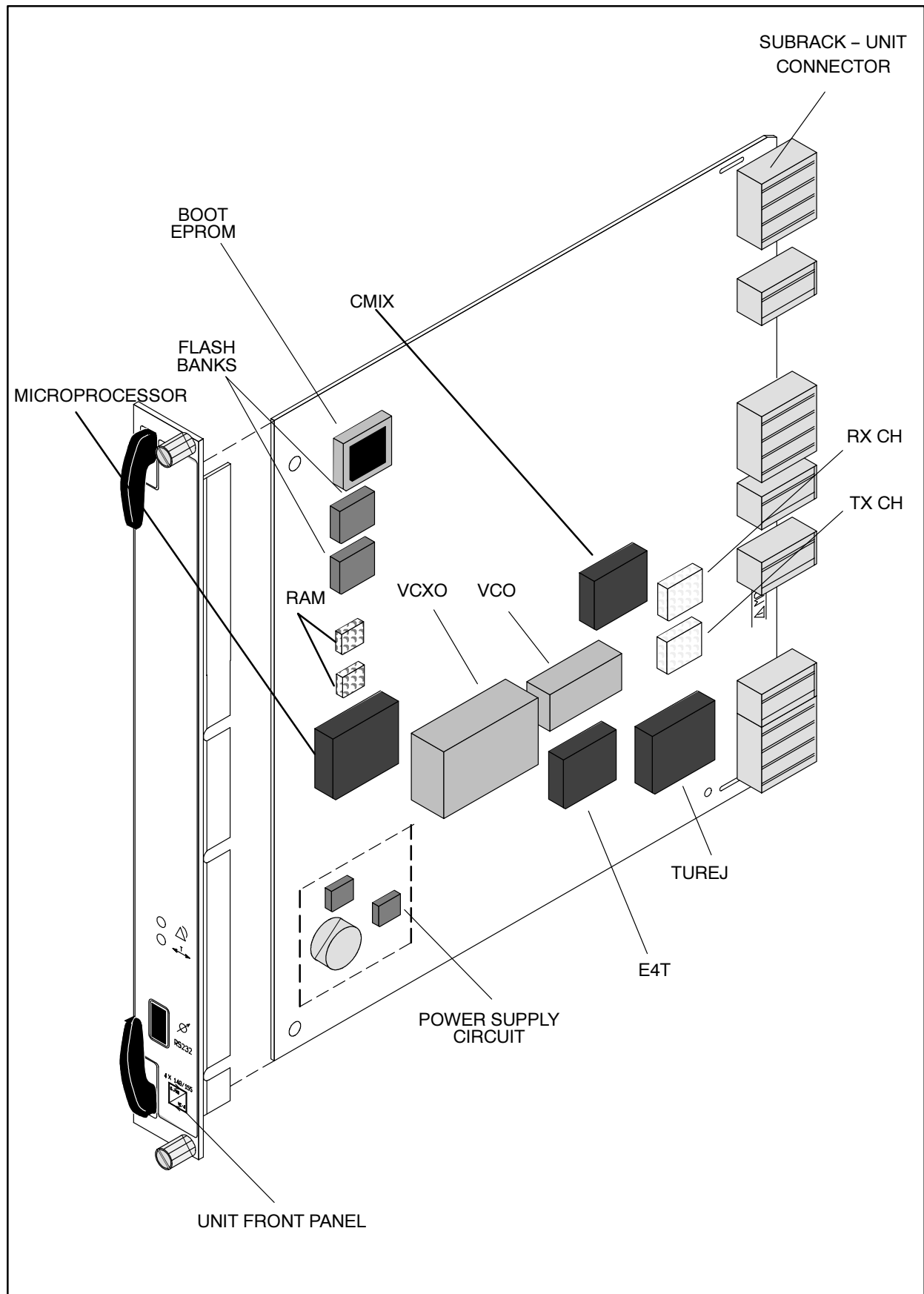


Fig. 5.11-1 1xSTM-1/140Mbit/s Tributary Unit physical structure

Functional Description

Summary

In the following the function supported by each tributary circuit section are listed:

Transmit Side

- ◆ *reception of one STM-1 stream from the Switching Matrix Circuits (divided into four 38.88 Mbit/s sub-streams), a 38.88MHz timing signal and a synchronization pulse signal*

If the incoming signal is structured according to the PDH standard:

- ◆ *extraction the 139264 kbit/s stream inserted in the proprietary STM-1 stream and its transmission to the sub-rack connector as required by the ITU-T G.703 specification*

If the incoming signal is structured according to the SDH standard:

- ◆ *extraction the VC-12, VC-3 and VC-4 inserted in the proprietary STM-1 stream, generation of a new SOH according to the information in the OH bus and transmission of the obtained STM-1 stream to the sub-rack connector*

Receive Side

- ◆ *reception of one 139264 or 155520kbit/s stream and automatic attenuation recover*
- ◆ *conversion of the signal from CMI to NRZ and insertion into the internal proprietary STM-1 frame*
- ◆ *sending the proprietary STM-1 stream (divided into four 38.88 Mbit/s sub-streams) to the Switching Matrix Circuits using the timing signal provided by the Switching Matrix circuits themselves*
- ◆ *management of the information contained in the SOH received over the OH bus from the Central Controller of the Equipment*

Common Function

- ◆ *interfacing the Central Controller of the equipment by means of the Control Bus*
- ◆ *power feeding of the unit by means of on-board DC/DC converter circuit*
- ◆ *loop-back management*

Receive Side

This description refers to one tributary channel and to the block diagram in Fig. 5.11-1.

The CMI INPUT INTERFACE block receives a 139264 or 155520kbit/s (1 Vpp/75Ω) signal structured in conformance with G.703 specifications and CMI coded. It first matches the impedance and recovers any attenuation caused by the interconnection cables in the range from 0 to 12dB at 69632 or 77760kHz.

The received stream is issued to CMIX ASIC, which deviates part of it to CLOCK EXTRACTION block where it is processed to obtain a 139264 or 155520kHz clock signal.

The extracted clock signal is used in the CMIX ASIC to sample the stream received from the CMI INPUT INTERFACE, check that the structure of the received signal is correct and perform CMI to NRZ code conversion.

The loss of incoming signal alarm is detected by checking whether the extracted clock signal is present. This is performed in the CMI INPUT INTERFACE.

The NRZ 140 or 155Mbit/s signal is then divided into four 34816 or 38880kbit/s streams and sent to E4 T ASIC.

The E4 T ASIC allocates the 4 streams received to a C-4 container using a floating multiplexing structure plus POH bytes:

- ◆ *J1, B3, C2, G1* (for end-to-end communications);
- ◆ *H4, F2, F3* (specific for type of payload and user channels);
- ◆ *K3* (for APS management);
- ◆ *N1* (for Tandem Connection monitoring);

which, together with the C4, form a VC-4.

The AUG pointer and SOH bytes containing diagnostic information and the APS protocol (K1 and K2) complete the structure of an STM-1 frame generated in the E4 T ASIC. The content of the diagnostics message in the SOH bytes is as follows:

- ◆ *column 1 line 1* parity bit on channel number
- ◆ *column 1 line 2* subrack ID number
- ◆ *column 1 line 3* card and channel number

The above information is sent to the E4 T ASIC by the Central Controller circuits of the equipment through the OH-bus.

The TUREJ manages the STM-1 until the VC-12 level.

Another function implemented in the E4 T ASIC is generation of a $2^{23}-1$ pseudo-random sequence. This sequence is generated by the polynomial

$1+X^{18}+X^{23}$ and is used during the test function, when the incoming stream is replaced by this sequence.

The sequence is monitored on the receive side by a self-tuning tester. The STM-1 stream so formed is divided into 4 38.88Mbit/s sub-streams and distributed in parallel to the tributary-matrix units.

Distribution is timed using the synchronism signal issued by the Switching Matrix circuits of the equipment.

A 128kHz signal locked onto signal CK extracted from the 140Mbit/s stream received in input is also sent to the Switching Matrix circuits of the equipment.

Transmit Side

The unit receives the traffic data from two (A and B) Switching Matrix circuits of the equipment which act as master and slave units

Each Switching Matrix sends to the Tributary Unit one STM-1 equivalent stream with its associated clock and synch. references.

The proprietary STM-1 signal is transmitted on four wires in half-bytes (nibble) with a bit rate of 38.88Mbit/s.

A 102.5ns/62.5Hz multiframe synchronisation signal and a 38.88MHz clock signal are paired to the STM-1 stream.

The two (A and B) STM-1 streams are sent to the TUREJ ASIC which selects one of them according to the diagnostics information written into the proprietary SOH bytes (column 1, lines 1, 2 and 3).

Furthermore in the TUREJ ASIC, the POH bytes are extracted under control of the selector and processed as follows:

- ◆ *bytes J1, F2, F3, K3, N1 are sent to the OH-bus*
- ◆ *bytes B3, C2, G1, H4, are processed locally as indicated in G.708 specifications*
- ◆ *the bytes containing the C-4 pointer*
- ◆ *the five X bytes that form part of the multiplexing structure as per G.708, and are used to perform a majority calculation to establish positive justification of the Z byte where necessary*

The data bytes are then allocated to a DPRAM memory in the TUREJ ASIC and read using a clock signal that takes account of the transmission rate of the 140 or 155Mbit/s NRZ stream.

This stream is sent to CMIX ASIC, which performs NRZ to CMI code conversion and sends the resulting signal to the CMI OUTPUT INTERFACE where it is level and impedance matched according to G.703 requirements.

Common Function

Unit Controller

The unit is equipped with an on-board microcontroller 8 bit 16MHz with two program flash banks; the memory duplication allows to download new application softwares while the unit is in service with no traffic affecting.

The microcontroller manages the control bus for the communication to the central controller of the equipment and a serial line to the unit front panel connector for monitoring purposes.

The microcontroller has also a serial connection to the switching matrix circuit of the equipment for carrying out the 'fast protection' function.

This function allows the switching matrix circuit to transmit to the optical line the unit configuration according to the protection scheme in a faster way, without involving the central controller which would need a longer time.

The unit also contains the INVENTORY block where the unit inventory data (i.e. identification number, unit hardware code, installed software code) are stored and made available to the Central Controller of the Equipment.

DC/DC Converter

The Unit is provided with a on-board DC/DC converter. This converter accepts two incoming battery voltages ($-48\text{V} \pm 20\%$ to $-60\text{V} \pm 20\%$) and provides +5V, +3.3V, +9V, -9V and -5.2V supply voltages to all the components on the unit.

Power supply block also generates the unit alarm related to the supply voltages. Malfunctions, if any, of the power supply voltages, determining the failure of at least one of the secondary supply voltages, are signalled by the lighting up of the unit alarm red LED.

Loop-backs

The unit can perform two different kind of loop-backs:

- ◆ *Front-end*
- ◆ *Back-end*

When the front-end end loop-back is performed, the incoming data from the CMI INPUT INTERFACE are sent to the CMI ASIC. Here the signal is processed and the loop-backed to the CMI OUTPUT INTERFACE.

When the back-end loop-back is performed, the incoming data from the switching matrix of the equipment through the E4 T ASIC is processed by the CMIX ASIC and then transmitted backwards to the E4 T ASIC.

Technical Characteristics

<i>Microprocessor</i>	1 microprocessor, Motorola 68302, 8bit, 16MHz
<i>Data memory</i>	2 x 128kbytes RAM Memory
<i>Program memory</i>	2 x 256kbytes FLASH EEPROM
<i>Bootstrap memory</i>	1 x 256kbytes EPROM Memory
<i>Inventory and setting data memory</i>	1 x 2kbytes EEPROM Memory

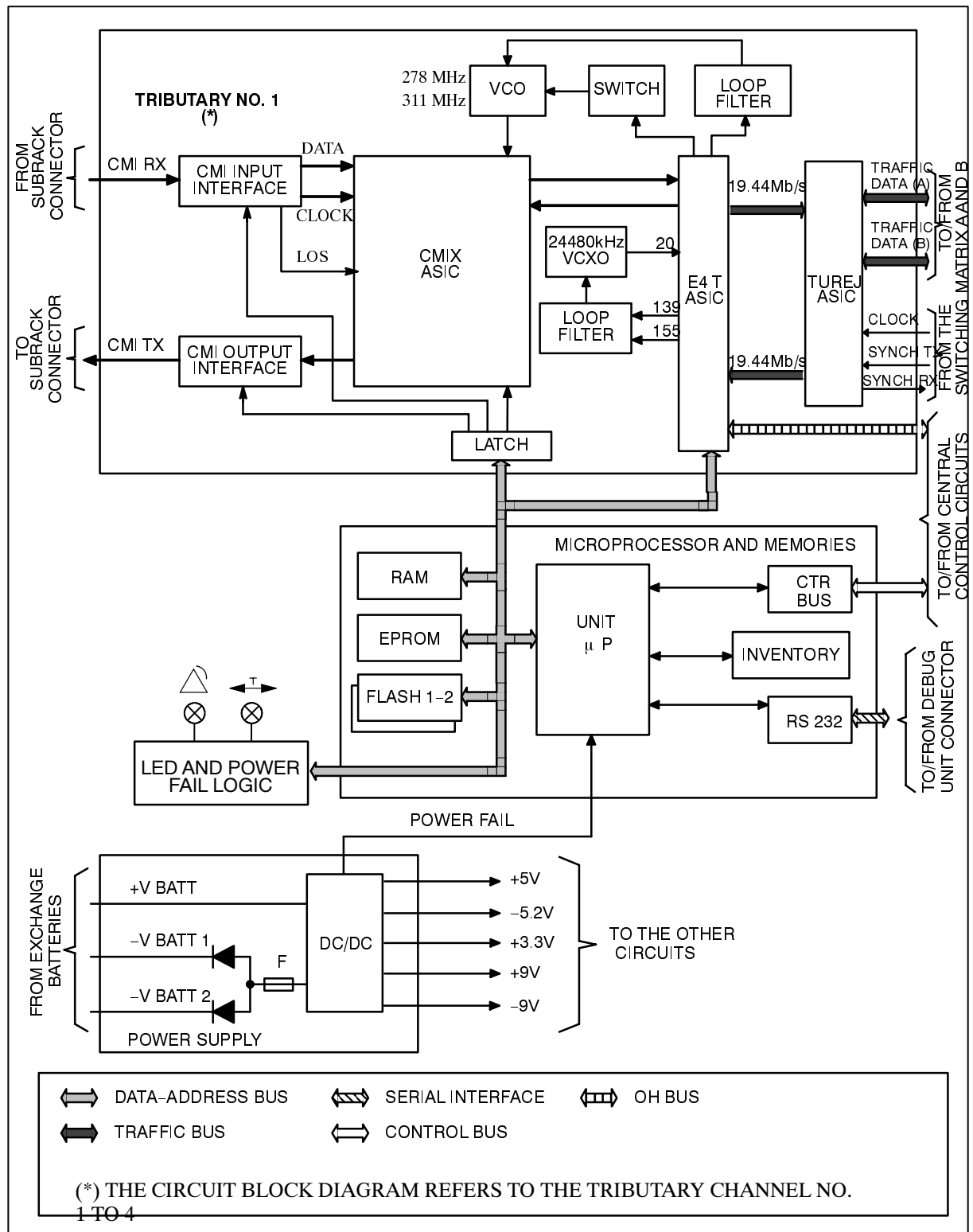


Fig. 5.11-2 1xSTM-1/140Mbit/s Tributary Unit – Block diagram