

Elkhart Lake

Module Core Library SKU1

Schematics (Hierarchical)

December 2019

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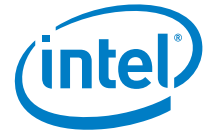
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Revision History

Date	Revision	Description
December 2019	0.7	Initial release.

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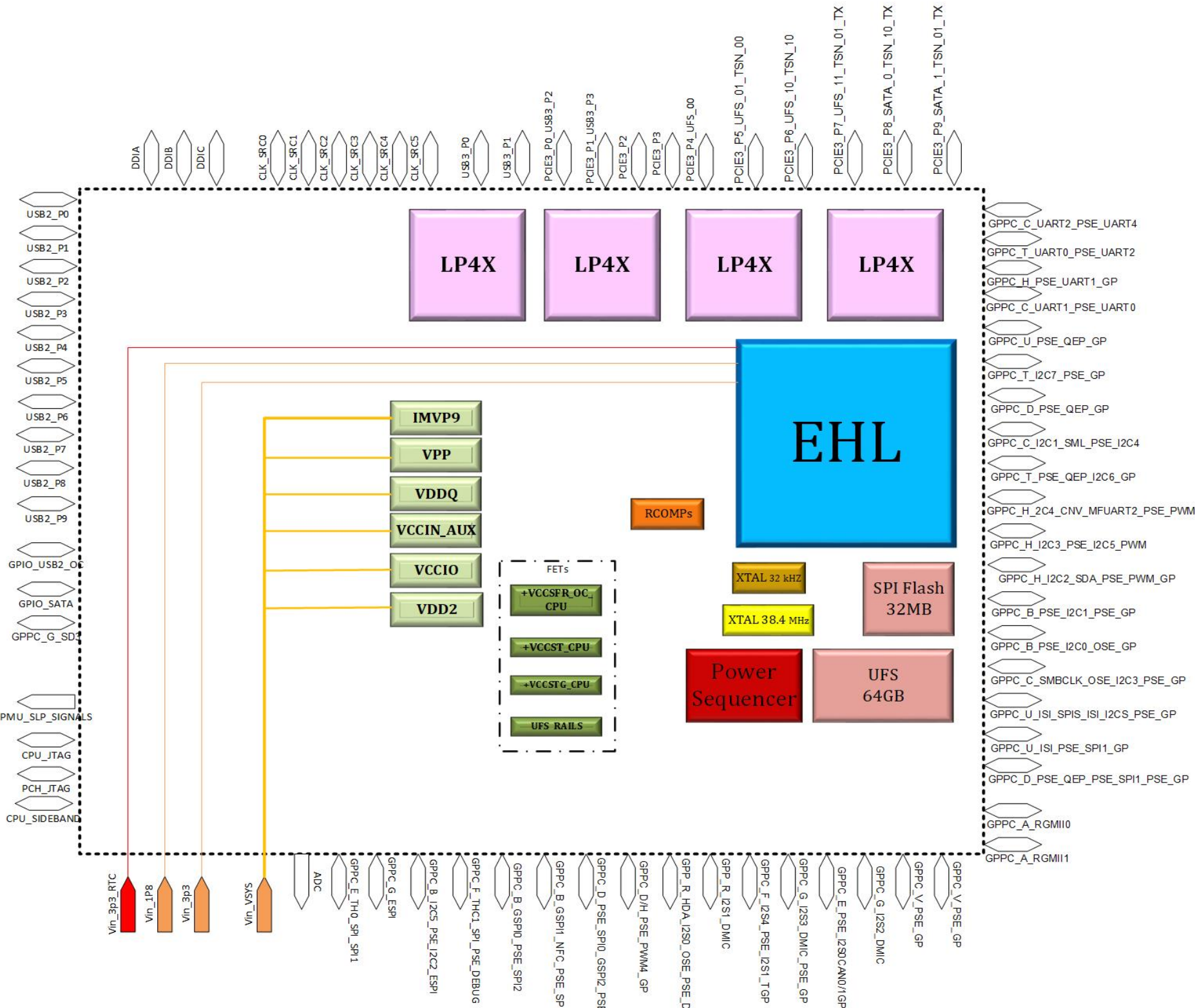
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BLOCK DIAGRAM

EHL LP4x Discrete VR
MCL SKU1

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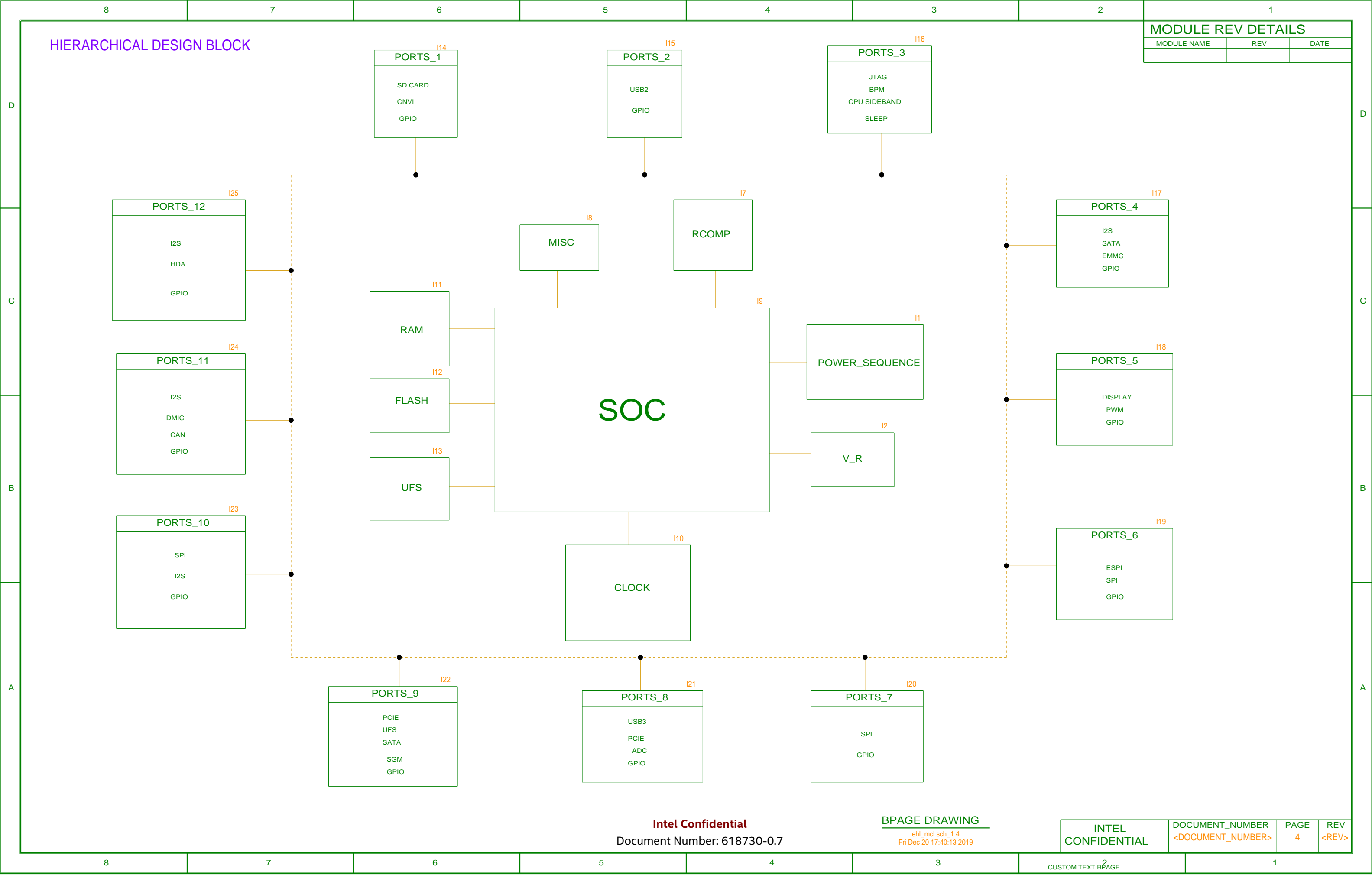
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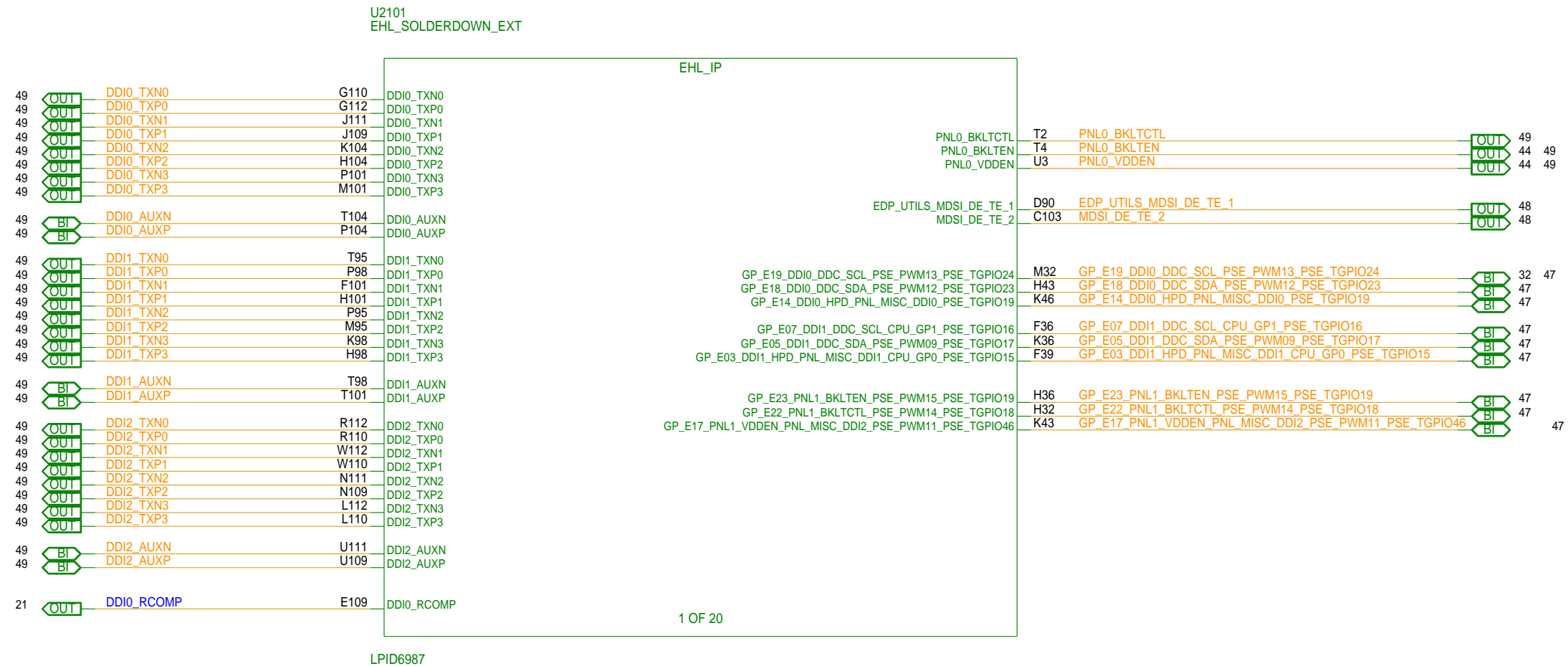
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MODULE NAME	REV	DATE

SOC - DISPLAY PORT



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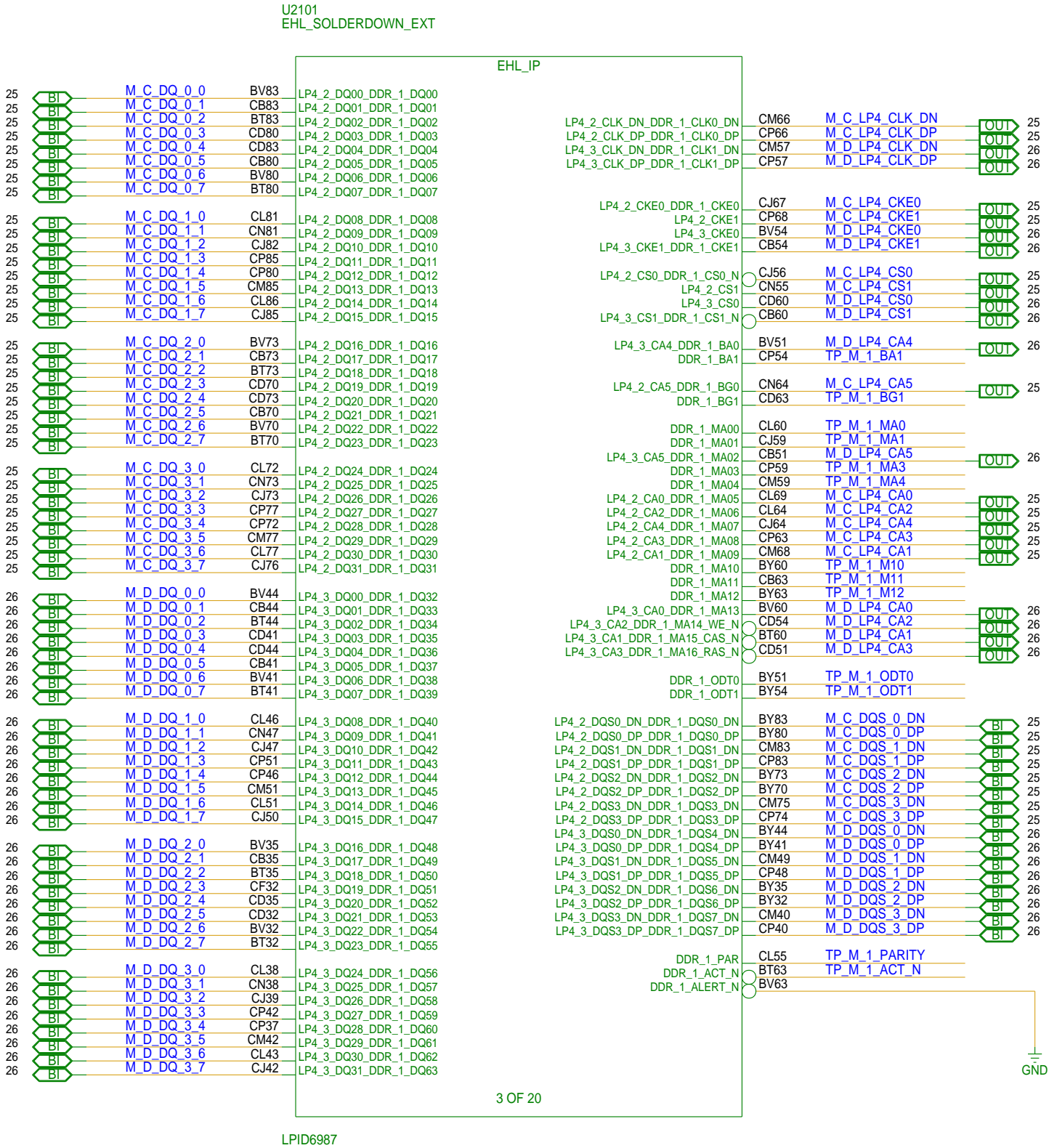
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SOC - MEMORY CHANNEL B

MODULE REV DETAILS

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MODULE NAME	REV	DATE

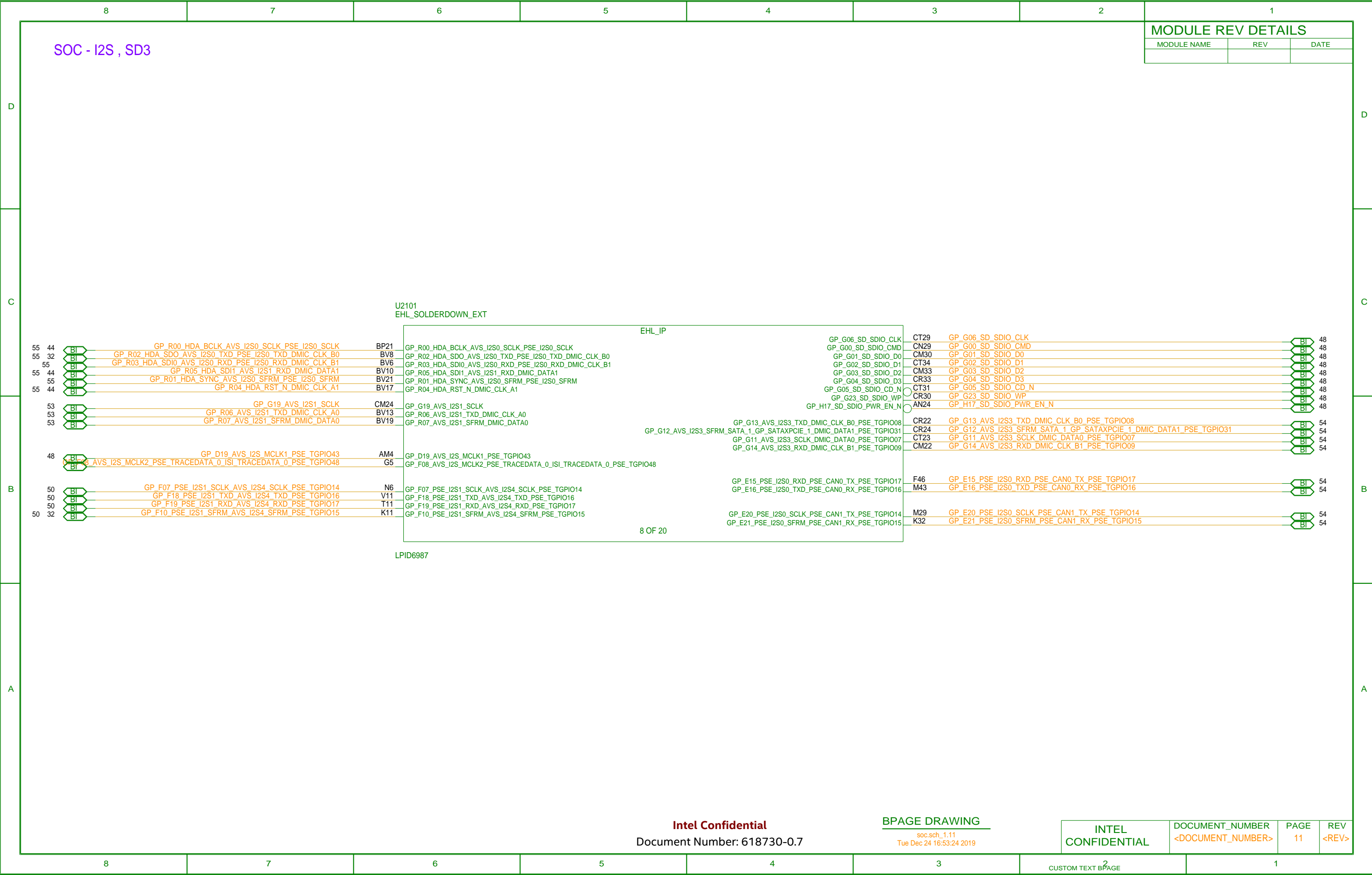


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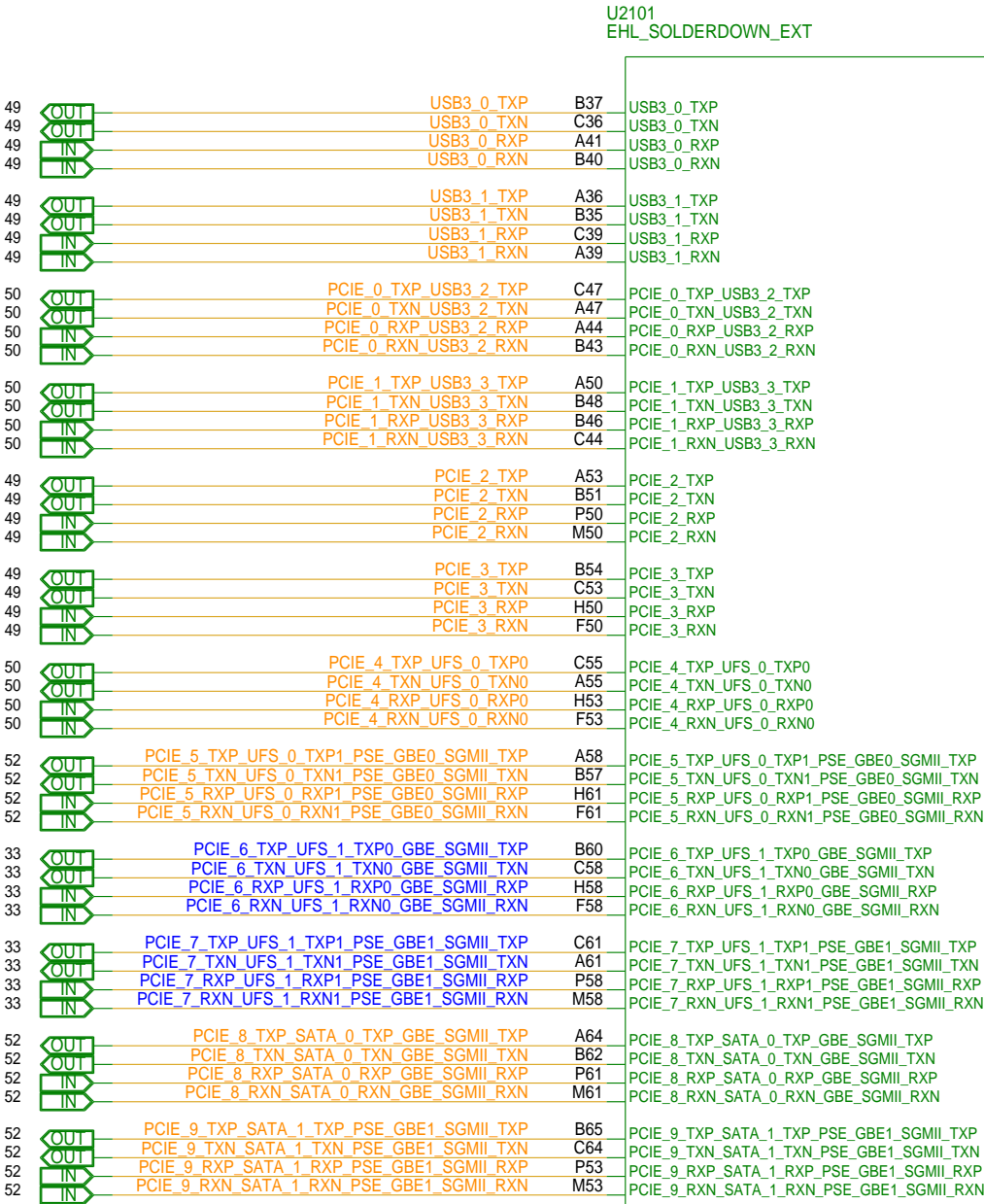
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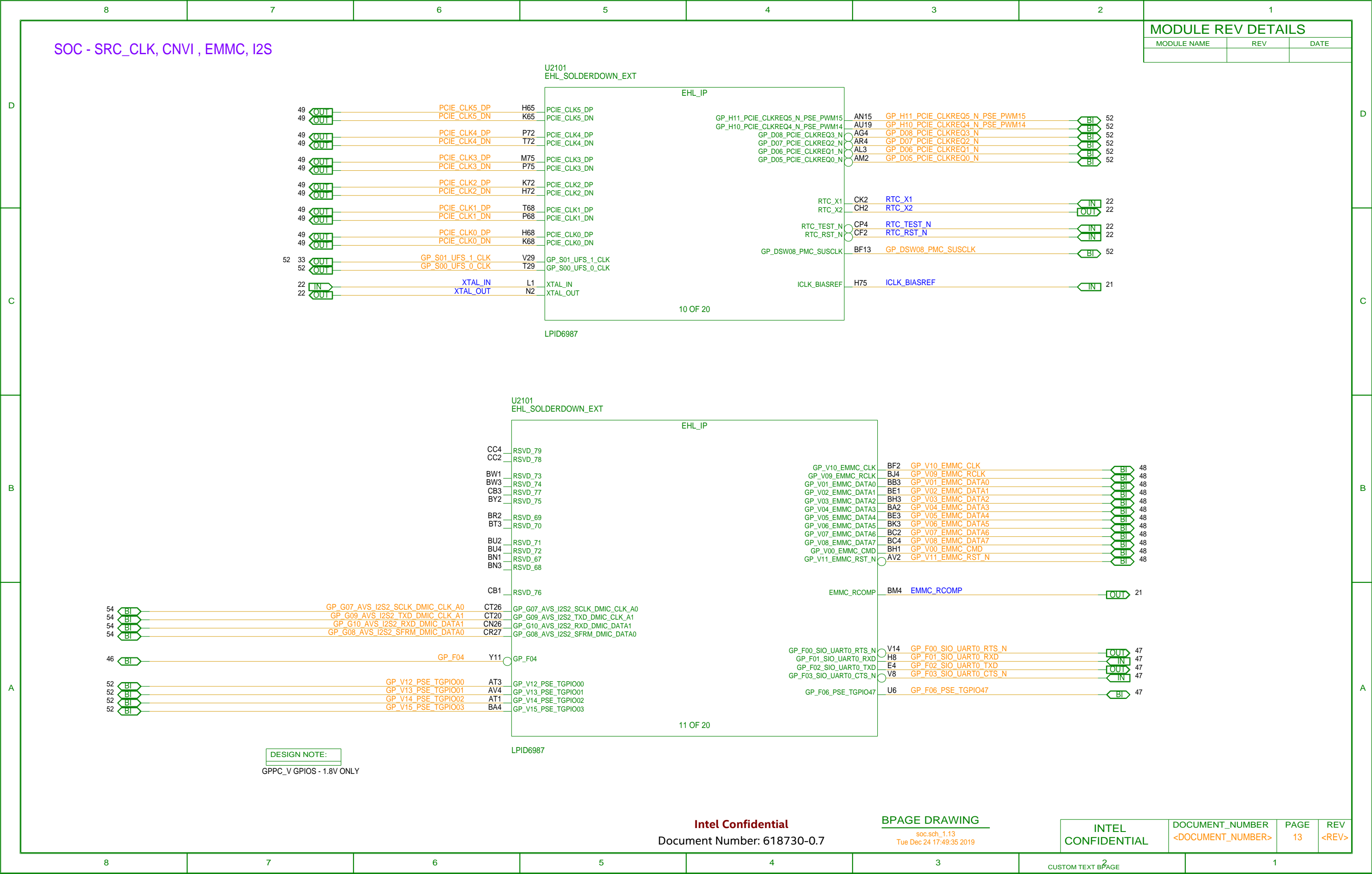
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LPID6987



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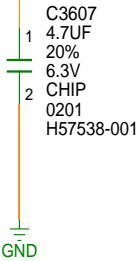
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SOC - PDBOM

MODULE REV DETAILS

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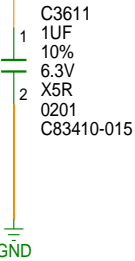
+VCCDPHY_1P24_SOC



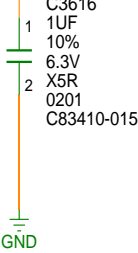
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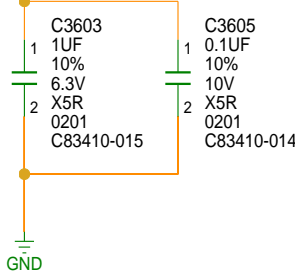
+VCC_RTC_EXT_SOC



+VCCSTG_CPU



+V3.3A_RTC

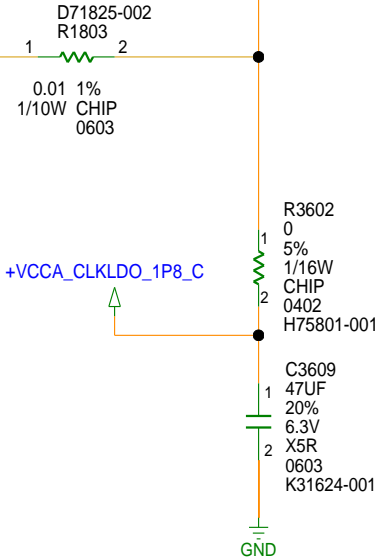


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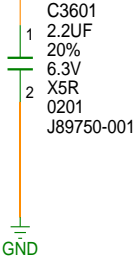
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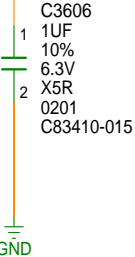
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CAD NOTE:

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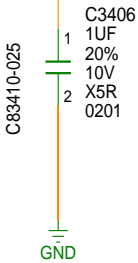
+VCCDSW_1P05_SOC



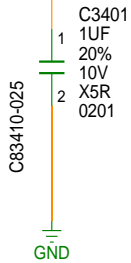
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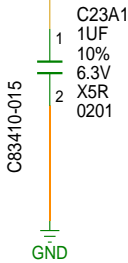
+VCCAGSH_CPU



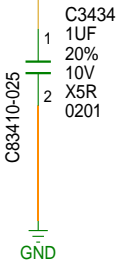
+VCCSFR_OC_CPU



+VCCST_CPU



+VCC1P05_OUT_FET_SOC



CAD NOTE:

PLACE CLOSE TO VCCSFR

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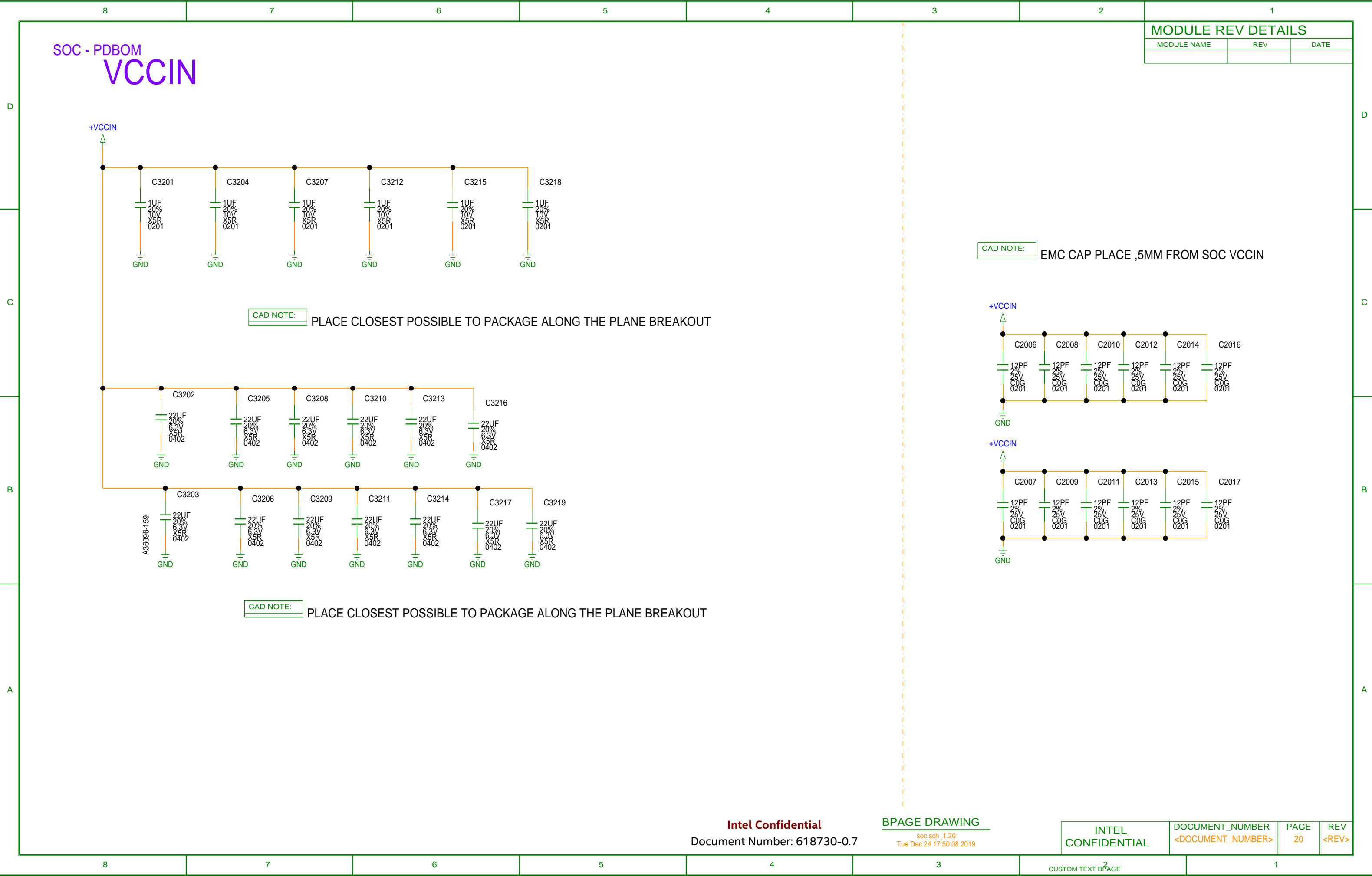
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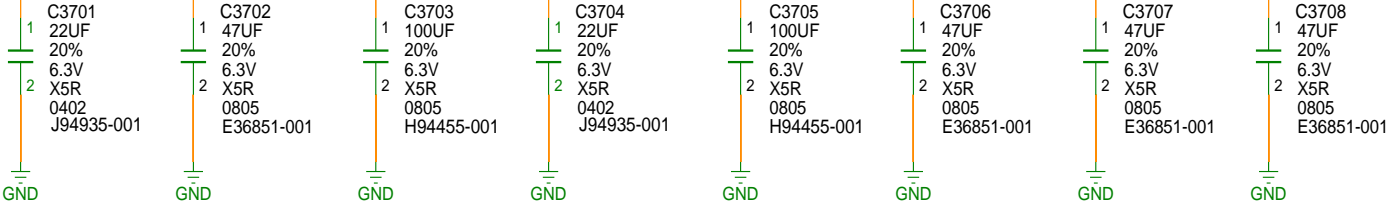


SOC - PDBOM

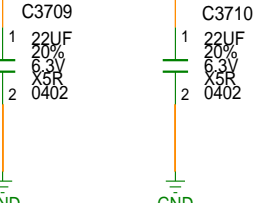
MODULE REV DETAILS

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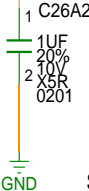
+VCCIO_CPU



CAD NOTE:

SOC BSC CAP

+VCCPRIM_FIVR_1P05_EDGE_SOC



CAD NOTE:

SOC EDGE CAP

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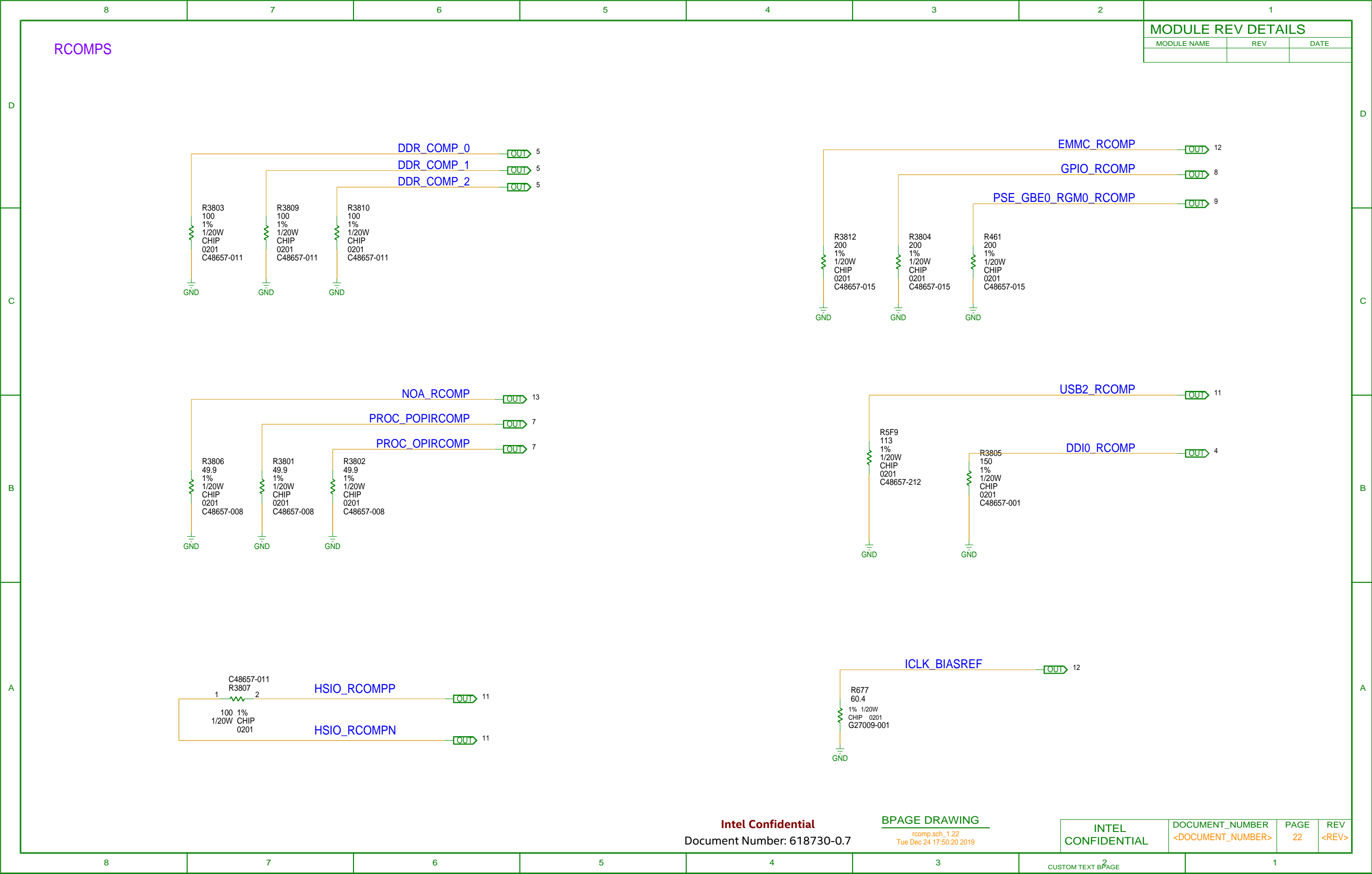
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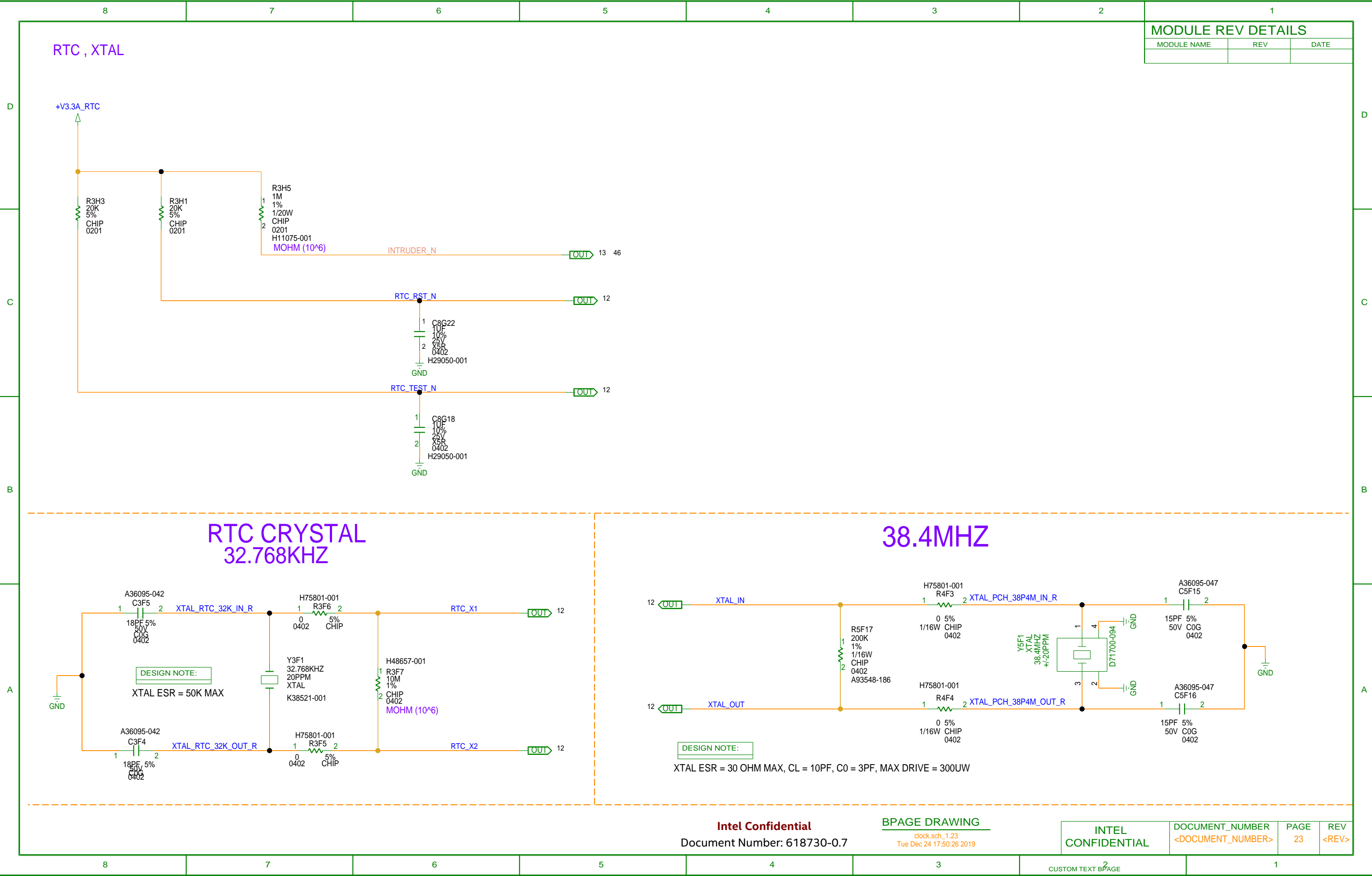
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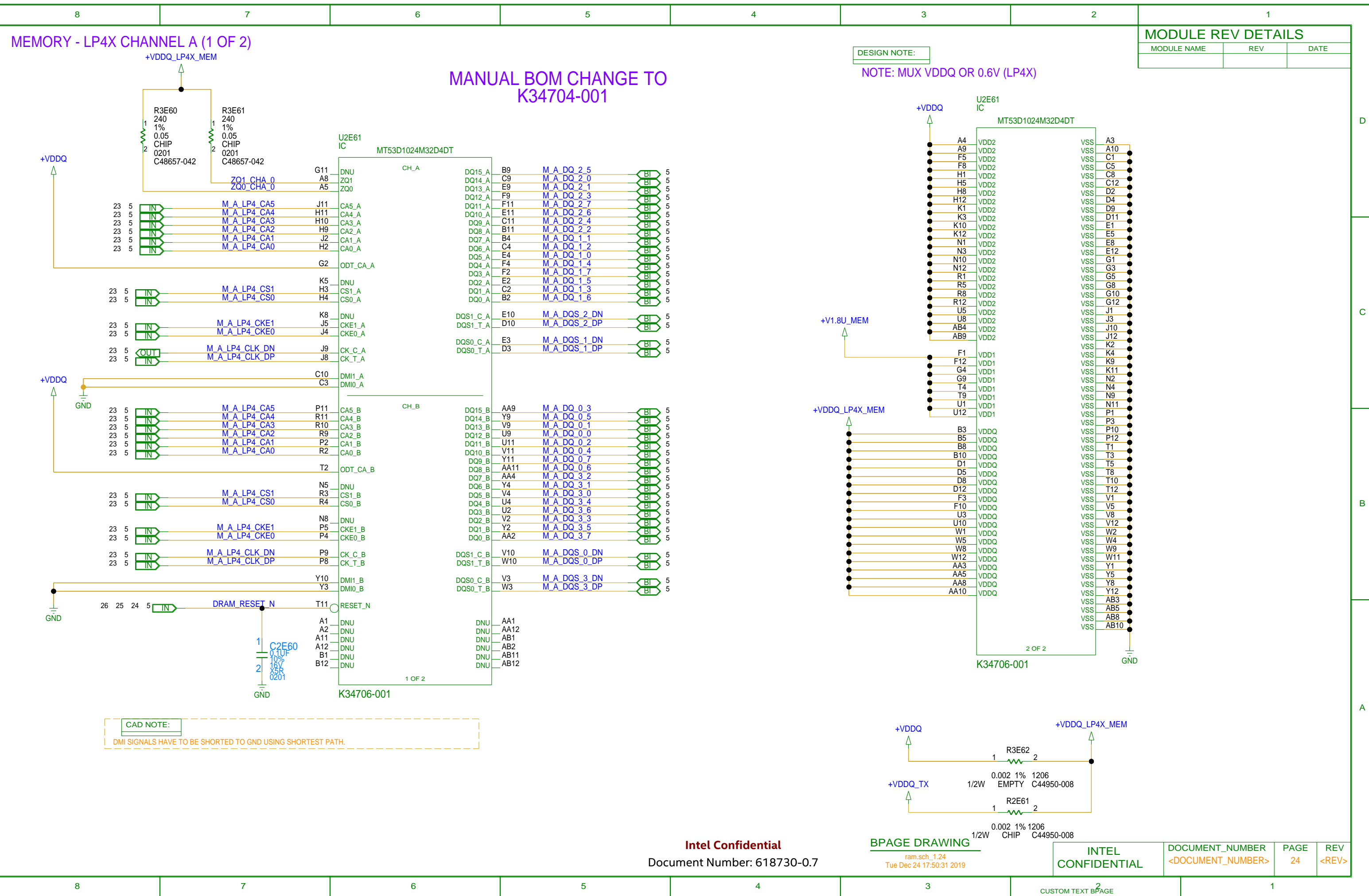
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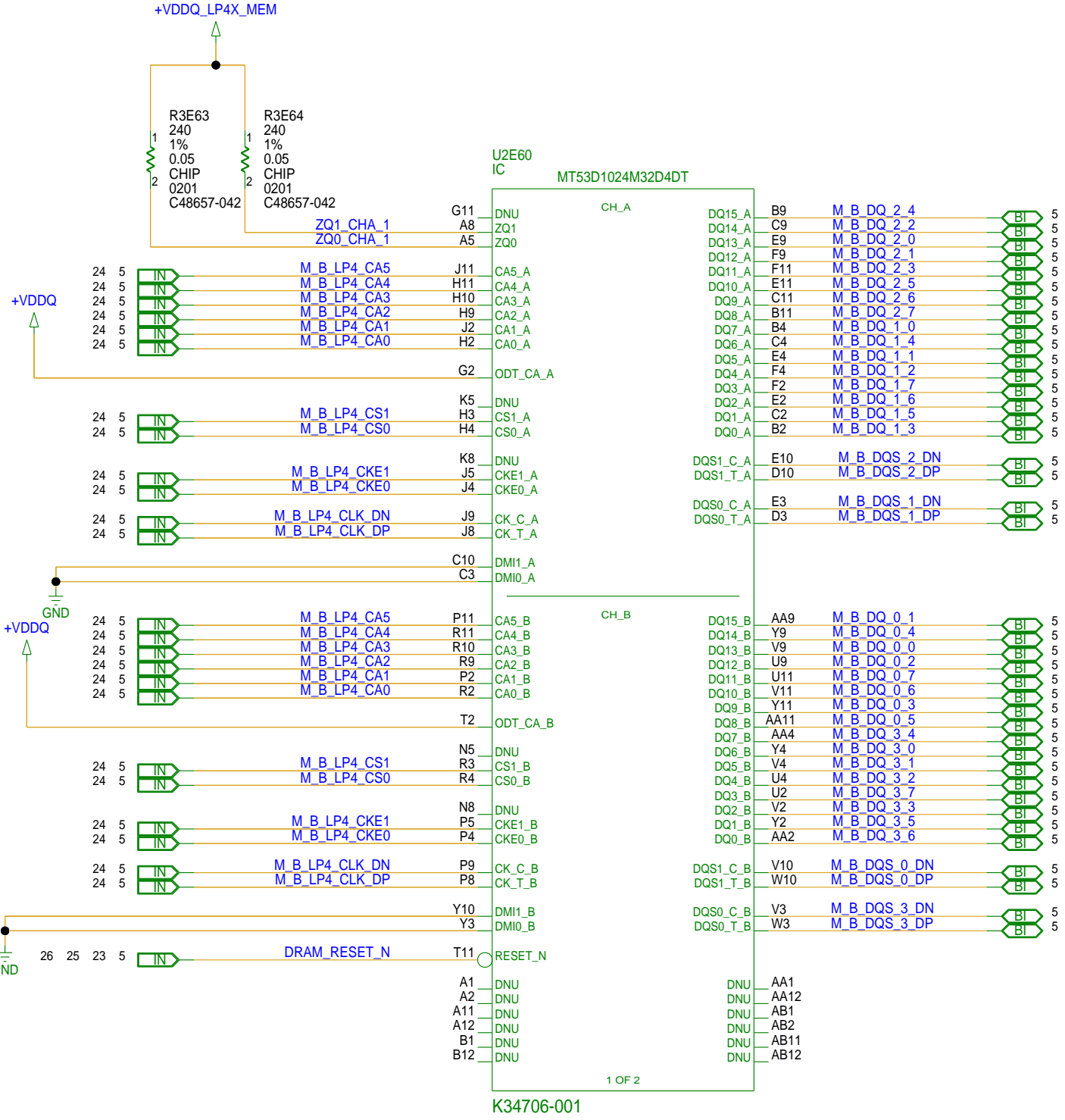
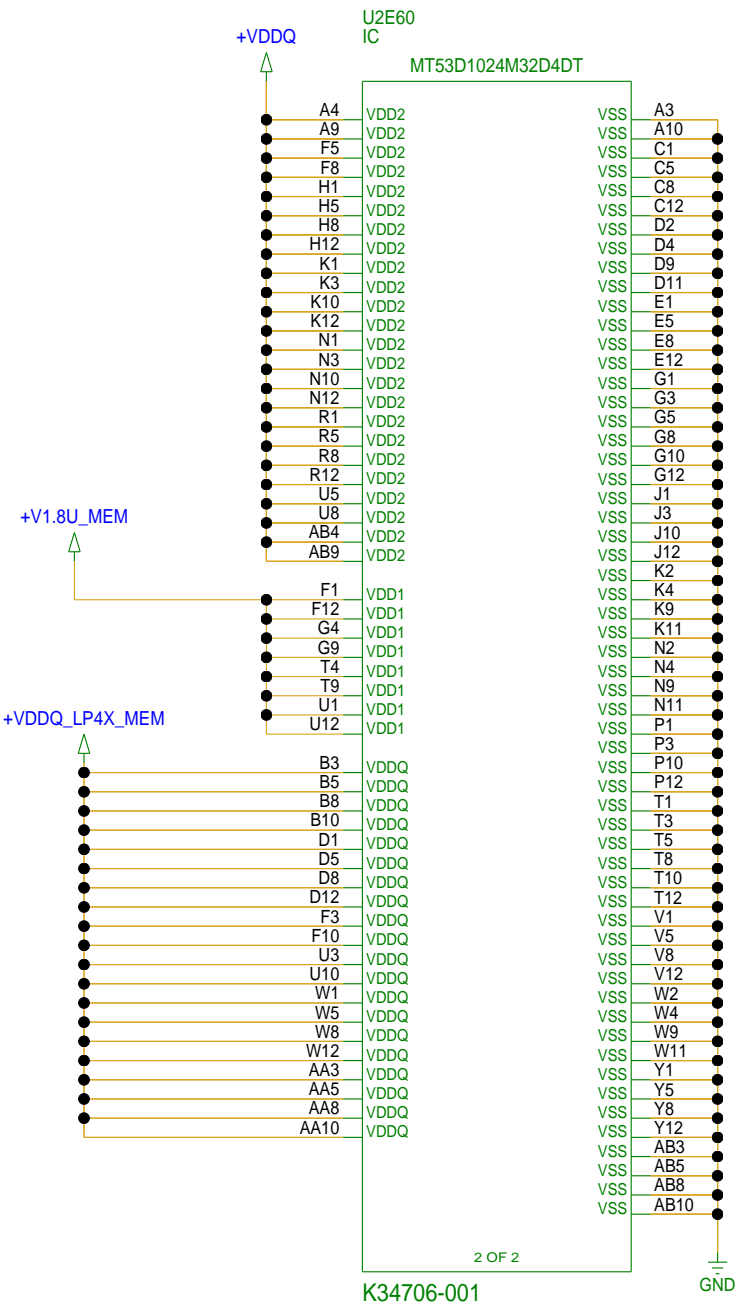
MEMORY - LP4X CHANNEL A (2 OF 2)

MODULE REV DETAILS

MODULE NAME	REV	DATE

DESIGN NOTE:

NOTE: MUX VDDQ OR 0.6V (LP4X)



CAD NOTE:

DMI SIGNALS HAVE TO BE SHORTED TO GND USING SHORTEST PATH.

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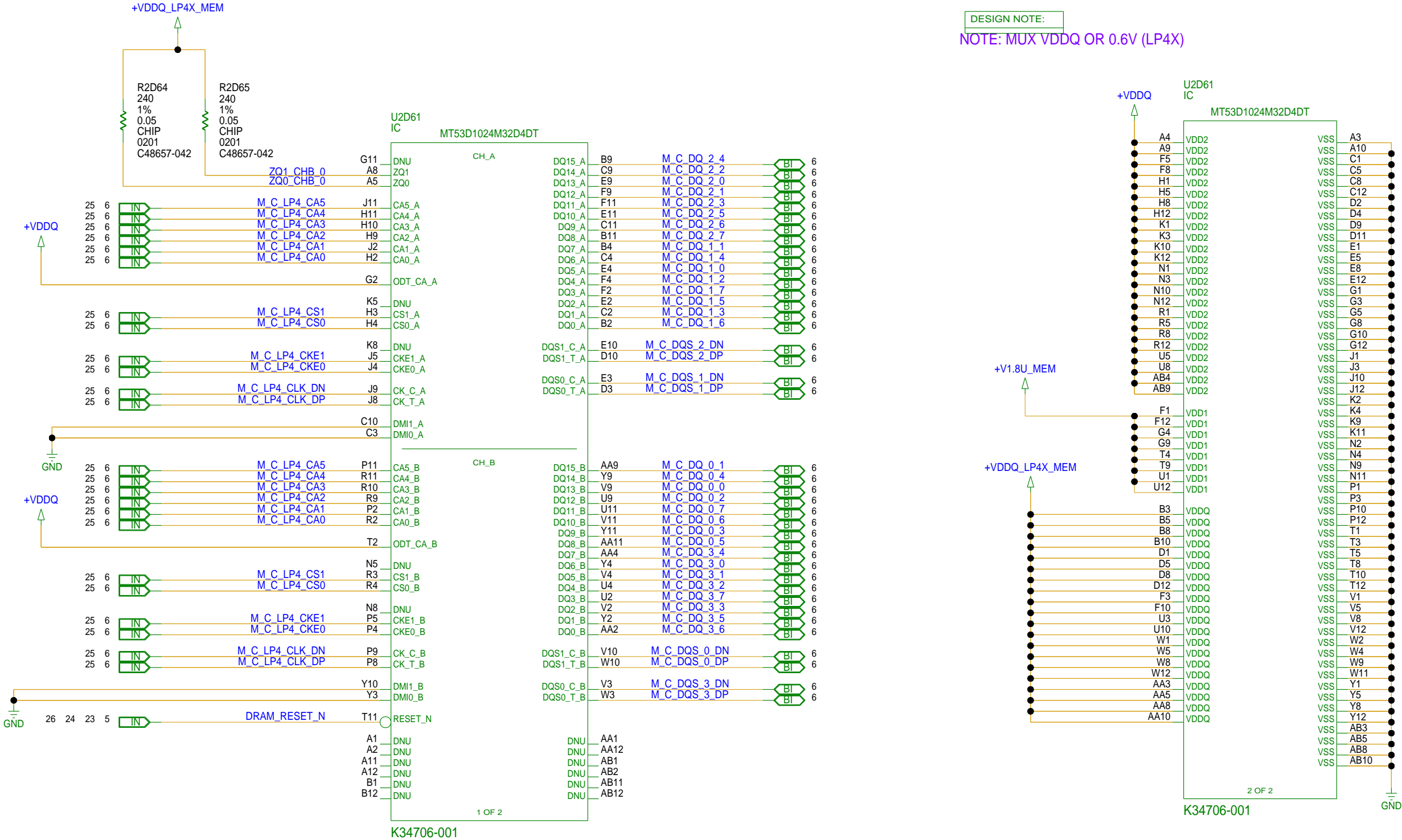
MEMORY - LP4X CHANNEL B (1 OF 2)

MODULE REV DETAILS

MODULE NAME	REV	DATE
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DESIGN NOTE:

NOTE: MUX VDDQ OR 0.6V (LP4X)



CAD NOTE:

DMI SIGNALS HAVE TO BE SHORTED TO GND USING SHORTEST PATH.

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NOTE: MUX VDDQ OR 0.6V (LP4X)

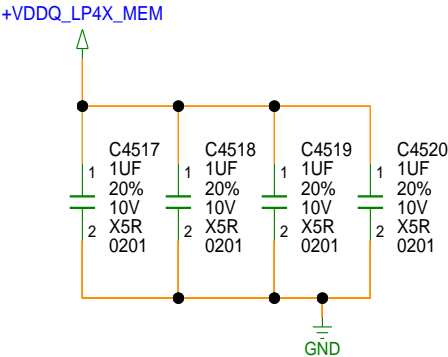
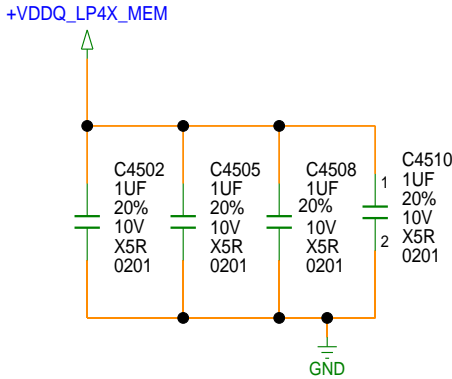


MODULE NAME	REV	DATE

MEMORY - LP4X CHANNEL A - PDBOM

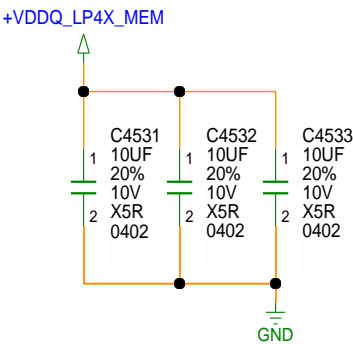
CAD NOTE:

DISTRIBUTE EVENLY, 4 FOR EACH DRAM MODULE



CAD NOTE:

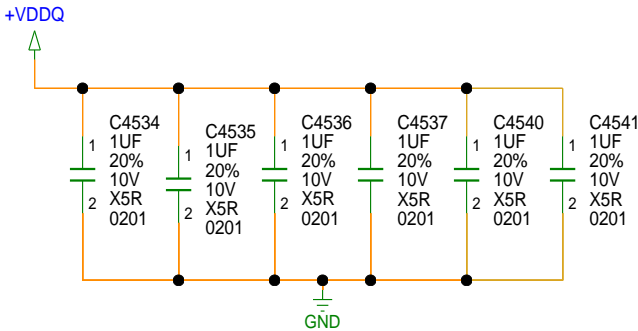
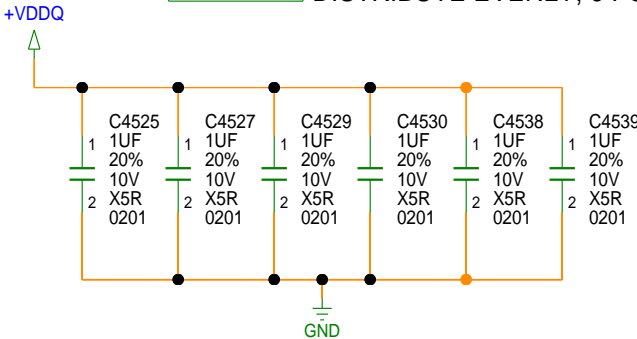
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VDDQ DECAPS

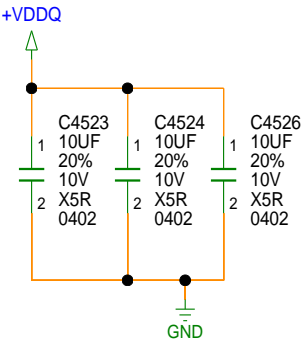
CAD NOTE:

DISTRIBUTE EVENLY, 6 FOR EACH DRAM MODULE



CAD NOTE:

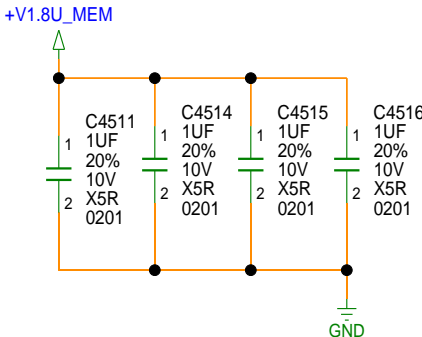
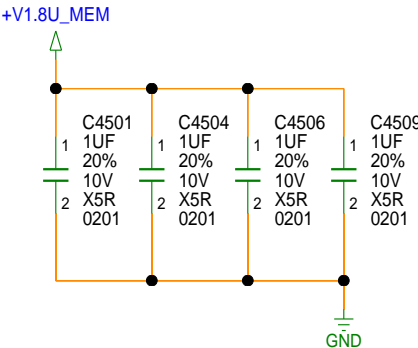
DISTRIBUTE EVENLY FOR EACH DRAM MODULES



VDD1 DECAPS

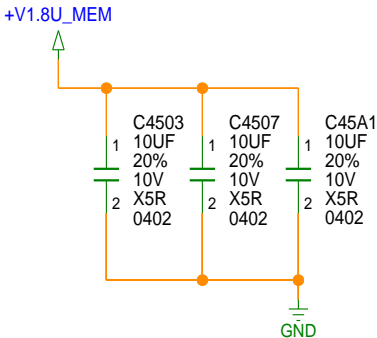
CAD NOTE:

DISTRIBUTE EVENLY, 4 FOR EACH DRAM MODULE



CAD NOTE:

DISTRIBUTE EVENLY FOR ALL LP4 MODULES



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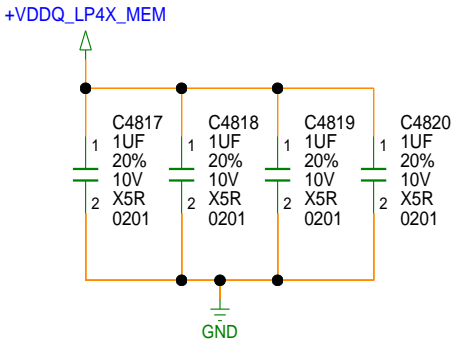
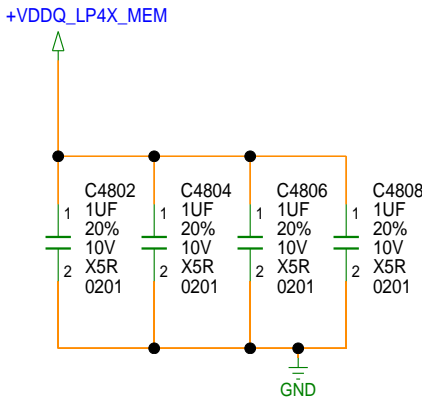
MEMORY - LP4X CHANNEL B - PDBOM

MEMORY- LPDDR4/4X CHANNEL - B - PD BOM

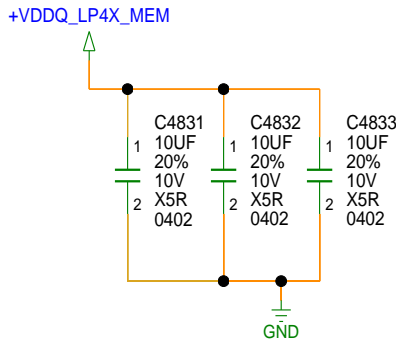
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MODULE NAME	REV	DATE

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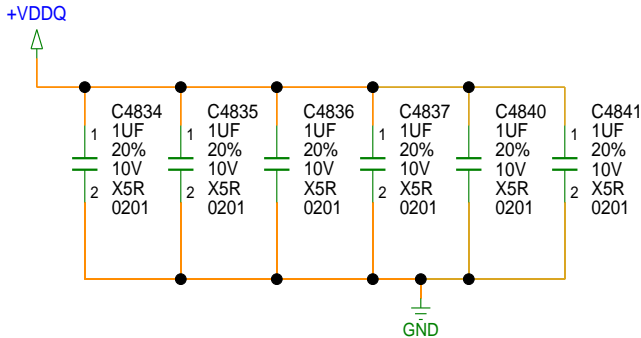
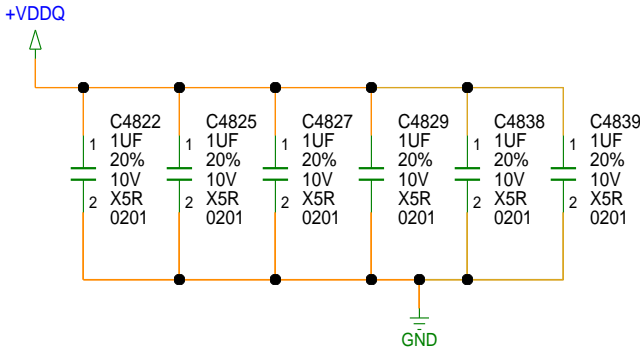


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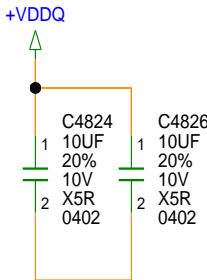


VDDQ DECAPS

CAD NOTE: DISTRIBUTE EVENLY, 6 FOR EACH DRAM MODULE

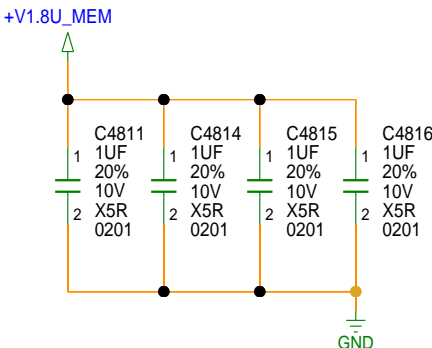
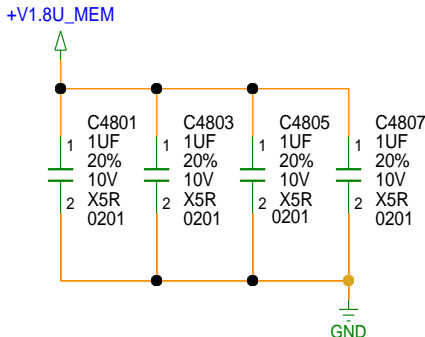


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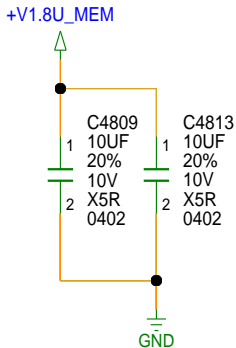


VDD1 DECAPS

CAD NOTE: DISTRIBUTE EVENLY, 4 FOR EACH DRAM MODULE



CAD NOTE: DISTRIBUTE EVENLY FOR ALL LP4 MODULES



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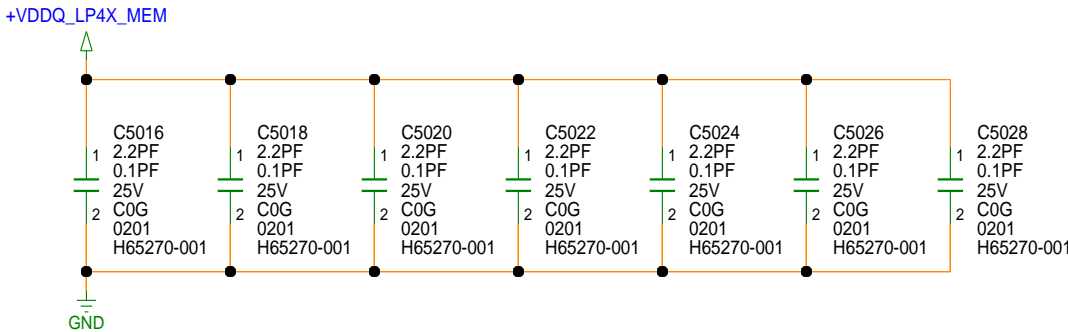
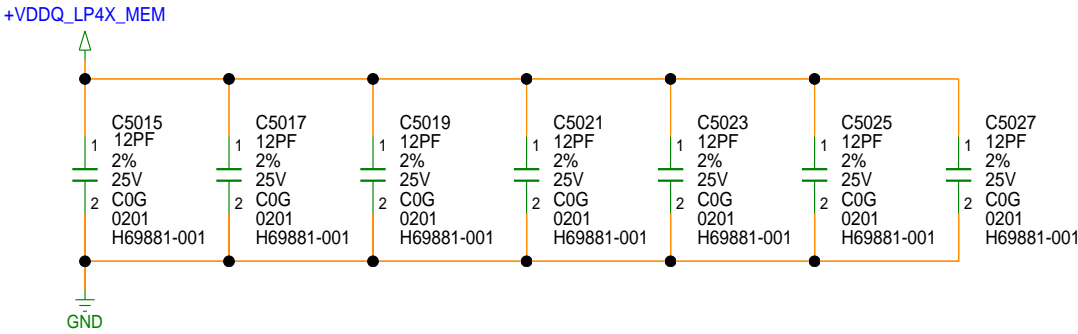
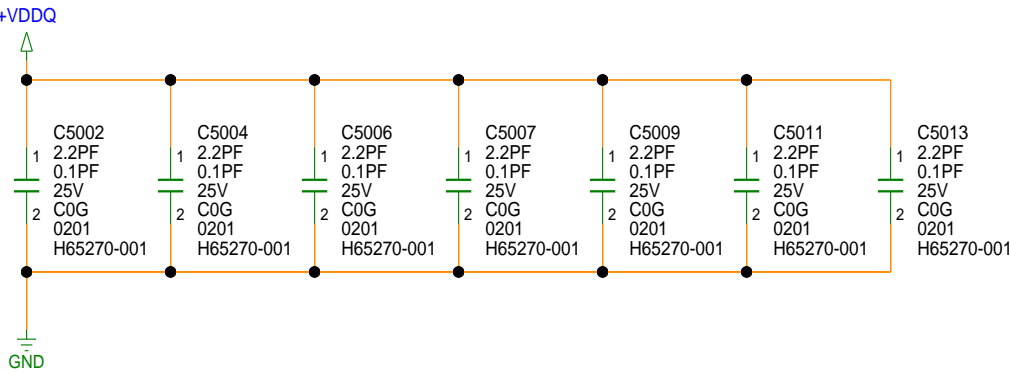
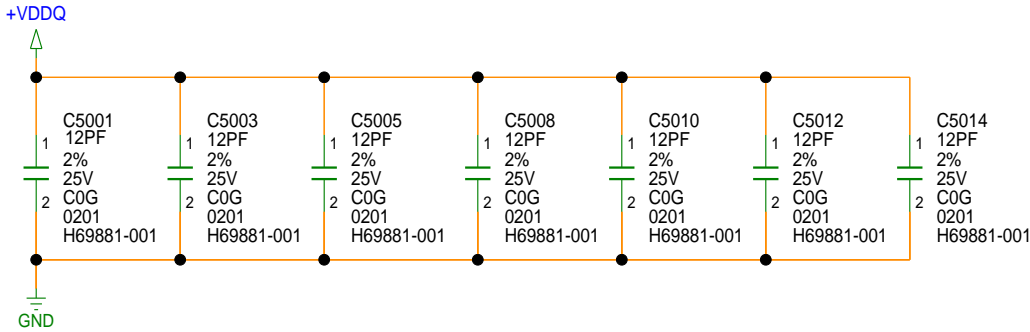
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MEMORY - LP4X PDBOM

MODULE REV DETAILS

MODULE NAME	REV	DATE



CAD NOTE:

PLACE AS PER THE GUIDELINES FROM PDG

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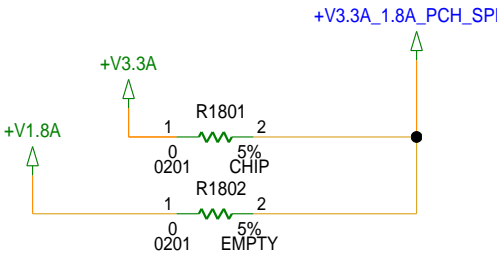
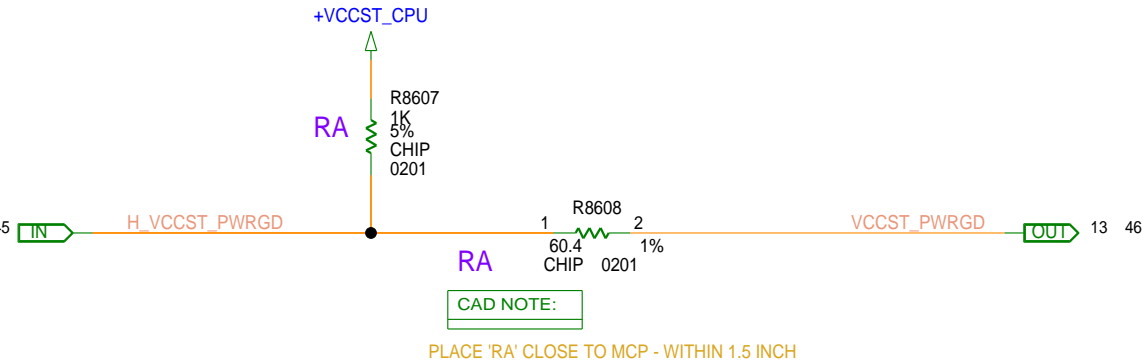
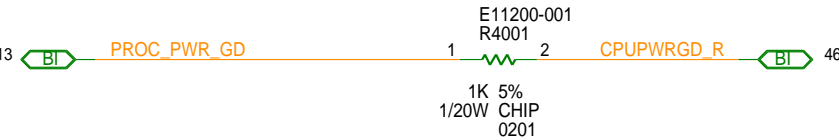
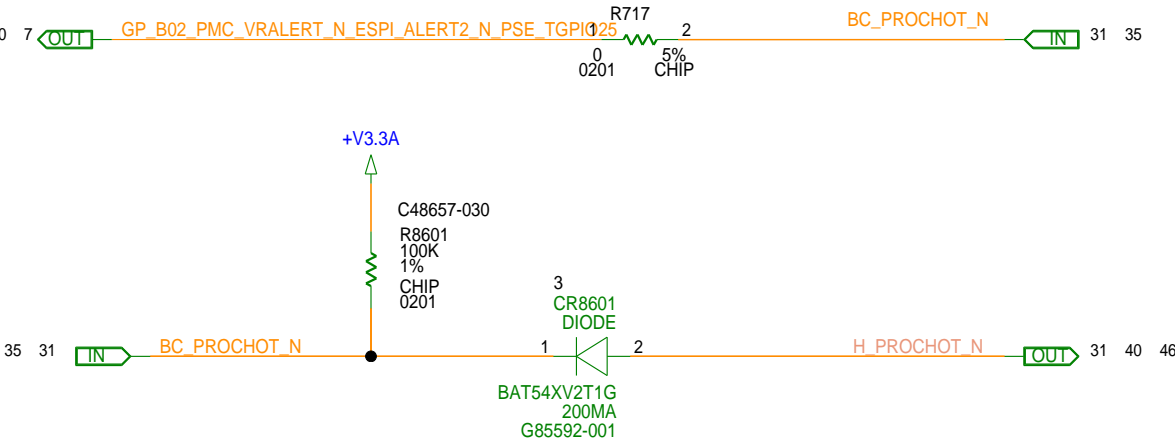
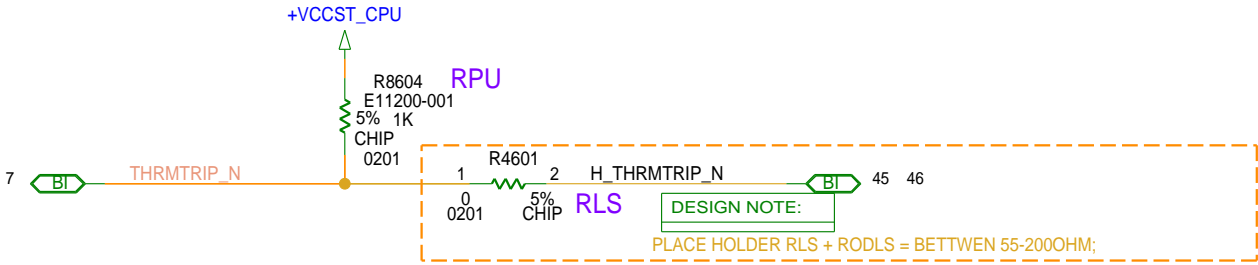
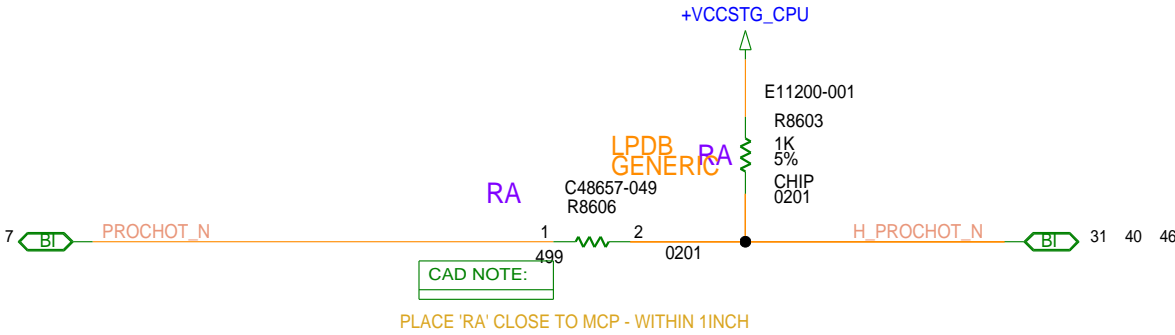


CPU SIDEBAND SIGNALS

I/O - CPU SIDEBAND SIGNALS

MODULE REV DETAILS

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MODULE NAME	REV	DATE



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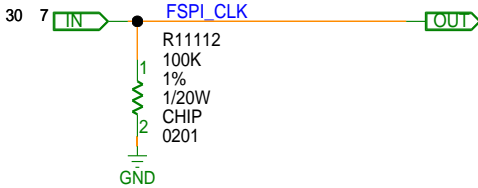
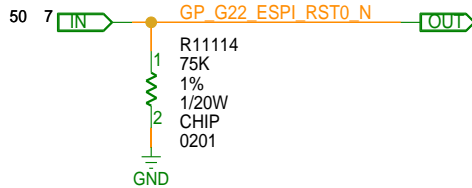
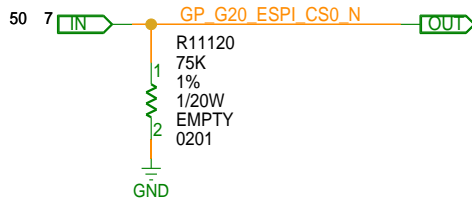
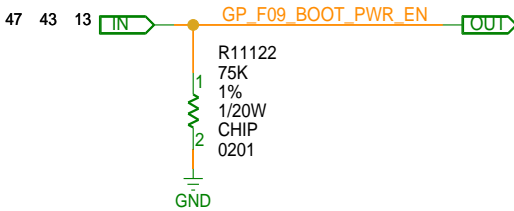
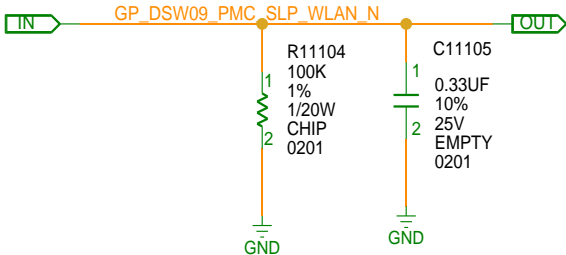
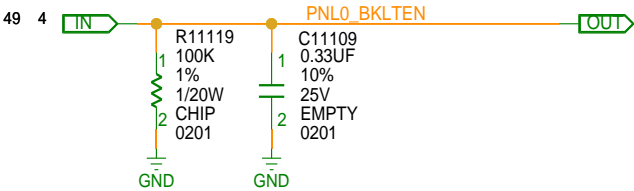
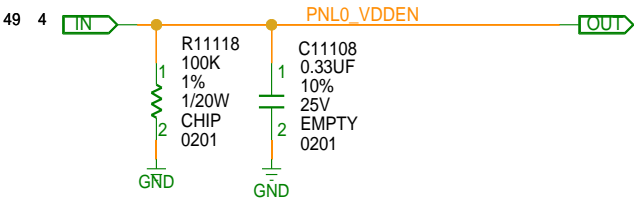
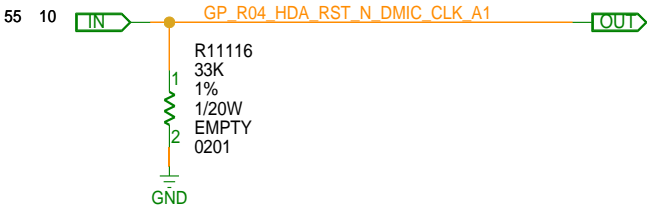
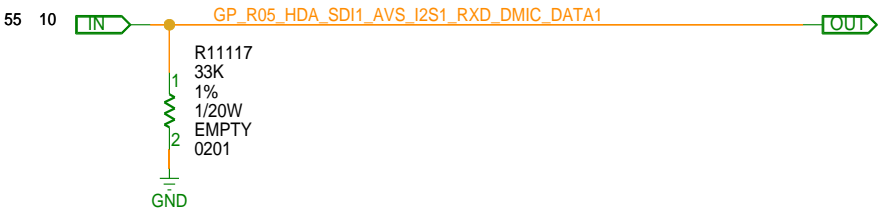
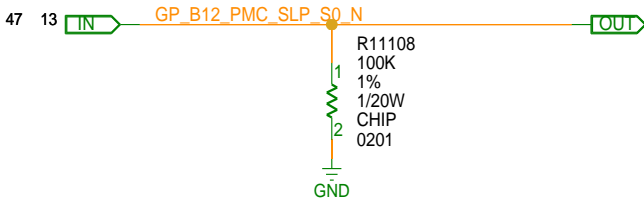
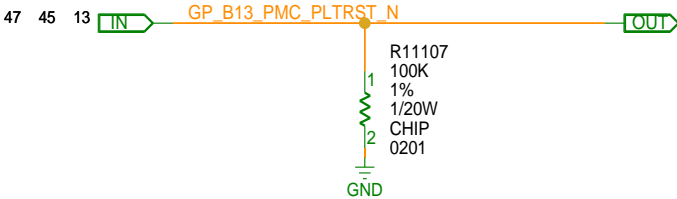
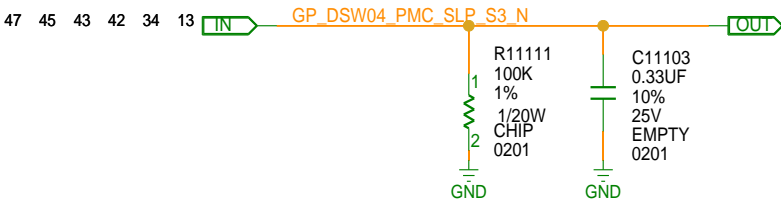
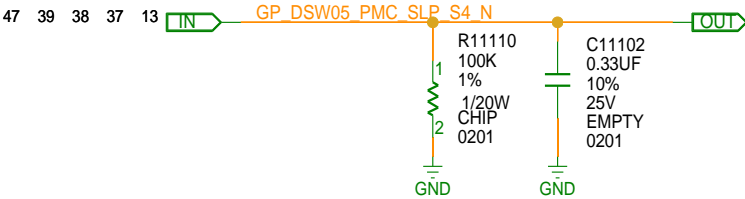
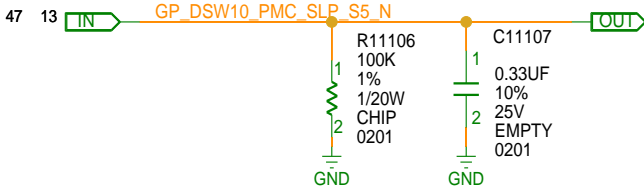
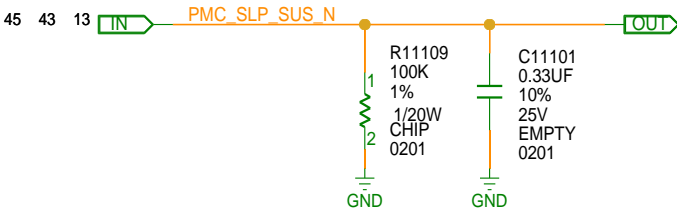
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PCH GLITCH CIRCUIT

MODULE REV DETAILS

MODULE NAME	REV	DATE

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CUSTOM TEXT BPAGE

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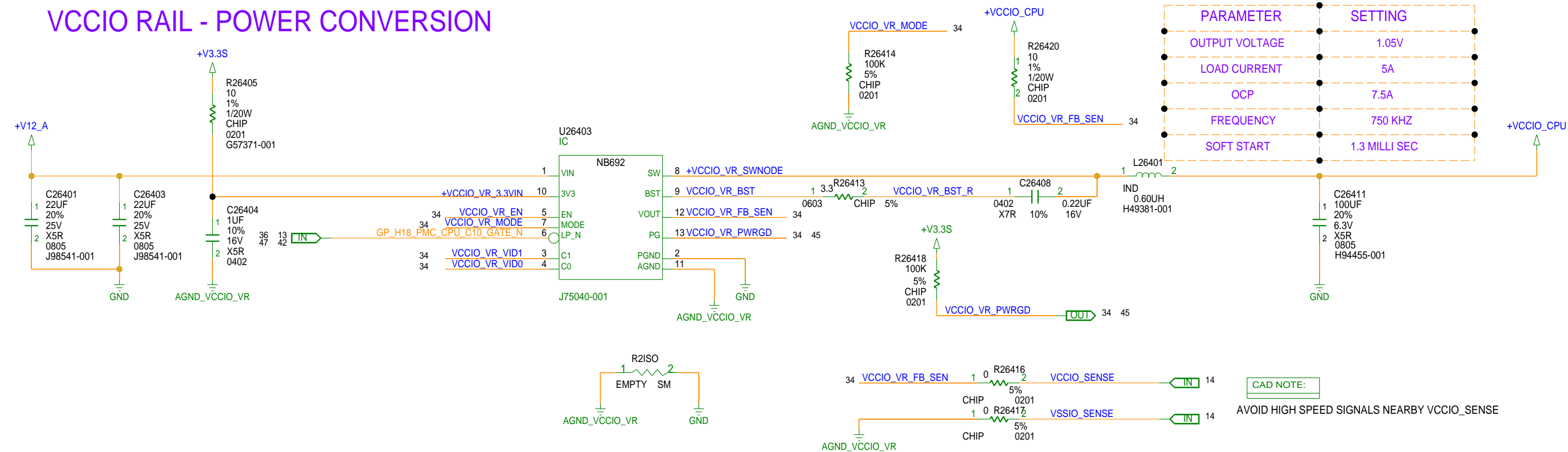
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POWER DELIVERY - VCCIO RAIL

MODULE REV DETAILS

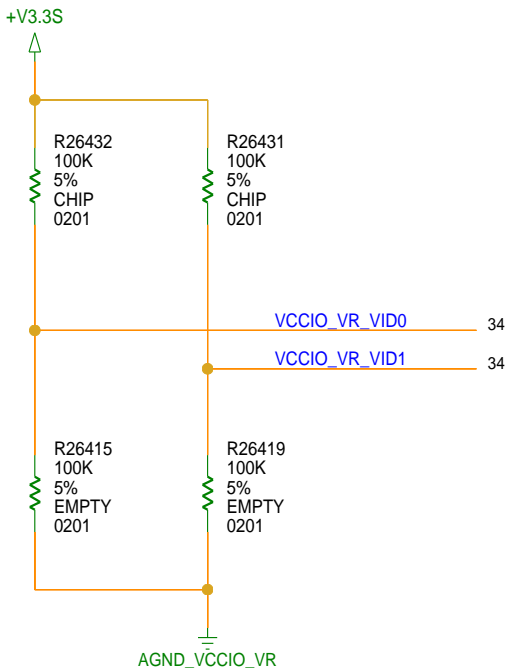
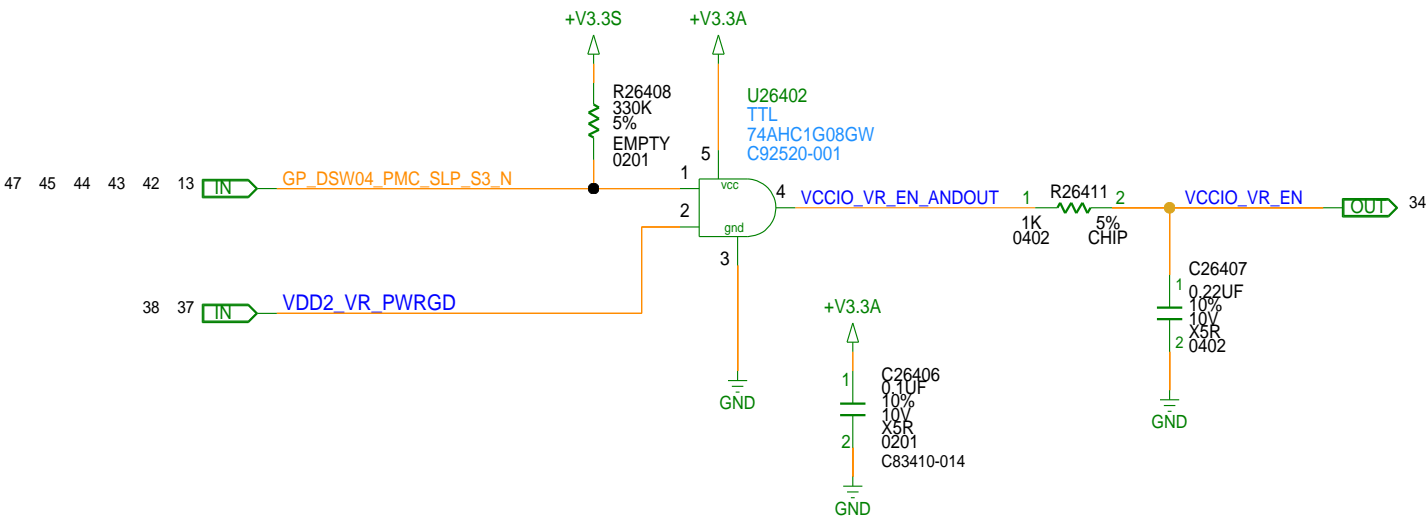
MODULE NAME	REV	DATE

VCCIO RAIL - POWER CONVERSION



VCCIO VR ENABLE SIGNAL GENERATION

VCCIO VR VID SELECTION TABLE



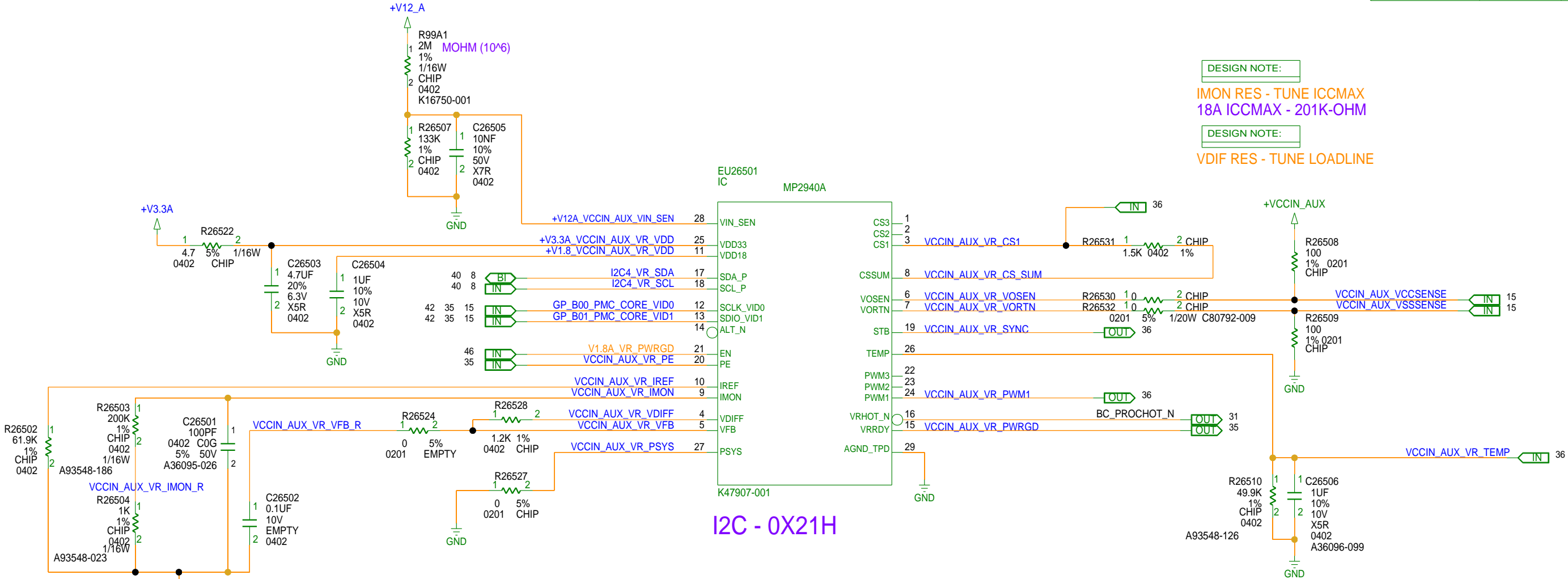
VID TABLE FOR MODE RES = 100K-OHM 1%

RES SETTING	OUTPUT VOLTAGE
LP# VID1 VID0	
0 X X	DECAY TO 0, PG HIGH
1 0 0	0.80V
1 0 1	0.95V
1 1 0	1.0V
1 1 1	1.05V

POWER DELIVERY - VCCIN AUX RAIL

MODULE REV DETAILS

MODULE NAME	REV	DATE



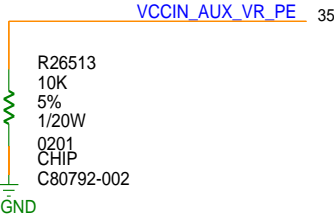
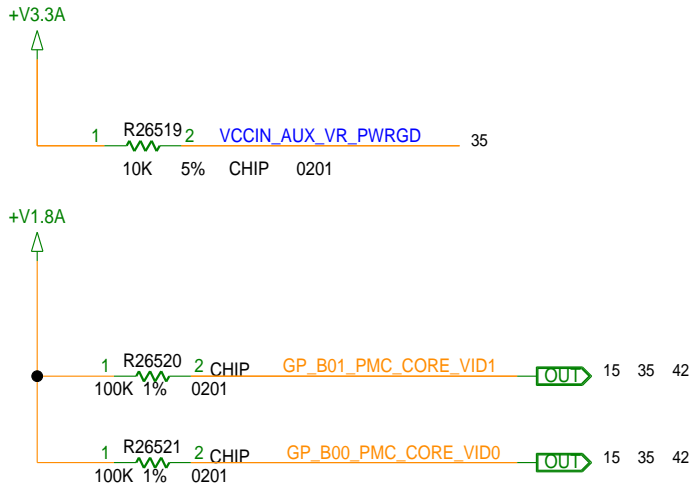
DESIGN NOTE:

IMON RES - TUNE ICCMAX
18A ICCMAX - 201K-OHM

DESIGN NOTE:

VDIF RES - TUNE LOADLINE

I2C - 0X21H

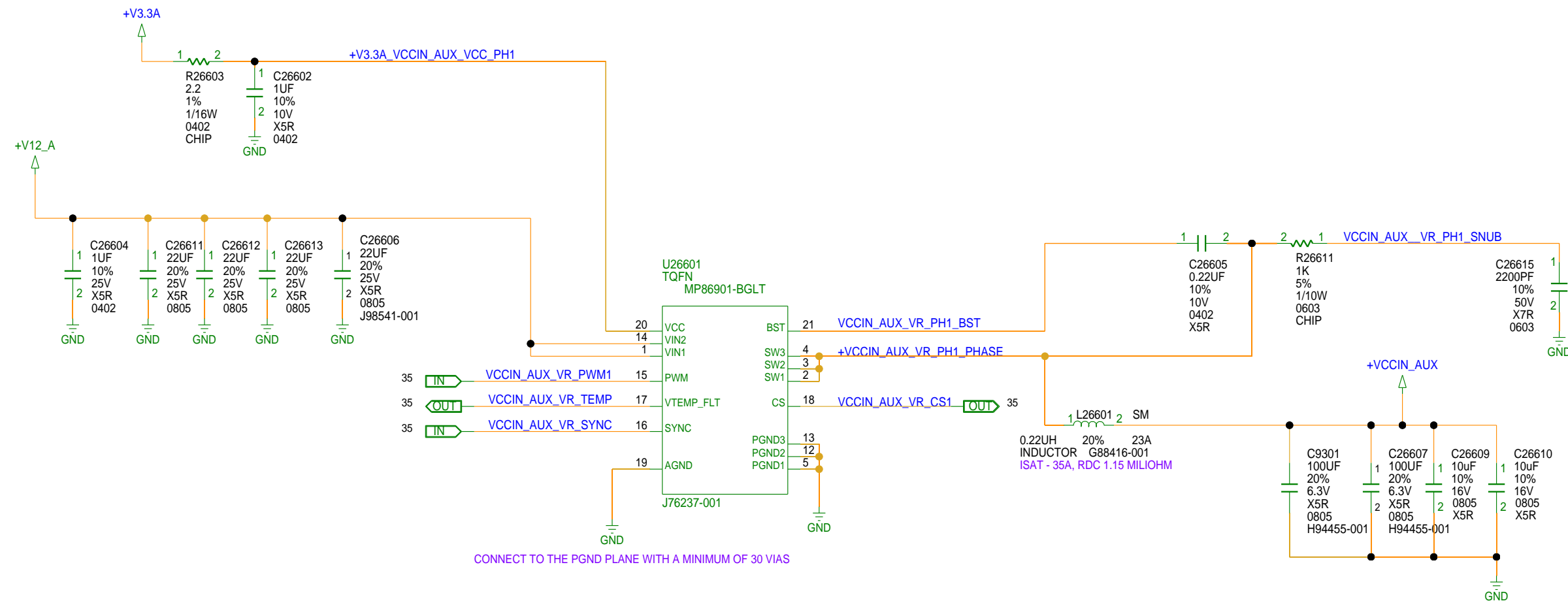


VID TABLE		
VID 1	VID 0	OUTPUT VOLTAGE
0	0	0 V
0	1	1.10 V
1	0	1.65 V
1	1	1.80 V

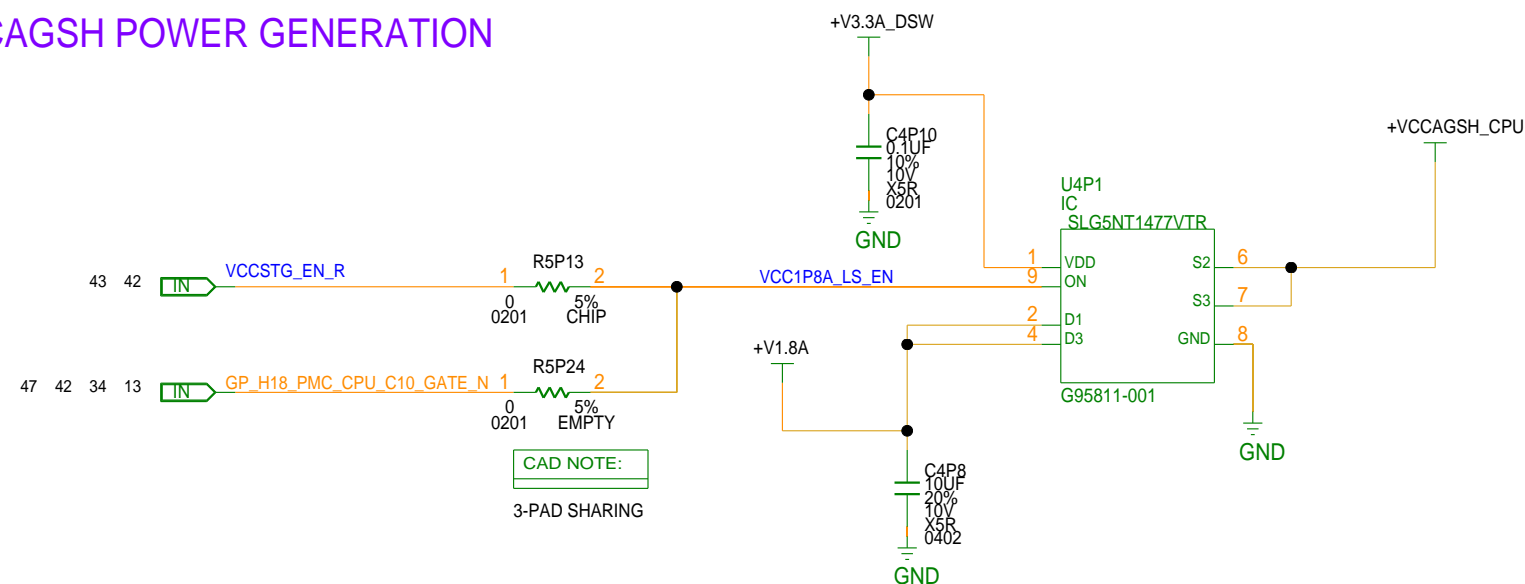
PARAMETER	SETTING
OUTPUT VOLTAGE	VID SELECTABLE
LOAD CURRENT	13A
OCF	35A
FREQUENCY	1MHZ
SOFT START	NA



MODULE REV DETAILS		
MODULE NAME	REV	DATE



+VCCAGSH POWER GENERATION

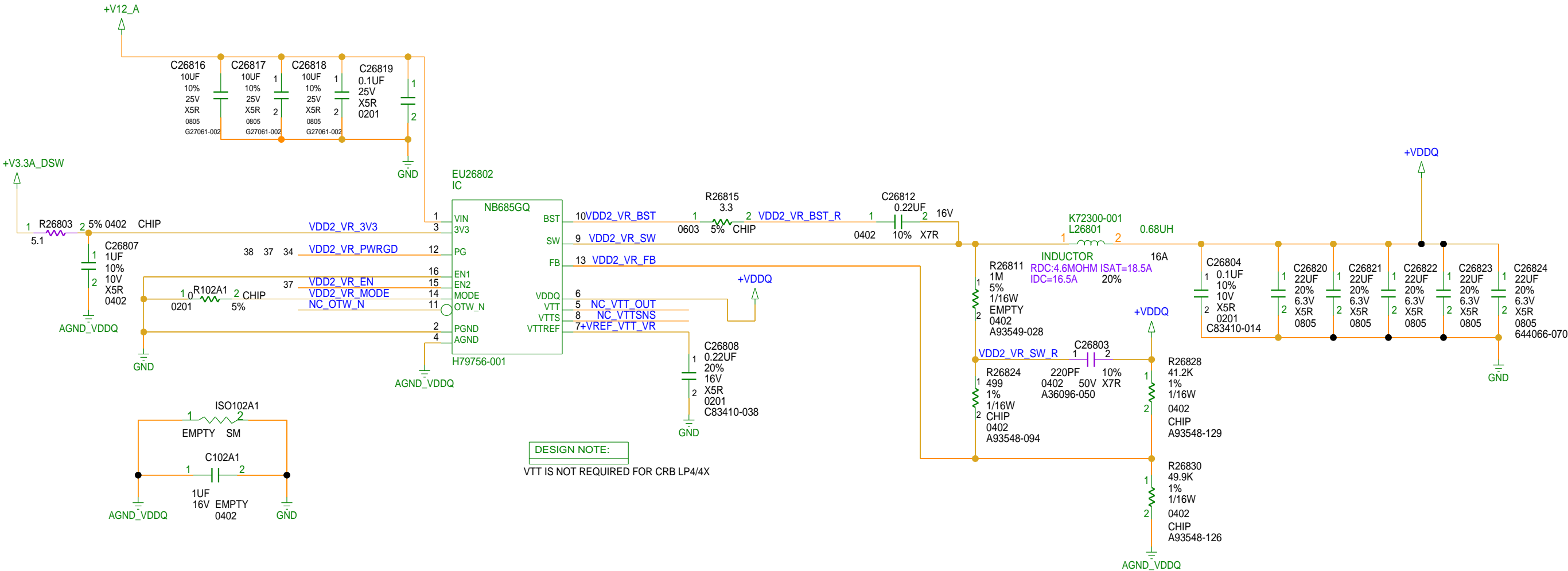


MODULE REV DETAILS

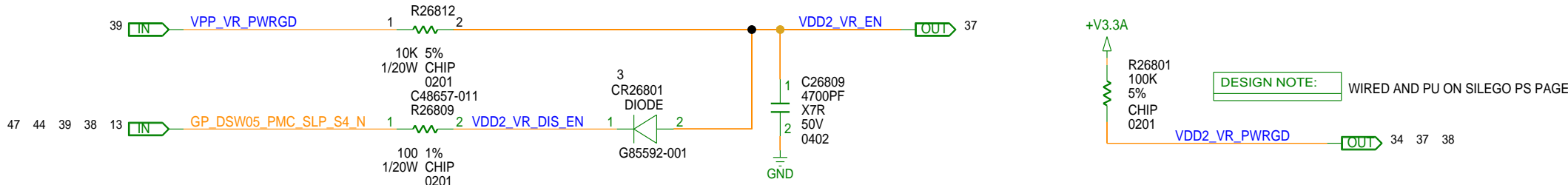
MODULE NAME	REV	DATE

POWER DELIVERY - VDD2(VDDQ) RAIL

VDD2 RAIL - POWER CONVERSION



VDD2 ENABLE SIGNAL GENERATION



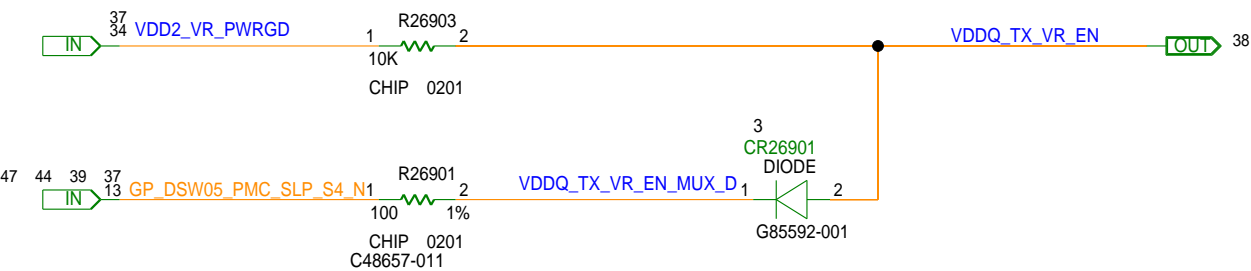
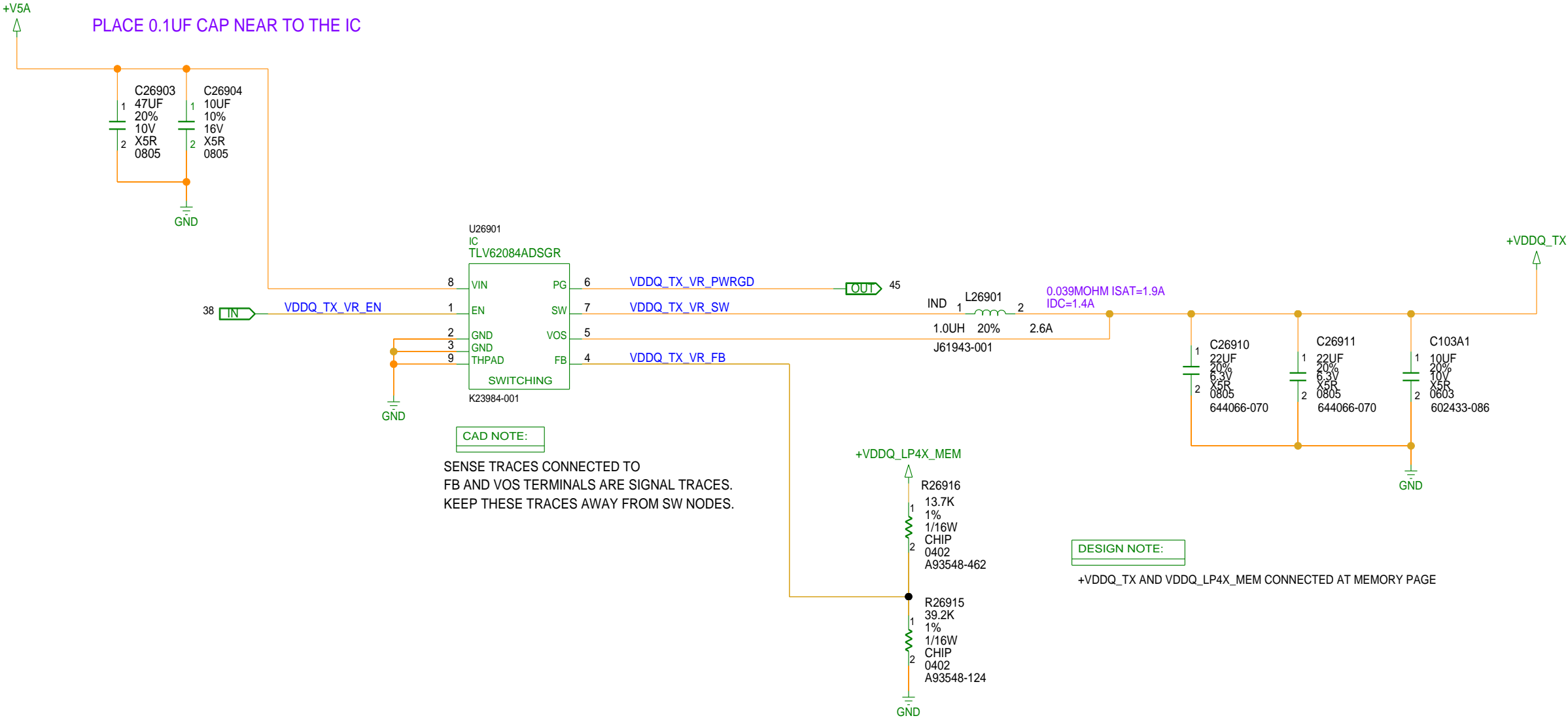
PARAMETER	SETTING
OUTPUT VOLTAGE	1.1V
LOAD CURRENT	11.65A
OCV	12.0A
FREQUENCY	700 KHZ
SOFT START	2.2 MS

POWER DELIVERY - VDDQ_TX RAIL

VDDQ_TX RAIL - POWER CONVERSION

MODULE REV DETAILS

MODULE NAME	REV	DATE



PARAMETER	SETTING
OUTPUT VOLTAGE	0.6V
LOAD CURRENT	1.5A
OCP	2.0A
FREQUENCY	2 MHZ
SOFT START	40 MICRO SEC

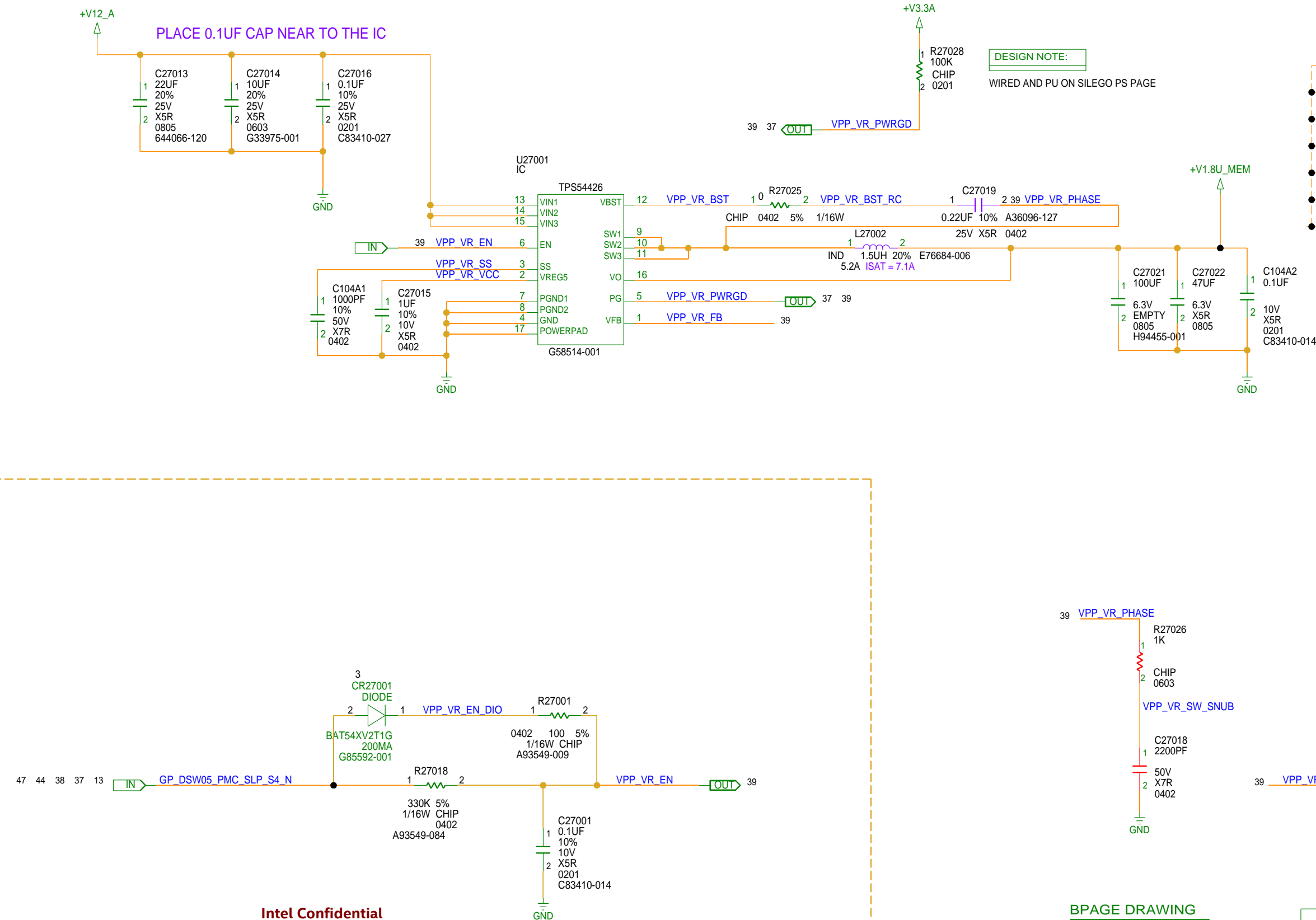
POWER DELIVERY -VPP(V1.8U_MEM) RAIL

VPP (1.8V) RAIL - POWER CONVERSION

PLACE 0.1UF CAP NEAR TO THE IC

DESIGN NOTE:
WIRED AND PU ON SILEGO PS PAGE

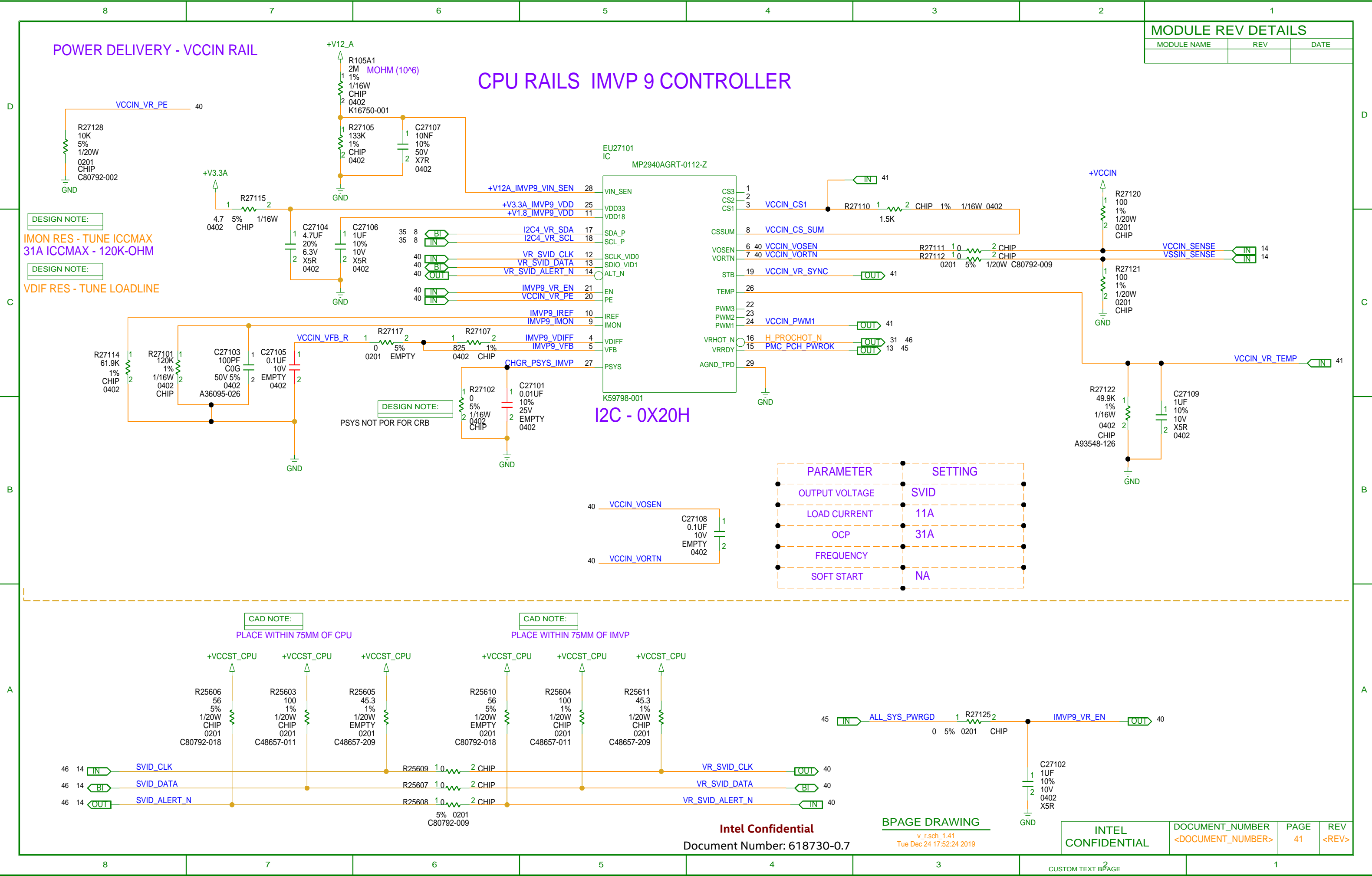
PARAMETER	SETTING
OUTPUT VOLTAGE	1.8V
LOAD CURRENT	3.8A
OCp	4.7A
FREQUENCY	700KHZ
SOFT START	0.4 MS



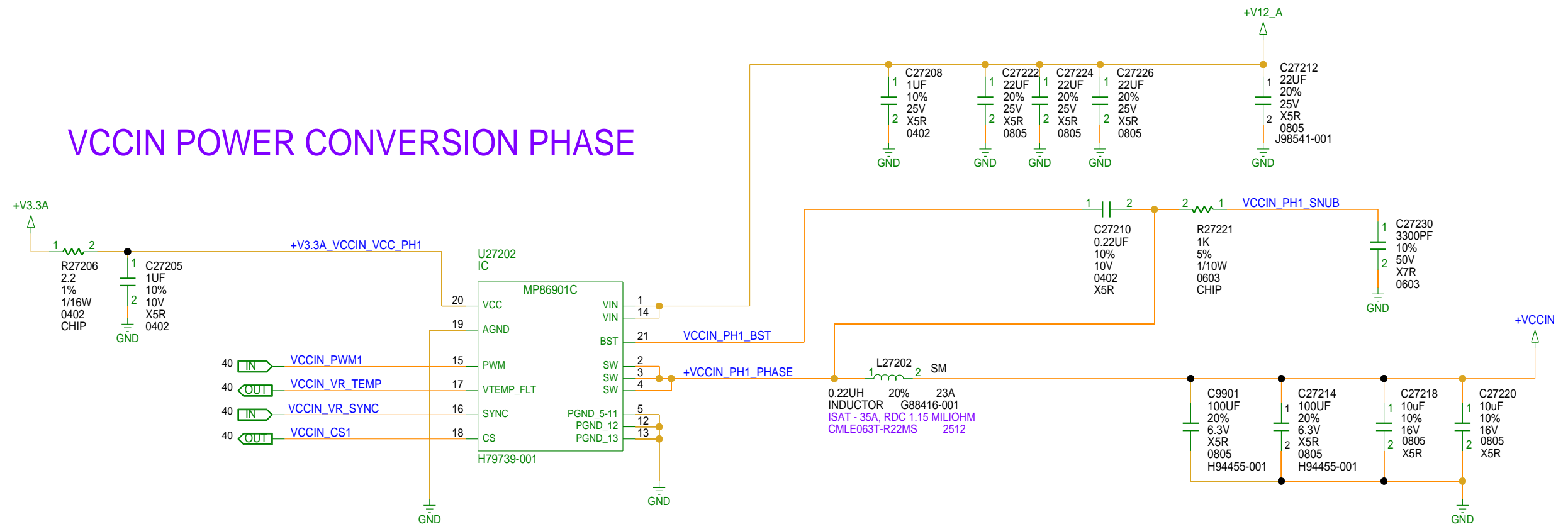
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Document Number: 618730-0.7

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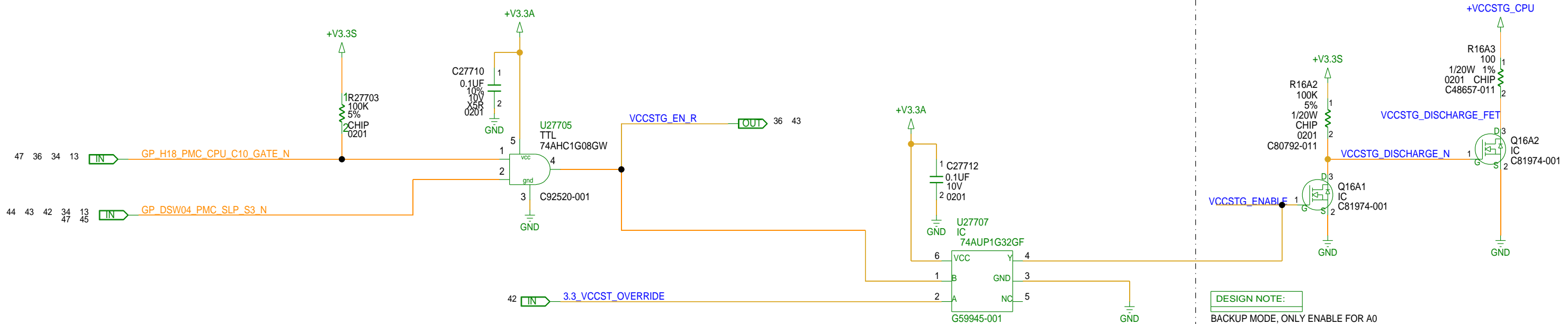
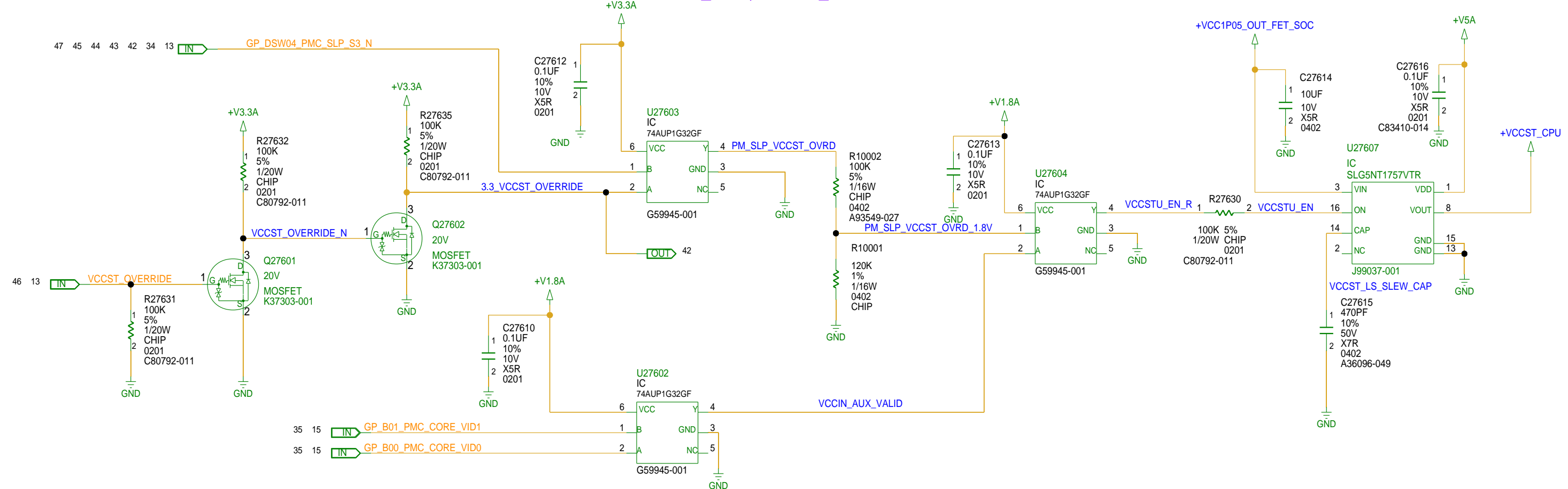


VCCIN POWER CONVERSION PHASE



CONNECT TO GND PLANE WITH A MINIMUM OF 40 VIAS

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VCCSFR_OC GENERATION

The schematic diagram illustrates the power management section of the SLG55550-001 SoC, specifically the +V1.8A_ADC_LDO and +VCCSFR_OC_CPU regulators.

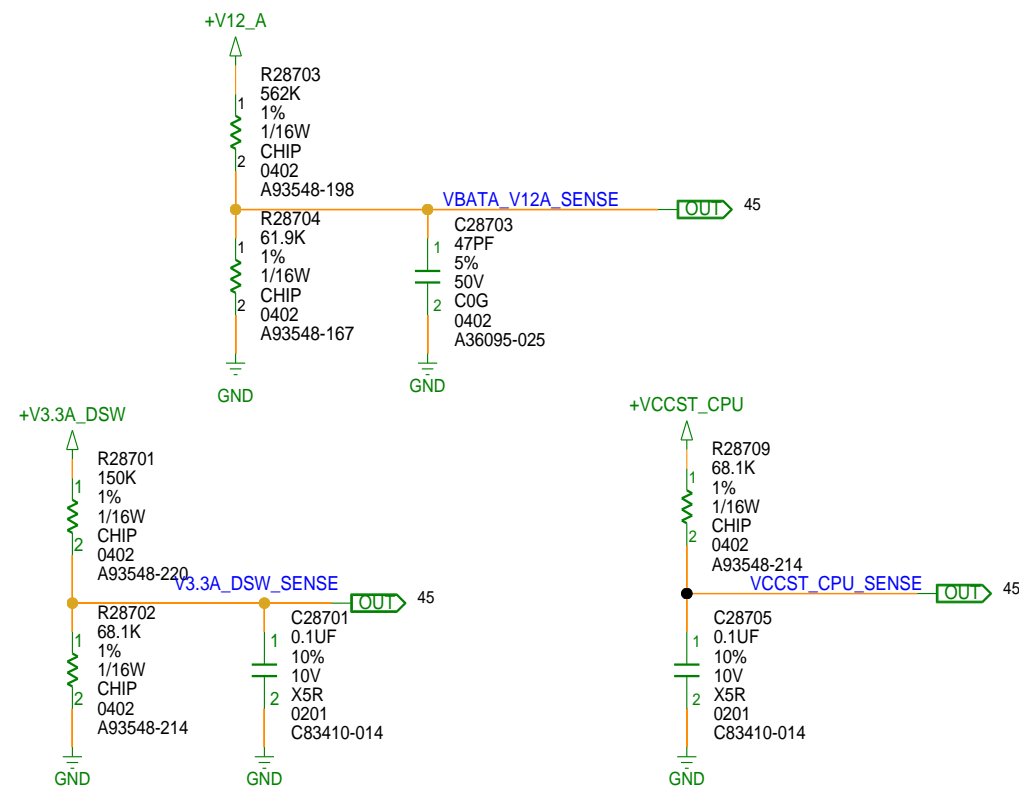
+V1.8A_ADC_LDO Regulator:

- Input:** GP_DS04_PMC_SLP_S3_N (pin 47) is connected to the IN pin of the TPS745 LDO (U27401).
- TPS745 LDO (U27401):**
 - IN: Connected to GP_DS04_PMC_SLP_S3_N.
 - EN: Connected to GND.
 - FB: Connected to the output node.
 - PG: Connected to GND.
 - THPAD: Connected to GND.
- Output Node:** The output of the LDO is connected to the +V1.8A_ADC_LDO output.
- Capacitors:**
 - C27401 (2.2uF, 20%, 6.3V, X5R, 0402) is connected to the input.
 - C27402 (0.1uF, 10%, 25V, EMPTY, 0201) is connected to the output.
 - C27403 (0.1uF, 10%, 10V, X5R, 0201) is connected to the output.
 - C27404 (10uF, 20%, 10V, X5R, 0402) is connected to the output.
- Resistors:**
 - R27406 (49.9K, 1%, 1/16W, CHIP, A93548-126) is connected to the output.
 - R27407 (22K, 1%, 1/16W, CHIP, A93548-639) is connected to the output.
 - R27405 (10K, 5%, 1/20W, CHIP, 0201) is connected to the output.
- Input Voltage:** +V3.3A is connected to the input of the LDO.

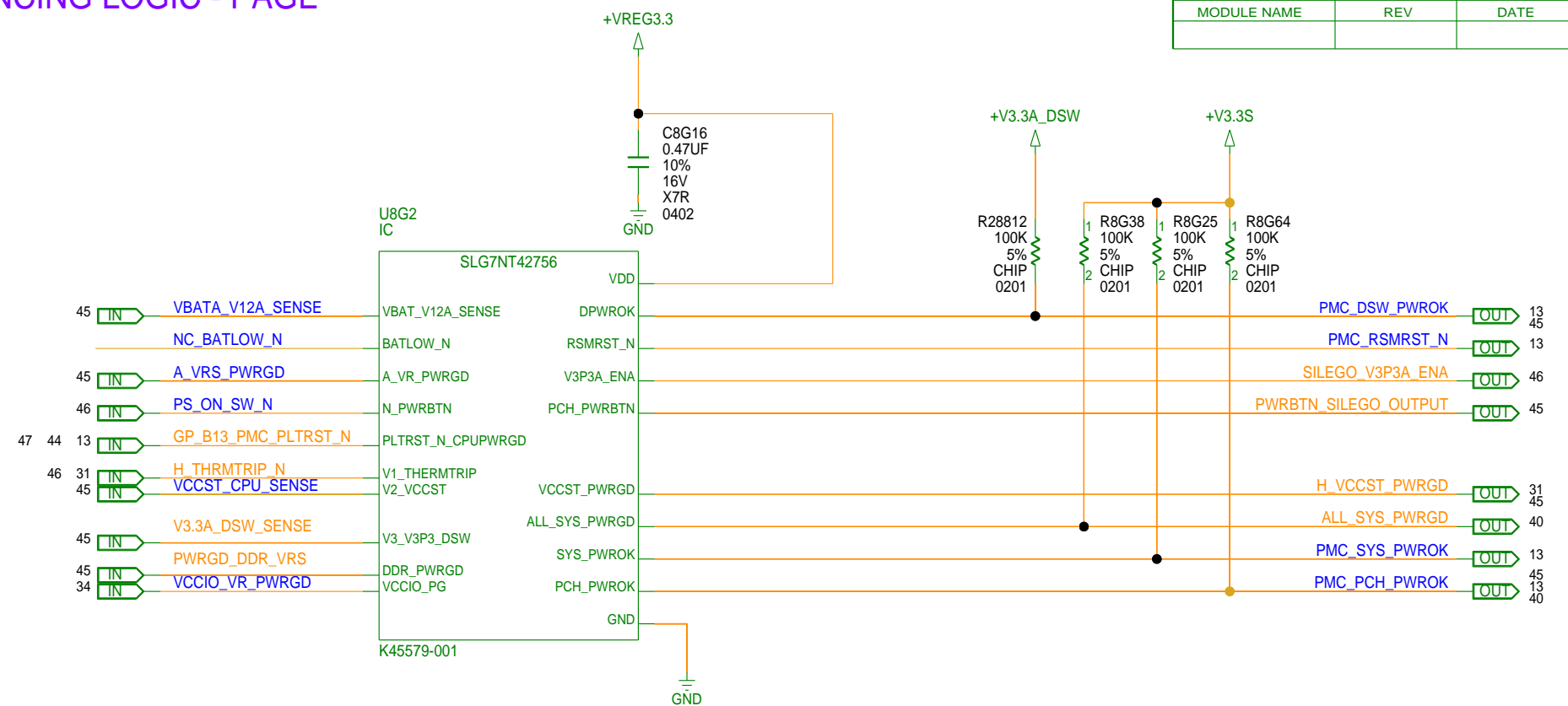
+VCCSFR_OC_CPU Regulator:

- Input:** VCCSTG_EN_R (pin 42) is connected to the ON pin of the SLG5NT1533V LDO (U27704).
- SLG5NT1533V LDO (U27704):**
 - ON: Connected to VCCSTG_EN_R.
 - VDD: Connected to the output node.
 - D: Connected to GND.
 - CAP: Connected to GND.
 - GND: Connected to GND.
- Output Node:** The output of the LDO is connected to the +VCCSFR_OC_CPU output.
- Capacitors:**
 - C27703 (0.1uF, 10%, 10V, X5R, 0201) is connected to the input.
 - C27704 (0.1uF, 10%, 10V, X5R, 0402) is connected to the input.
 - C27706 (330PF, 10%, 50V, X7R, 0402) is connected to the output.

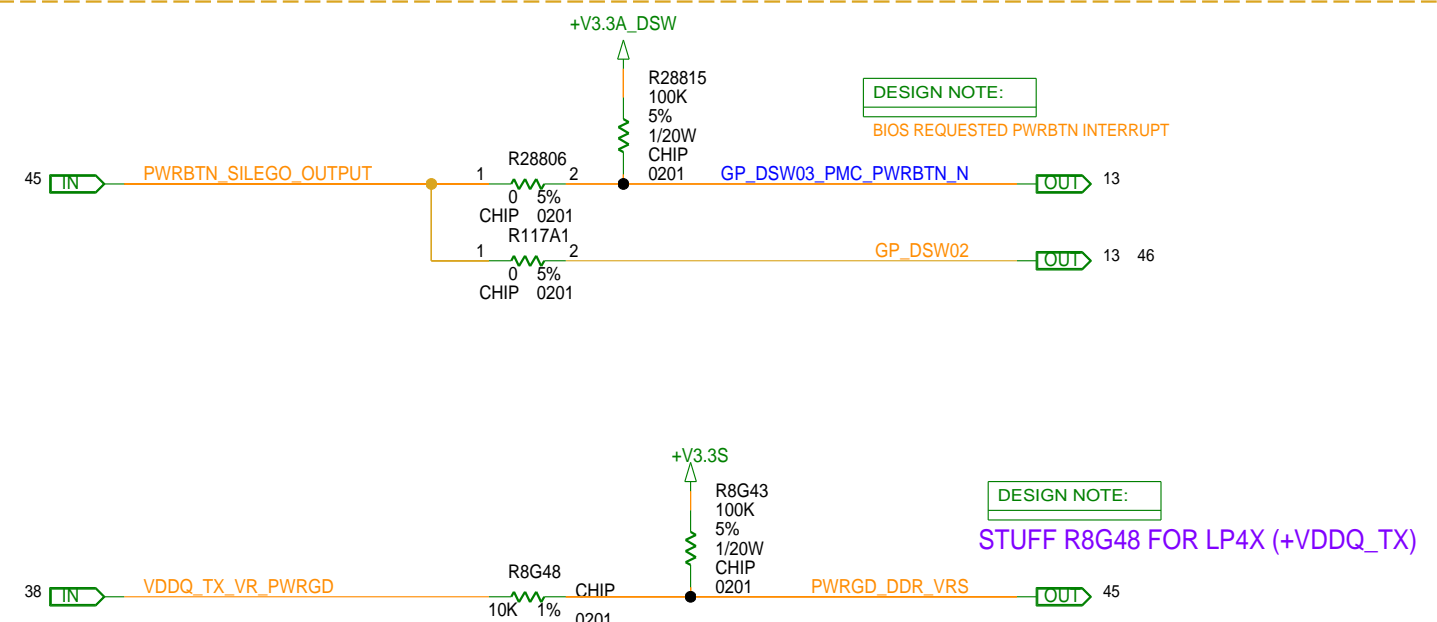
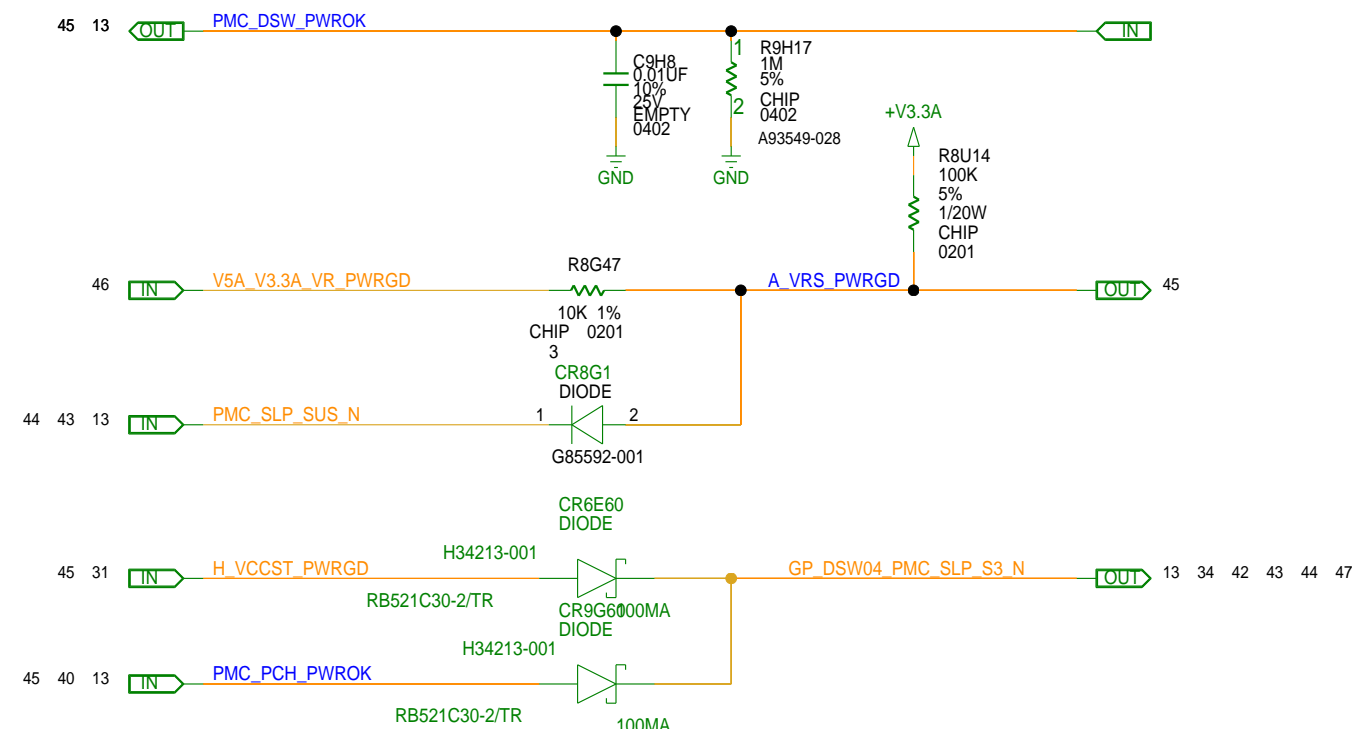
POWER DELIVERY - POWER SEQ.



POWER SEQUENCING LOGIC - PAGE



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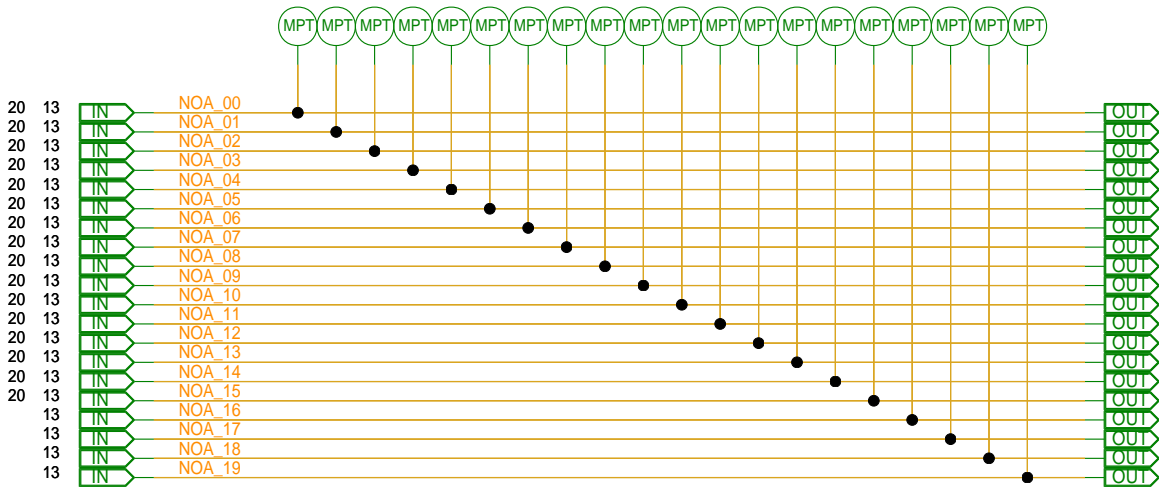
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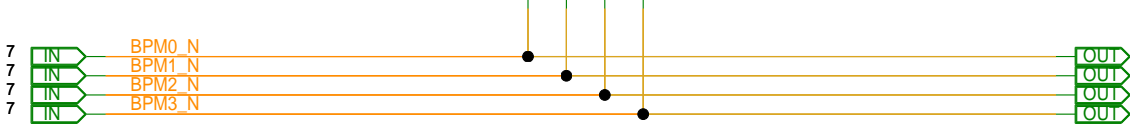
NOA SIGNALS



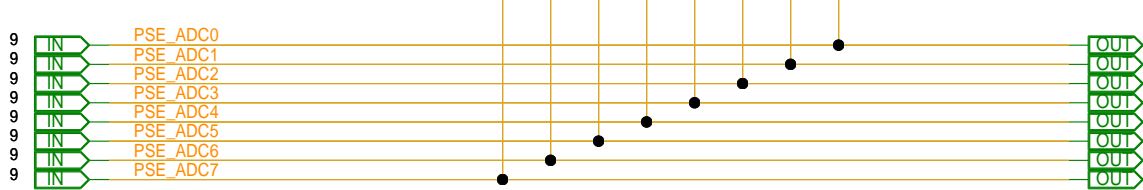
SVIC



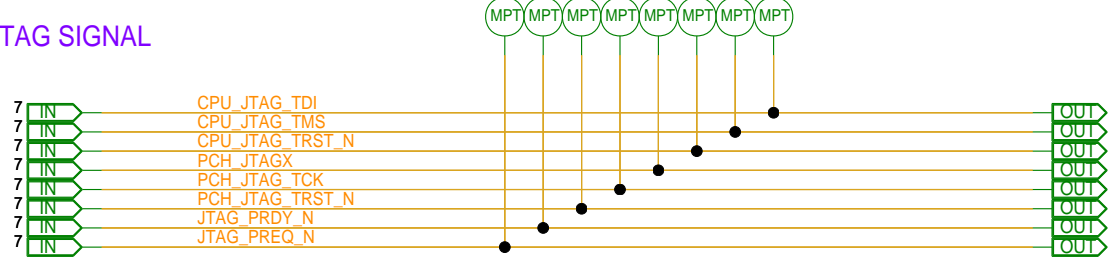
BPM SIGNALS



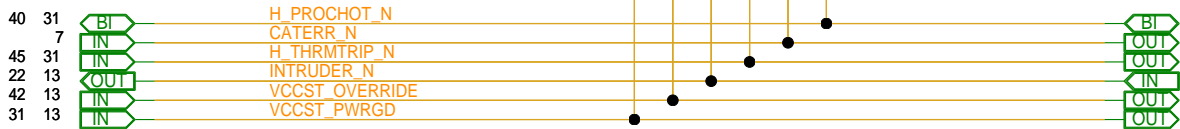
PSE ADC



JTAG SIGNAL



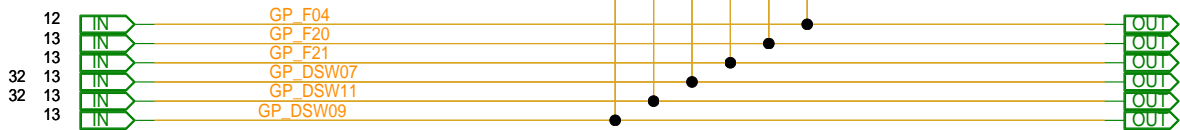
CPU SIDEBAND



CPU SIDEBAND



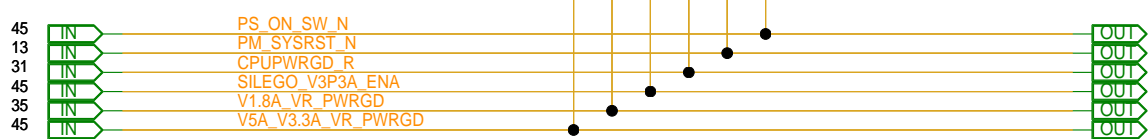
CPU SIDEBAND



FSPI CS



MCL MISCL SIGNALS

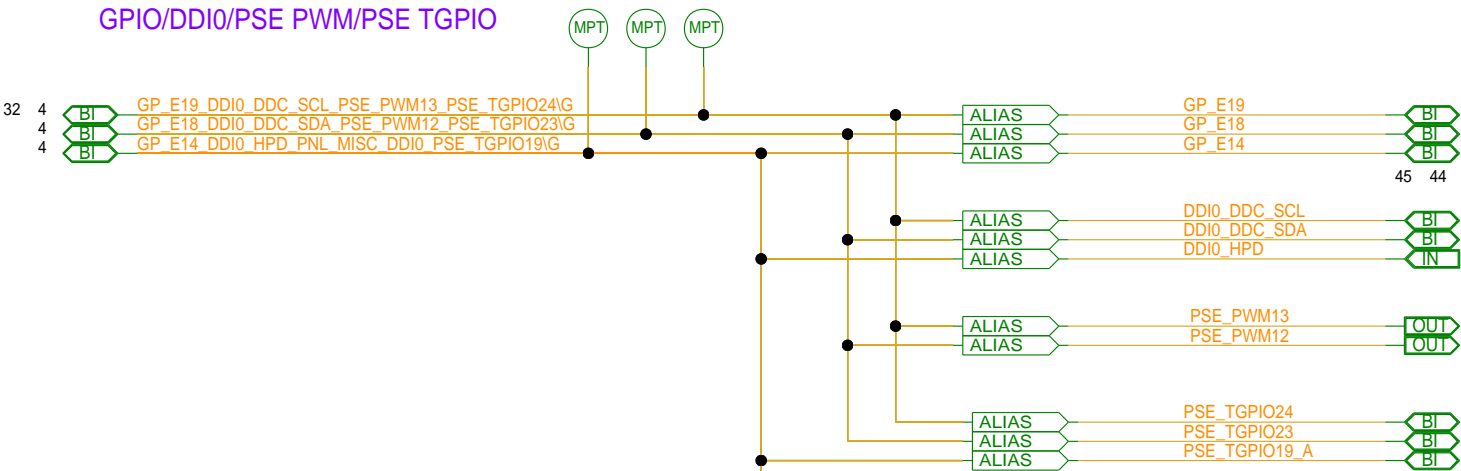


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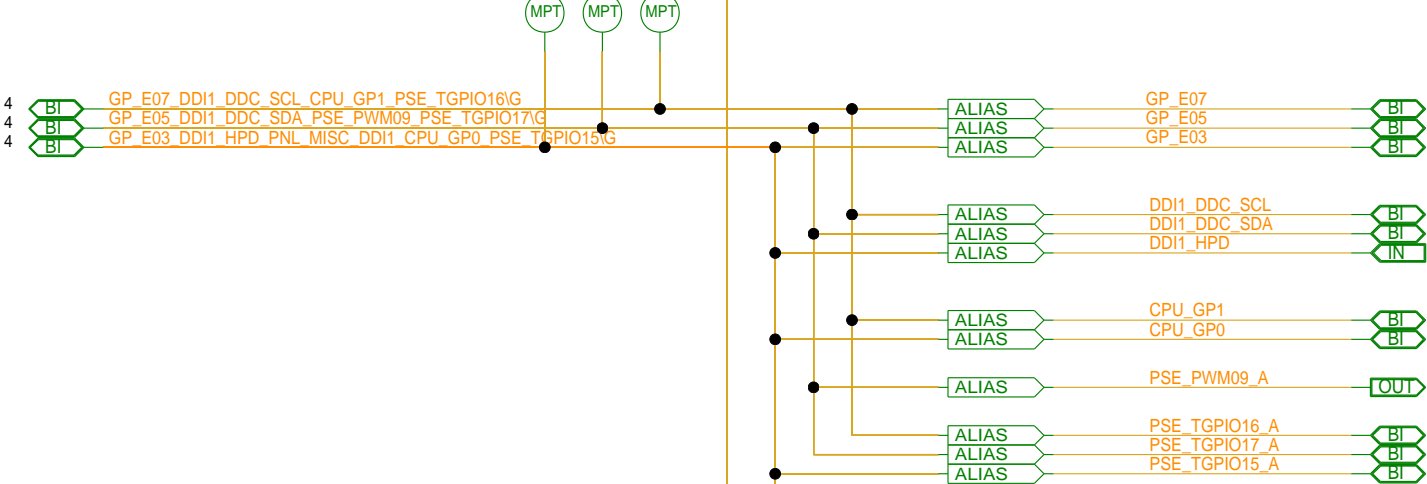
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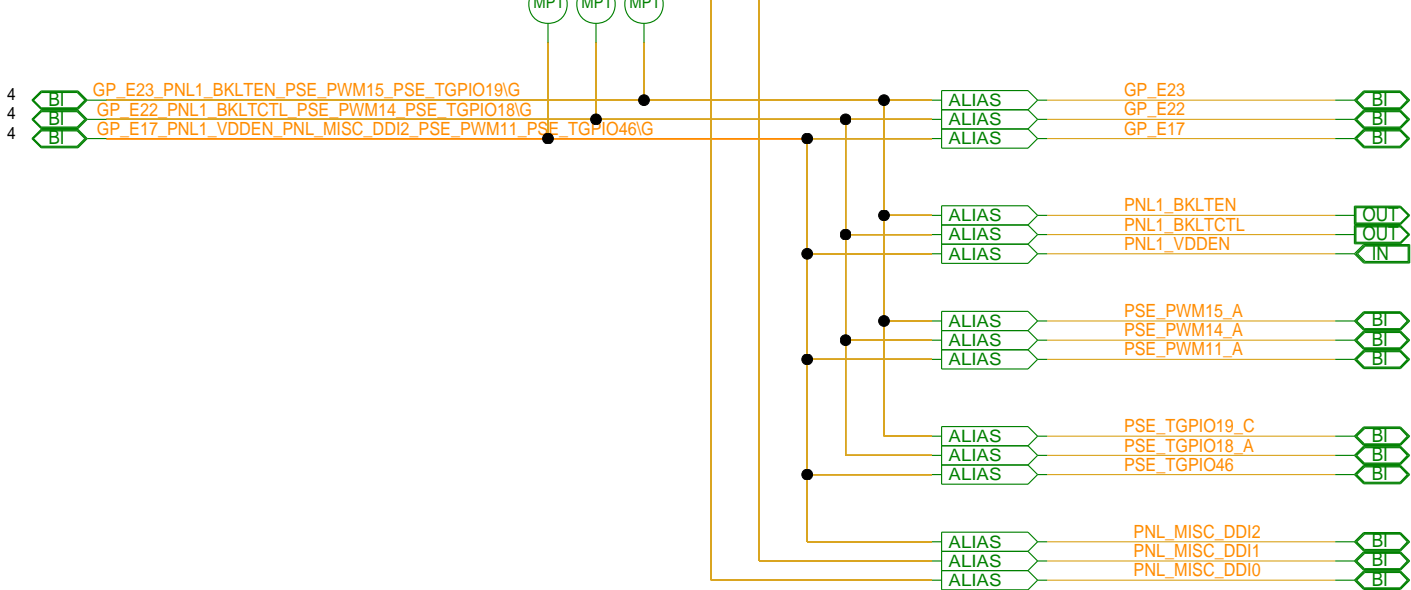
GPIO/DDIO/PSE PWM/PSE TGPIO



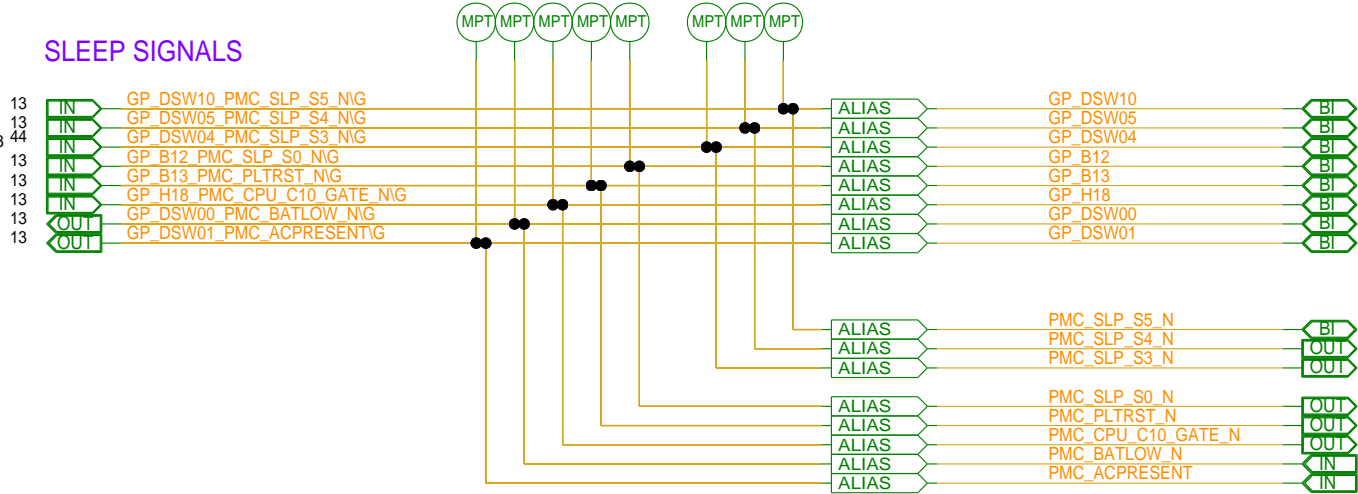
GPIO/DDI1/CPU/PSE PWM/PSE TGPIO



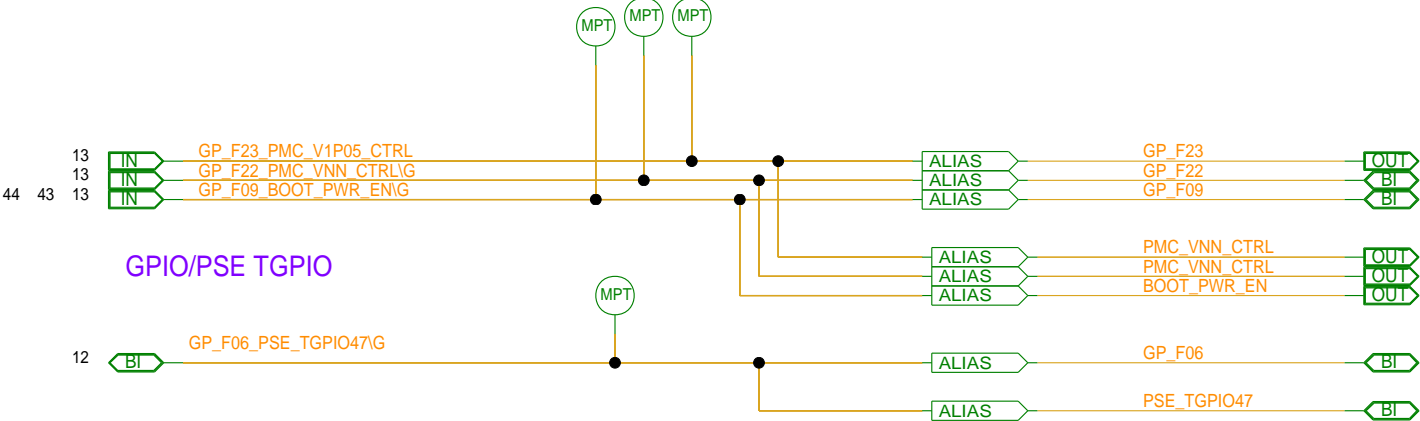
GPIO/PNL1 CTRL/PSE PWM/PSE TGPIO/PNL MISC



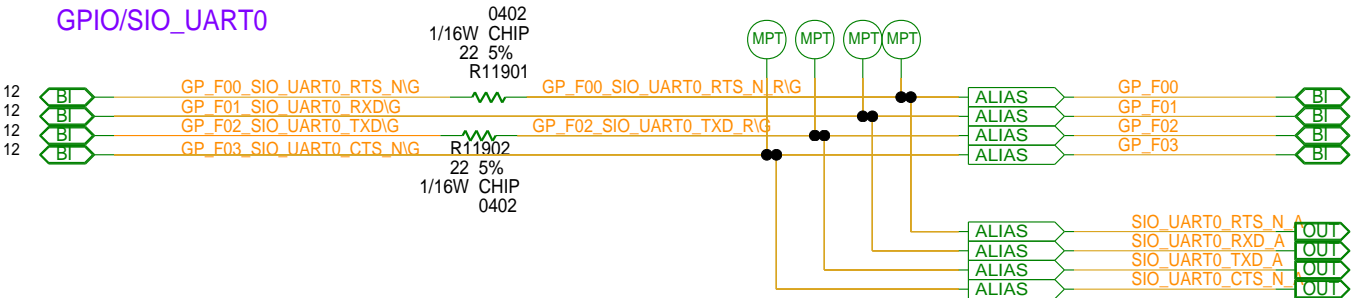
SLEEP SIGNALS



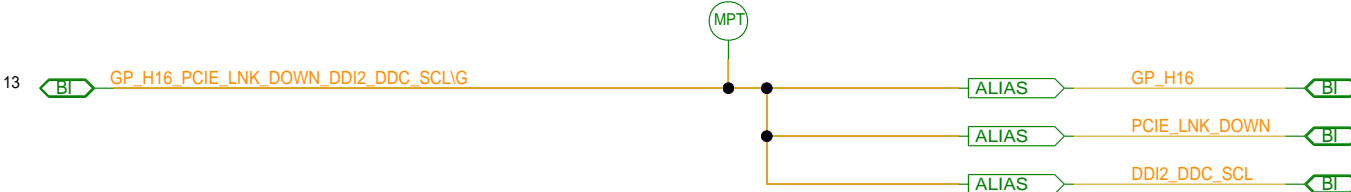
GPIO/PSE TGPIO



GPIO/SIO_UART0



GPIO/PCIE LNK/DDI2 SCL



MODULE REV DETAILS

MODULE NAME	REV	DATE

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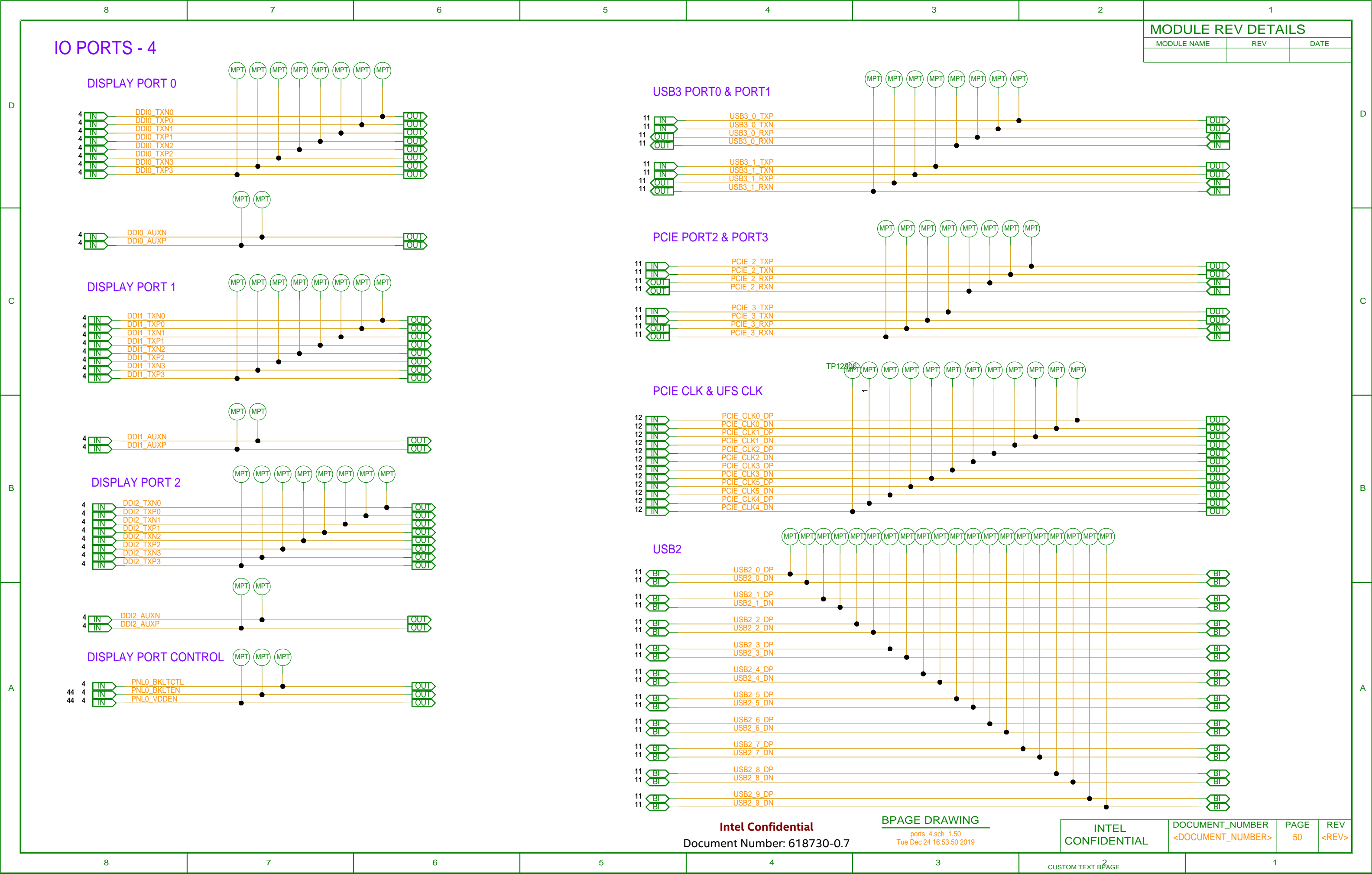
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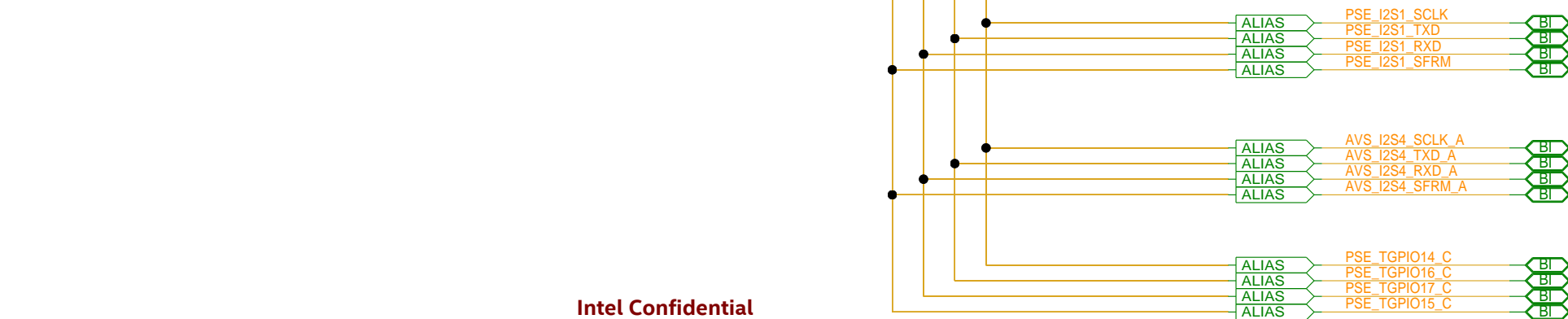
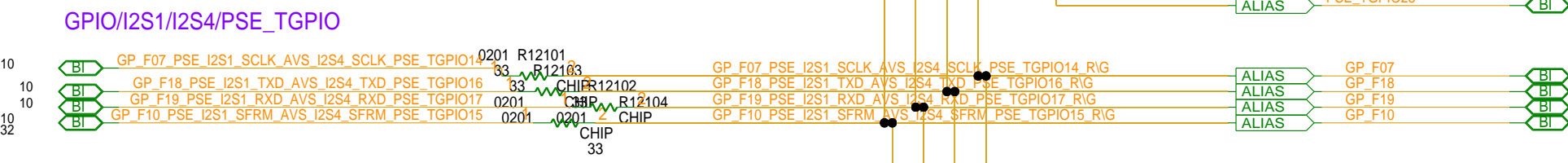
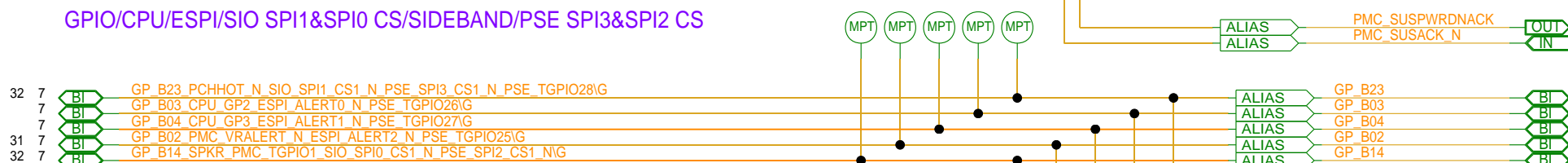
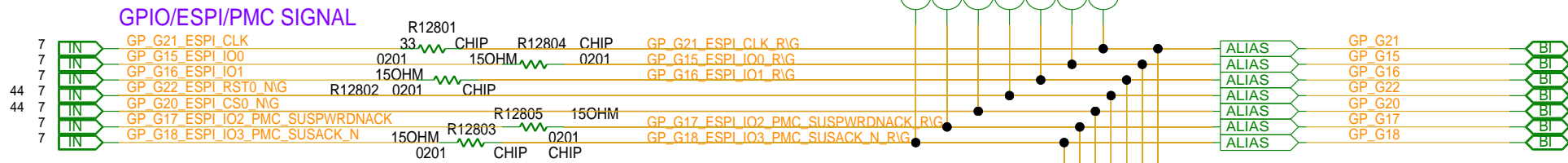
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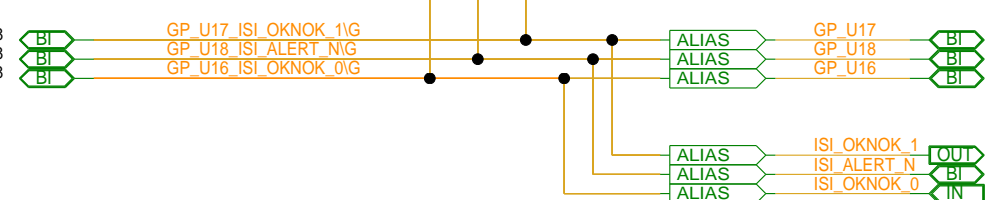
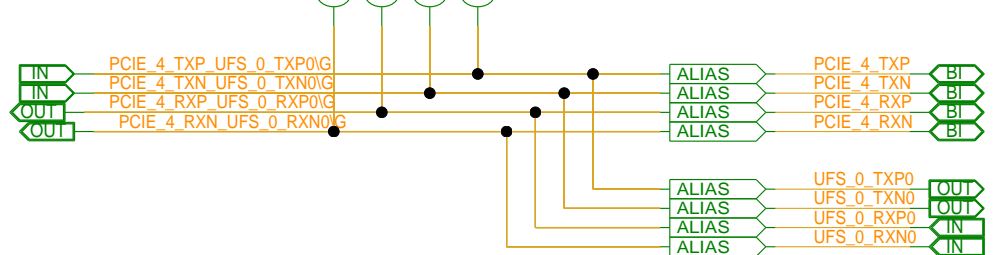
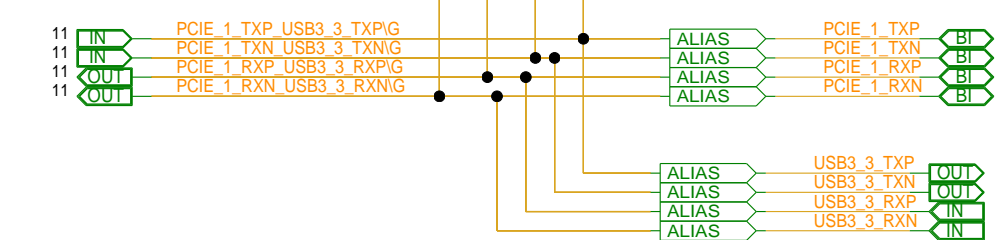
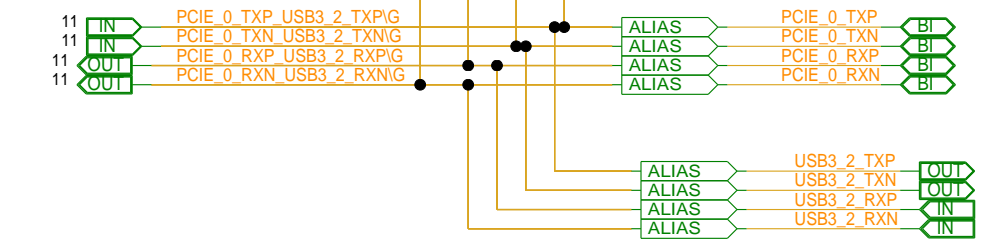
IO PORTS - 5



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MODULE REV DETAILS

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IO PORTS - 6

GPIO/PSE GBE1/PSE UART5/PSE HUART3/PSE TGPI0

GP_H01_PSE_GBE1_RST_N_PSE_UART5_TXD/G
GP_H00_PSE_GBE1_INT_PSE_UART5_RXD/G
GP_C06_PSE_GBE1_MDC/G
GP_C07_PSE_GBE1_MDIO_PSE_HUART3_RE/G
GP_H03_PSE_GBE1_PPS_PSE_UART5_CTS_N_PSE_TGPIO21/G
GP_H02_PSE_GBE1_AUXTS_PSE_UART5_RTS_N/G

MPT MPT MPT MPT MPT MPT

ALIAS GP_H01 BI
ALIAS GP_H00 BI
ALIAS GP_C06 BI
ALIAS GP_C07 BI
ALIAS GP_H03 BI
ALIAS GP_H02 BI

PSE_GBE1_RST_N OUT
PSE_GBE1_INT IN
PSE_GBE1_MDC IN
PSE_GBE1_MDIO BI
PSE_GBE1_PPS OUT
PSE_GBE1_AUXTS IN

PSE_UART5_TXD OUT
PSE_UART5_RXD IN
PSE_UART5_CTS_N IN
PSE_UART5_RTS_N OUT

ALIAS PSE_HUART3_RE IN

ALIAS PSE_TGPIO21 BI

GPIO/SIO SPI0/PSE SPI2/ESPI CS

GP_B16_SIO_SPI0_CLK_PSE_SPI2_CLK/G
GP_B18_SIO_SPI0_MOSI_PSE_SPI2_MOSIG
GP_B17_SIO_SPI0_MISO_PSE_SPI2_MISO/G
GP_B15_SIO_SPI0_CS0_N_PSE_SPI2_CS0_N_ESPI_CS2_N/G

MPT MPT MPT MPT

ALIAS GP_B16 BI
ALIAS GP_B18 BI
ALIAS GP_B17 BI
ALIAS GP_B15 OUT

SIO_SPI0_CLK OUT
SIO_SPI0_MOSI OUT
SIO_SPI0_MISO IN
SIO_SPI0_CS0_N OUT

PSE_SPI2_CLK OUT
PSE_SPI2_MOSI OUT
PSE_SPI2_MISO IN
PSE_SPI2_CS0_N OUT

ALIAS ESPI_CS1_N OUT

GPIO/GBE/PSE I2C6/SIO I2C0/PSE I2C7/PSE UART3

GP_U01_GBE_RST_N_PSE_I2C6_SDA/G
GP_U00_GBE_INT_PSE_I2C6_SCL/G
GP_C17_GBE_MDC_PSE_UART3_TXD_SIO_I2C0_SCL/G
GP_C16_GBE_MDIO_PSE_UART3_RXD_SIO_I2C0_SDA/G
GP_U02_GBE_PPS_PSE_I2C7_SCL/G
GP_U03_GBE_AUXTS_PSE_I2C7_SDA/G

MPT MPT MPT MPT MPT MPT

ALIAS GP_U01 BI
ALIAS GP_U00 BI
ALIAS GP_C17 BI
ALIAS GP_C16 BI
ALIAS GP_U02 BI
ALIAS GP_U03 BI

GBE_RST_N OUT
GBE_INT IN
GBE_MDC IN
GBE_MDIO BI
GBE_PPS OUT
GBE_AUXTS IN

PSE_I2C6_SDA BI
PSE_I2C6_SCL BI

SIO_I2C0_SCL BI
SIO_I2C0_SDA BI

PSE_I2C7_SCL BI
PSE_I2C7_SDA BI

PSE_UART3_TXD OUT
PSE_UART3_RXD IN

GPIO/PSE GBE1 RX

GP_A17_PSE_GBE1_RGMII_RXCLK/G
GP_A18_PSE_GBE1_RGMII_RXCTL/G
GP_A22_PSE_GBE1_RGMII_RXD0_AVIS_I2S5_RXD/G
GP_A21_PSE_GBE1_RGMII_RXD1_AVIS_I2S5_TXD/G
GP_A20_PSE_GBE1_RGMII_RXD2_AVIS_I2S5_SFRM/G
GP_A19_PSE_GBE1_RGMII_RXD3_AVIS_I2S5_SCLK/G

MPT MPT MPT MPT MPT MPT

ALIAS GP_A17 BI
ALIAS GP_A18 BI
ALIAS GP_A22 BI
ALIAS GP_A21 BI
ALIAS GP_A20 BI
ALIAS GP_A19 BI

PSE_GBE1_RGMII_RXCLK IN
PSE_GBE1_RGMII_RXCTL IN
PSE_GBE1_RGMII_RXD0 IN
PSE_GBE1_RGMII_RXD1 IN
PSE_GBE1_RGMII_RXD2 IN
PSE_GBE1_RGMII_RXD3 IN

AVIS_I2S5_RXD IN
AVIS_I2S5_TXD OUT
AVIS_I2S5_SFRM BI
AVIS_I2S5_SCLK OUT

GPIO/SIO SPI1/PSE SPI3/ESPI CS

GP_B20_SIO_SPI1_CLK_PSE_SPI3_CLK/G
GP_B22_SIO_SPI1_MOSI_PSE_SPI3_MOSIG
GP_B21_SIO_SPI1_MISO_PSE_SPI3_MISO/G
GP_B19_SIO_SPI1_CS0_N_PSE_SPI3_CS0_N_ESPI_CS2_N/G

MPT MPT MPT MPT

ALIAS GP_B20 BI
ALIAS GP_B22 BI
ALIAS GP_B21 BI
ALIAS GP_B19 BI

SIO_SPI1_CLK BI
SIO_SPI1_MOSI OUT
SIO_SPI1_MISO IN
SIO_SPI1_CS0_N OUT

PSE_SPI3_CLK BI
PSE_SPI3_MOSI OUT
PSE_SPI3_MISO IN
PSE_SPI3_CS0_N OUT

ALIAS ESPI_CS2_N OUT

GPIO/DDI2/PSE TGPI0/PSE PWM

GP_H20_PSE_PWM07_DDI2_HPDP_PSE_TGPIO55/G
GP_H19_DDI2_DDC_SDAPMC_TGPIO0_PSE_TGPIO20/G

MPT MPT

ALIAS GP_H20 BI
ALIAS GP_H19 BI

DDI2_HPDP BI
DDI2_DDC_SDA BI

PSE_TGPIO55 BI
PSE_TGPIO20 BI

PSE_PWM07 OUT

PMCTGPIO0 OUT

GPIO/SIO I2C5/PSE I2C2/ESPI

GP_B10_SIO_I2C5_SCL_PSE_I2C2_SCL_ESPI_ALERT3_N/G
GP_B09_SIO_I2C5_SDA_PSE_I2C2_SDA_ESPI_CS3_N/G

MPT MPT

ALIAS GP_B10 BI
ALIAS GP_B09 BI

SIO_I2C5_SCL BI
SIO_I2C5_SDA BI

PSE_I2C2_SCL BI
PSE_I2C2_SDA BI

ESPI_ALERT3_N OUT
ESPI_CS3_N OUT

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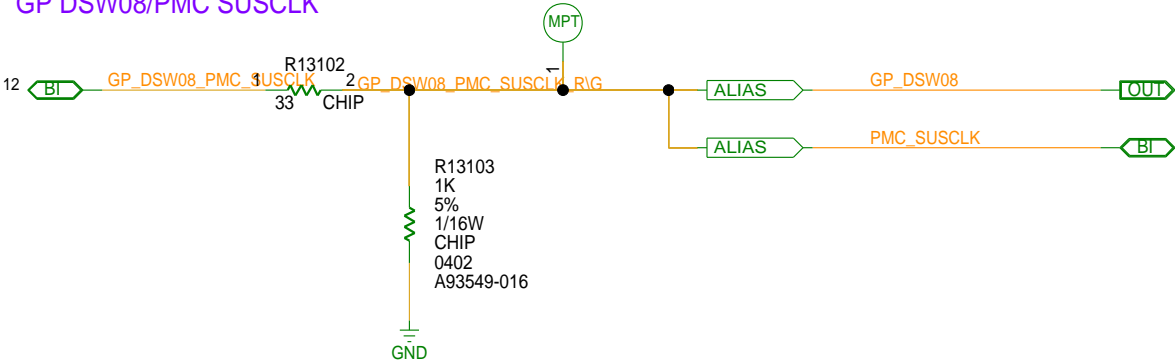
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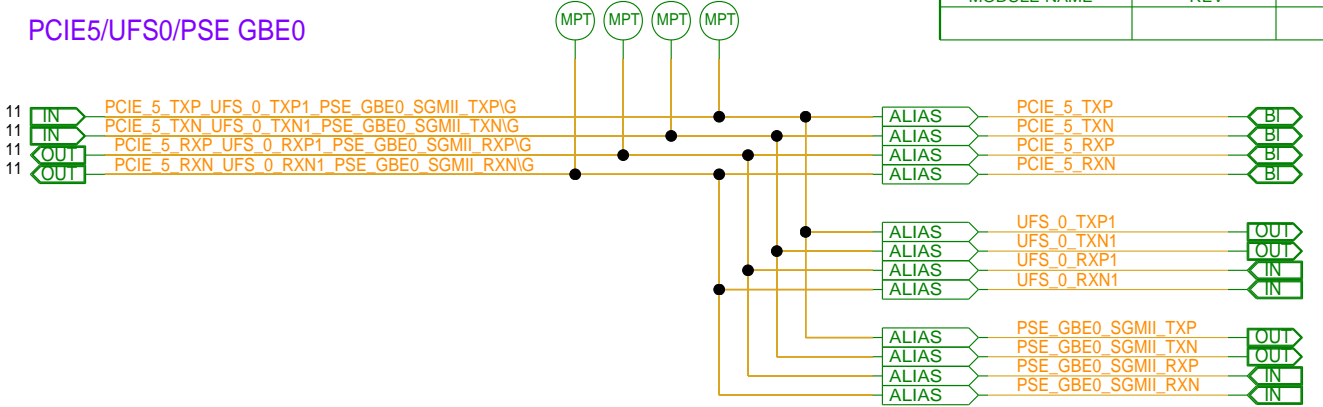
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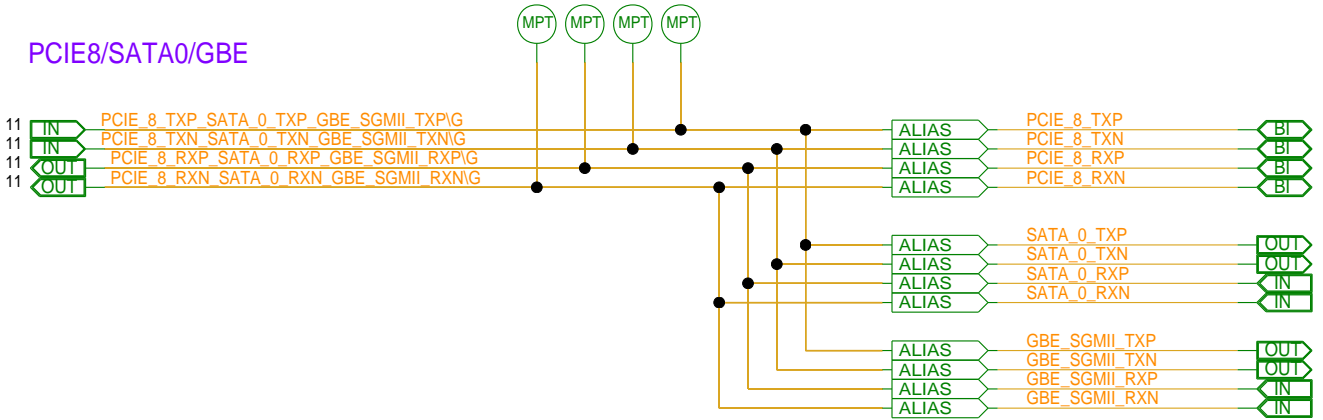
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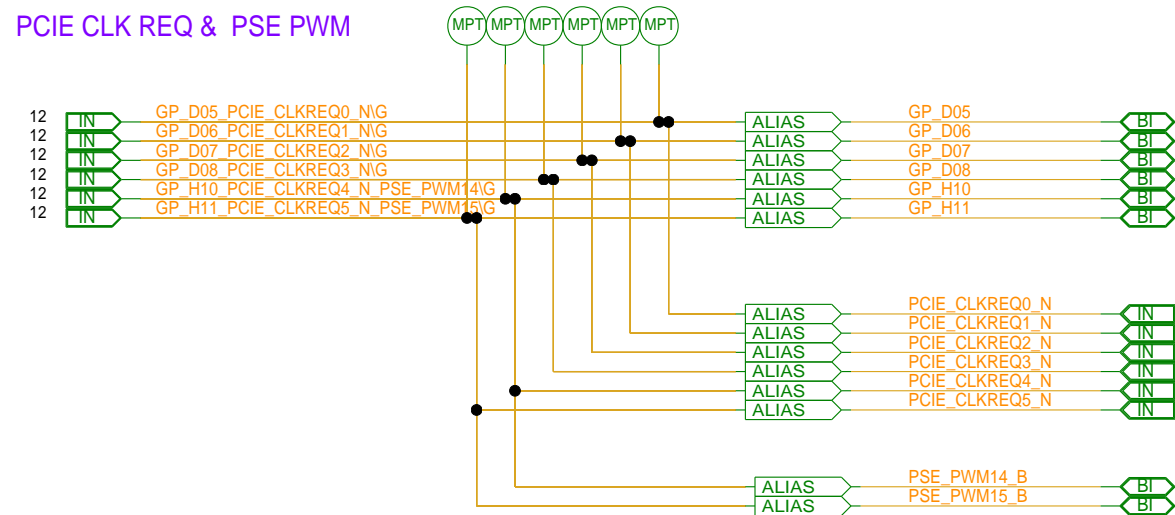
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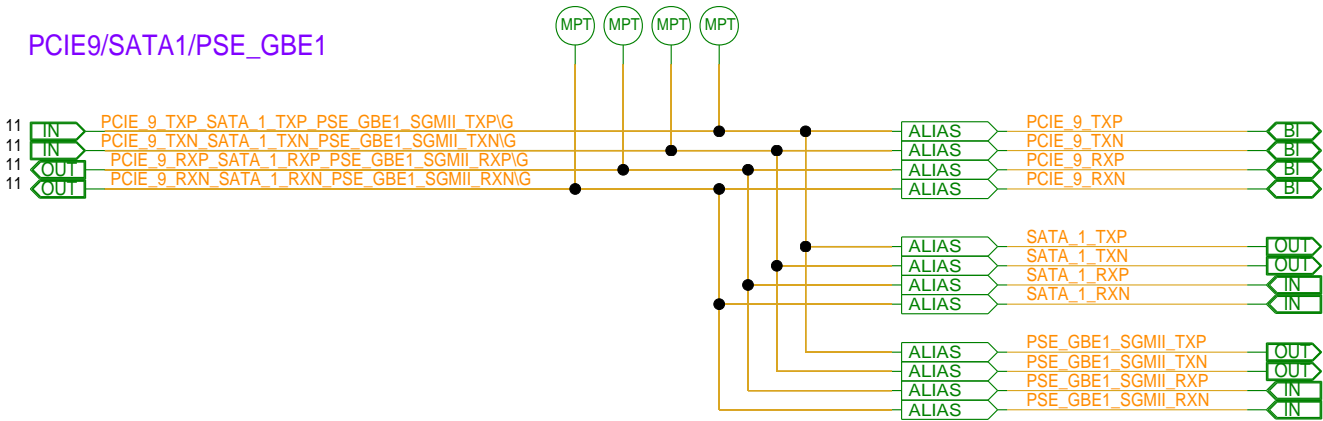
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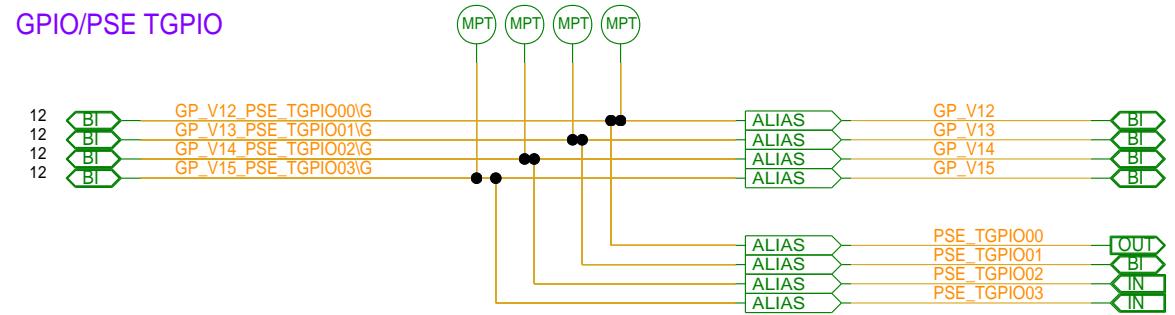
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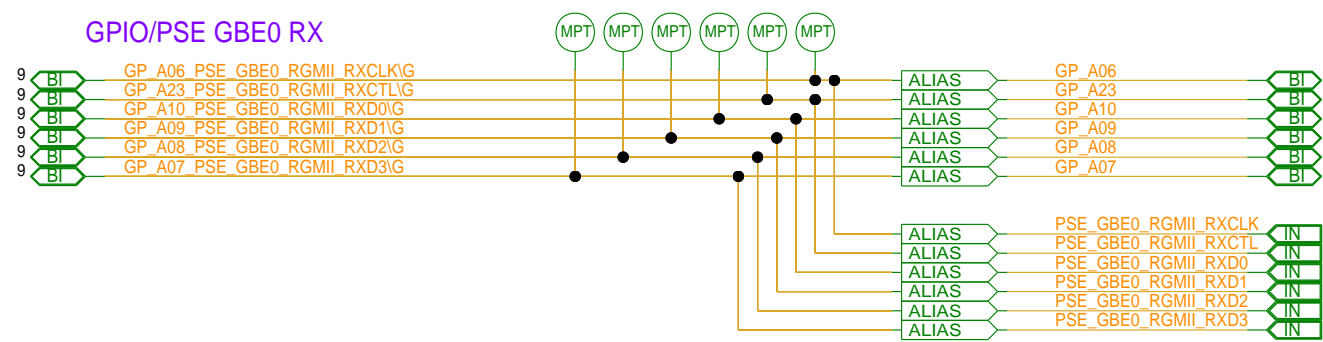
PCIE9/SATA1/PSE_GBE1



GPIO/PSE TGPIO



GPIO/PSE GBE0 RX

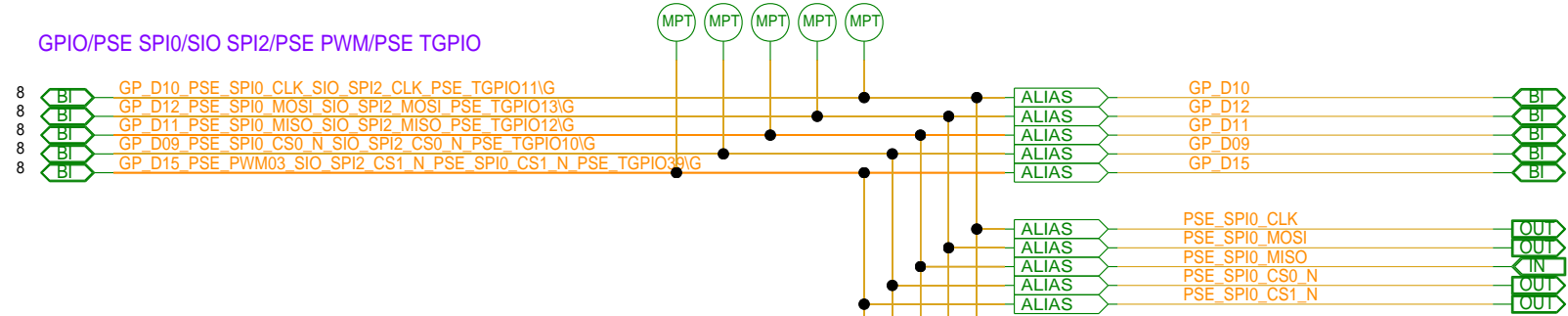


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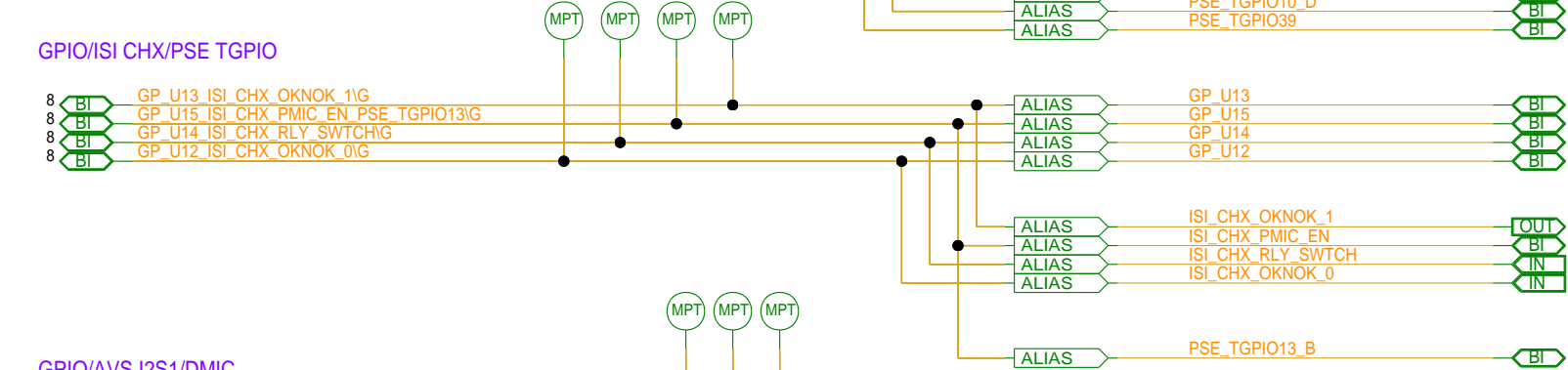
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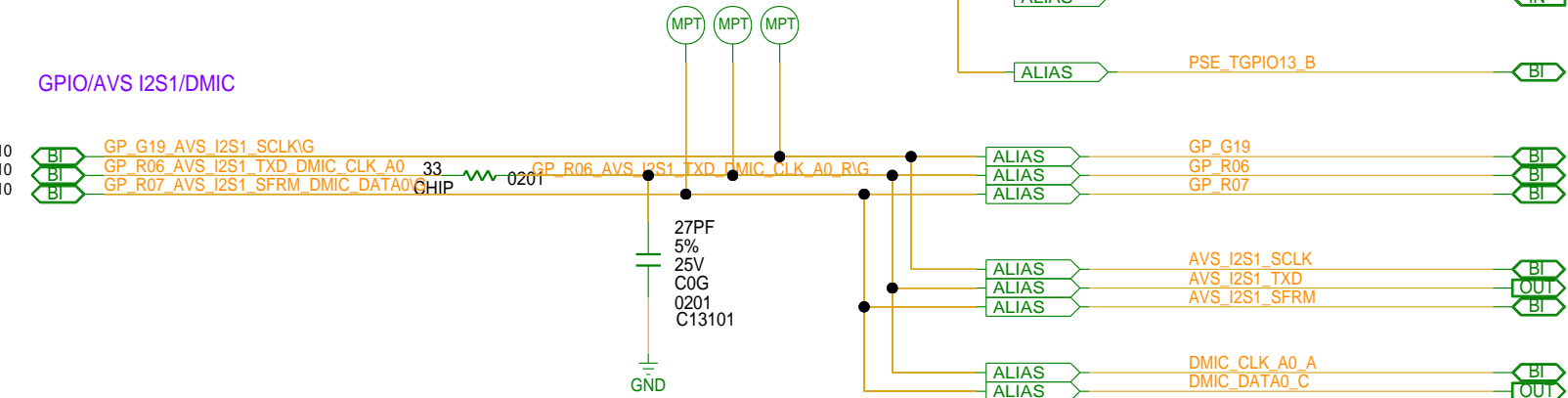
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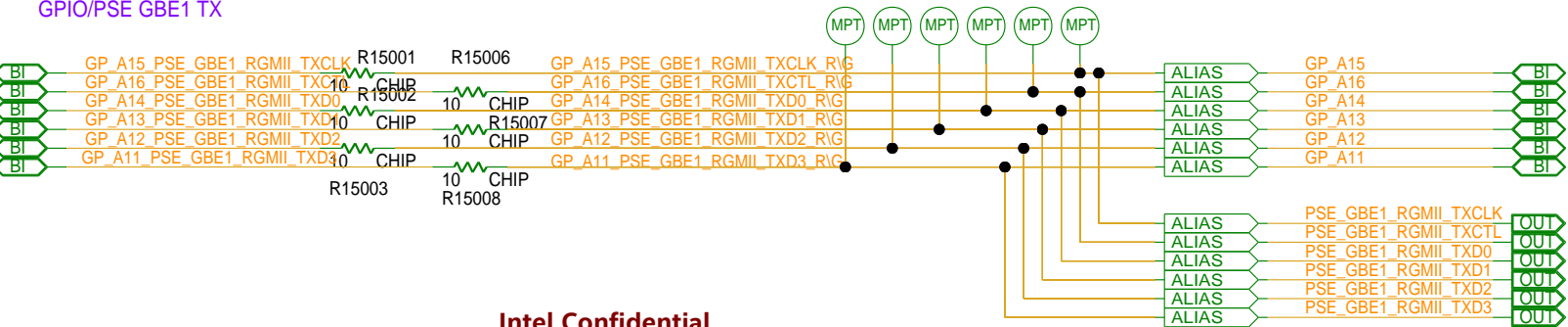
GPIO/ISI CHX/PSE TGPIO



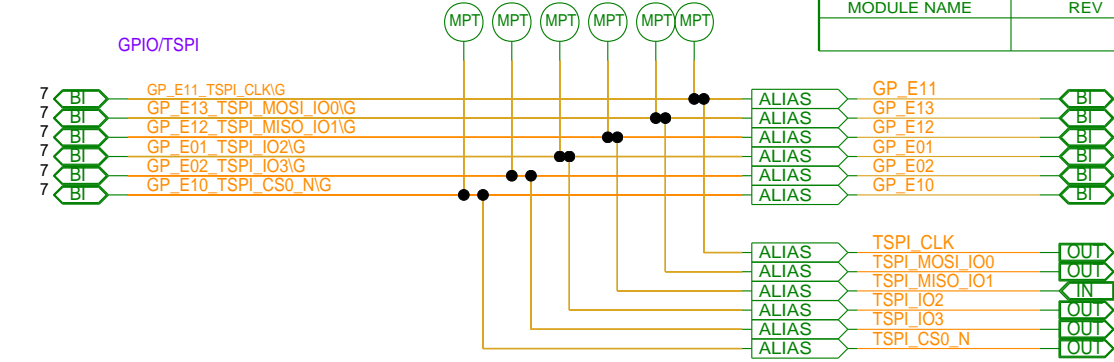
GPIO/AVS I2S1/DMIC



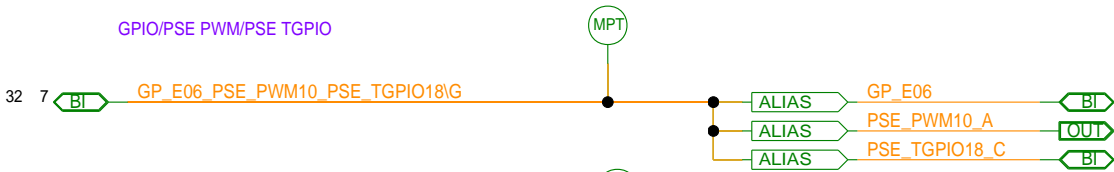
GPIO/PSE GBE1 TX



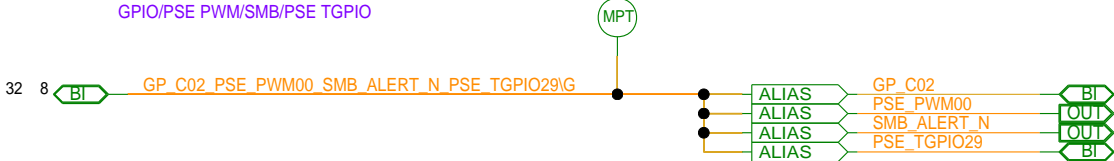
GPIO/TSPI



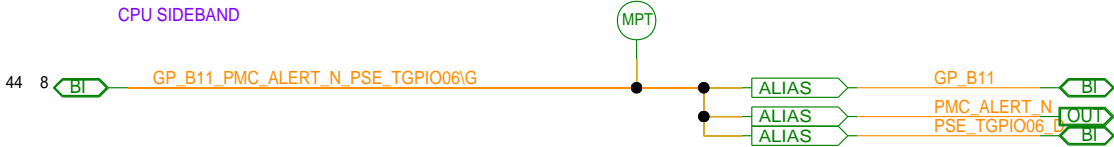
GPIO/PSE PWM/PSE TGPIO



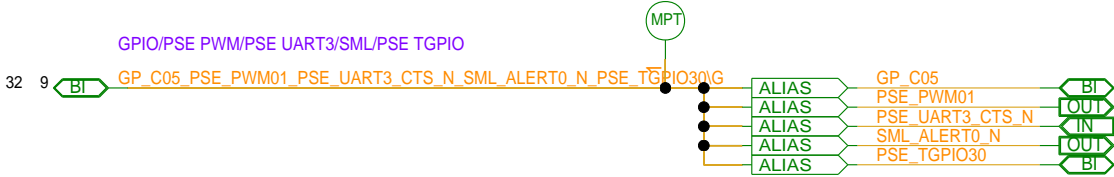
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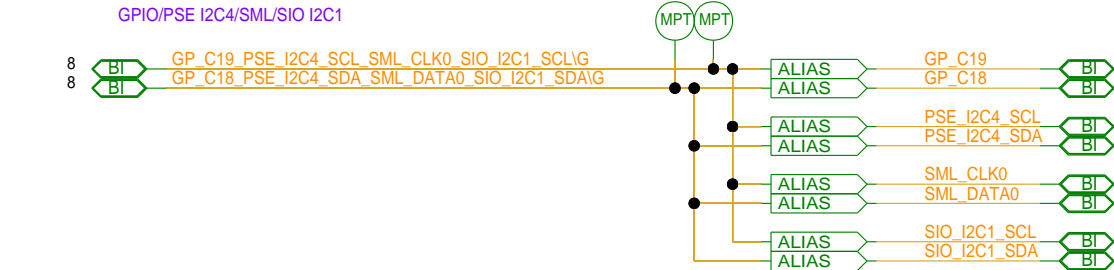
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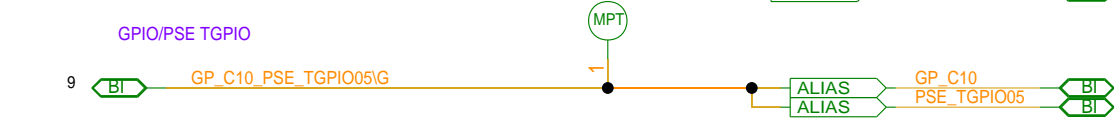
GPIO/PSE PWM/PSE UART3/SML/PSE TGPIO



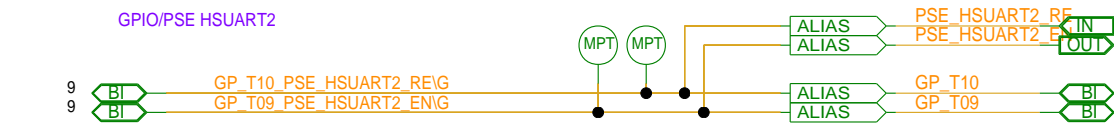
GPIO/PSE I2C4/SML/SIO I2C1



GPIO/PSE TGPIO



GPIO/PSE HSUART2



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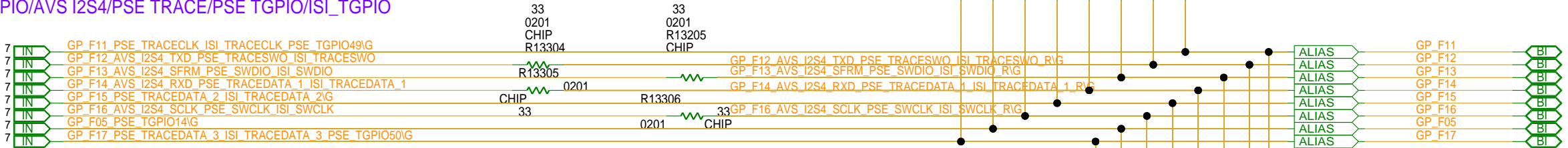


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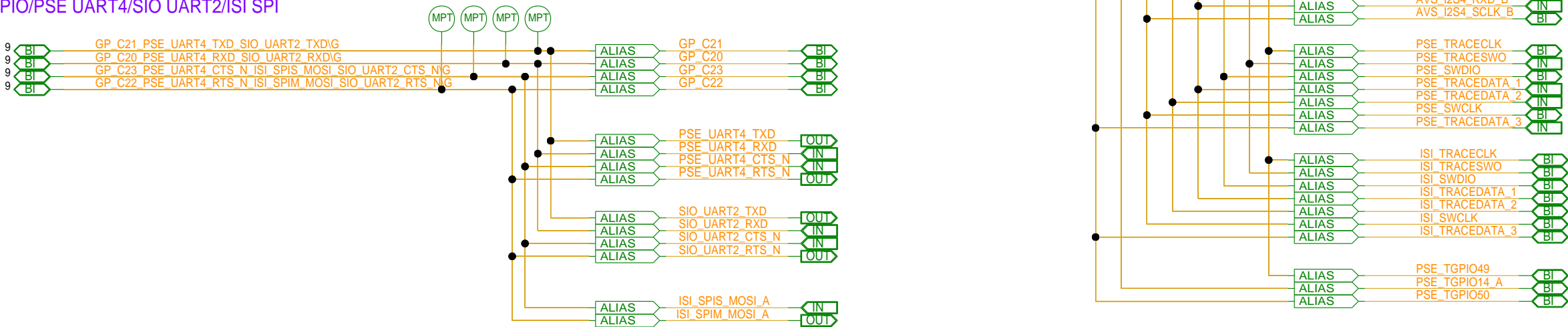
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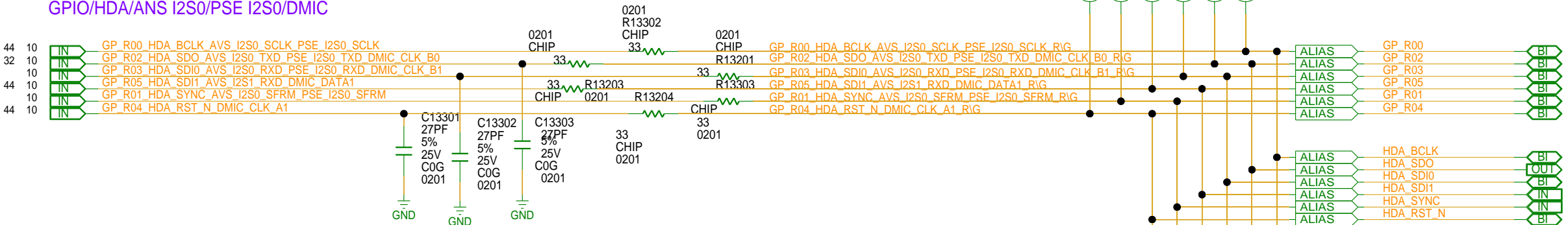
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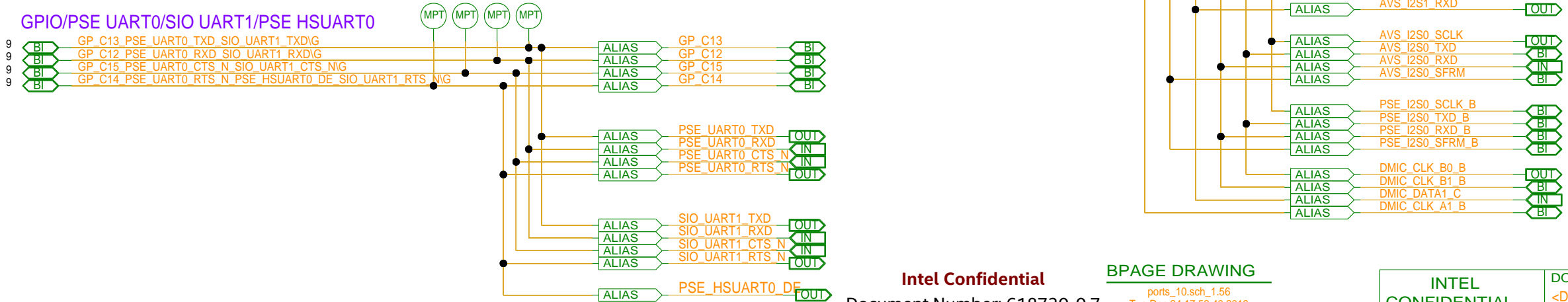
GPIO/PSE UART4/SIO UART2/ISI SPI



GPIO/HDA/ANS I2S0/PSE I2S0/DMIC

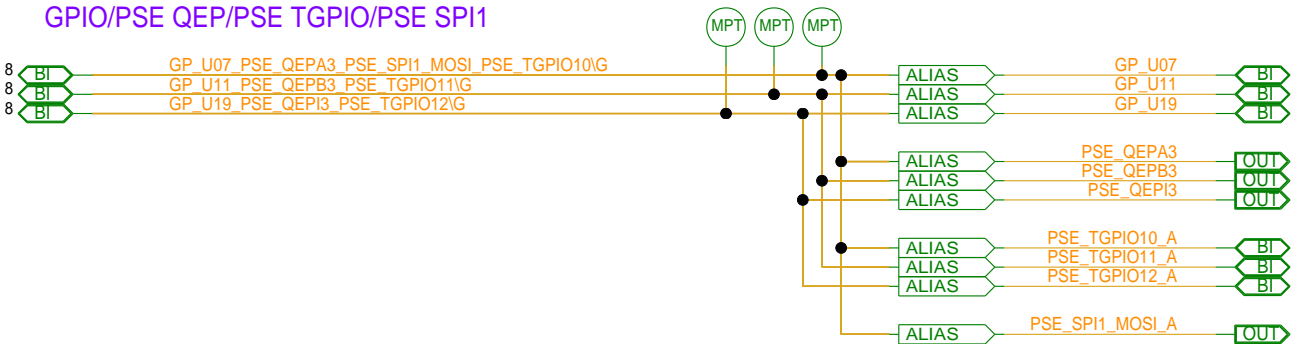


GPIO/PSE UART0/SIO UART1/PSE HSUART0

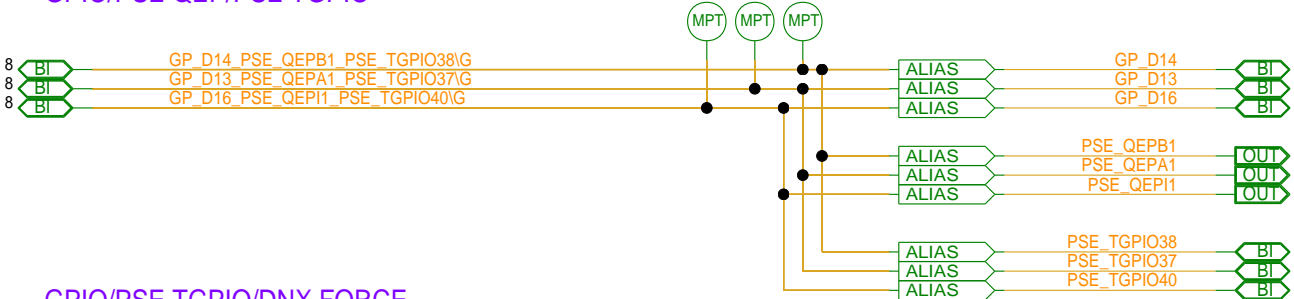


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GPIO/PSE QEP/PSE TGPIO/PSE SPI1



GPIO/PSE QEP/PSE TGPIO



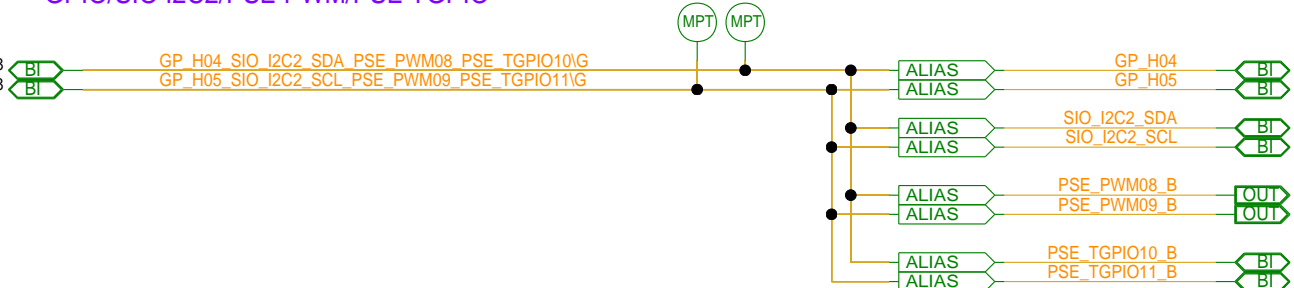
GPIO/PSE TGPIO/DNX FORCE



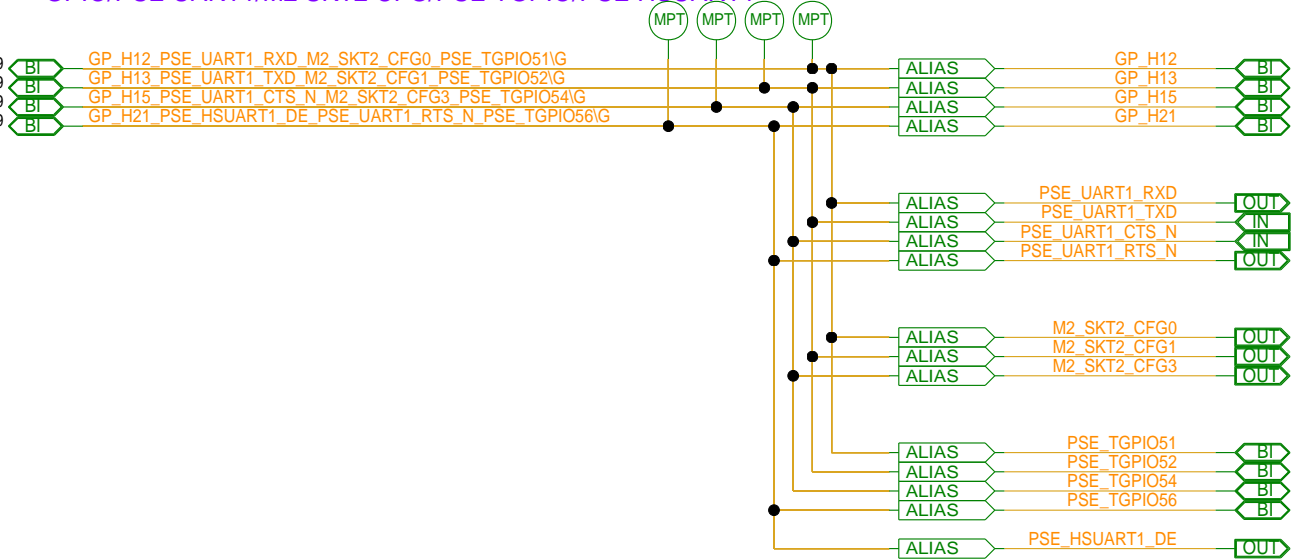
GPIO/M2 SKT2 CFG/PSE TGPIO



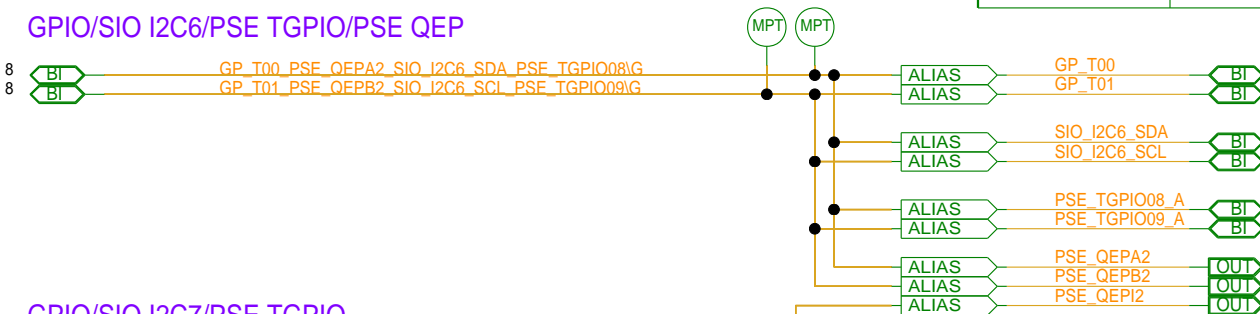
GPIO/SIO I2C2/PSE PWM/PSE TGPIO



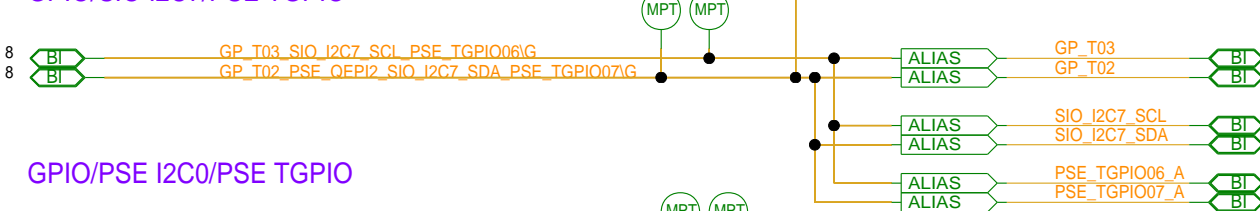
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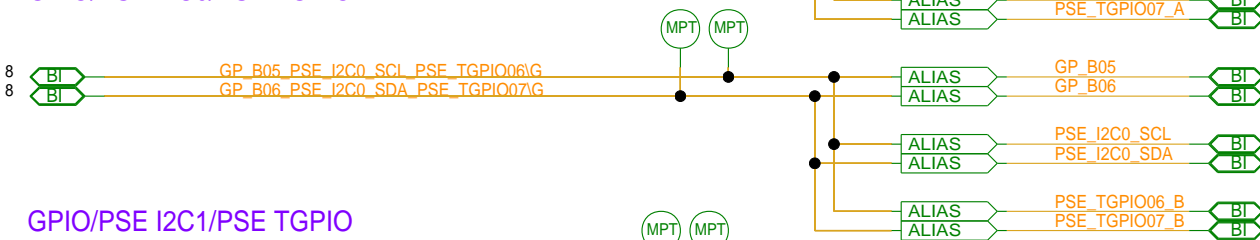
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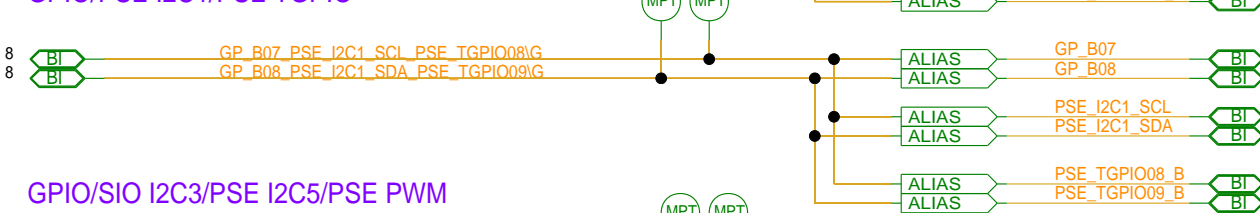
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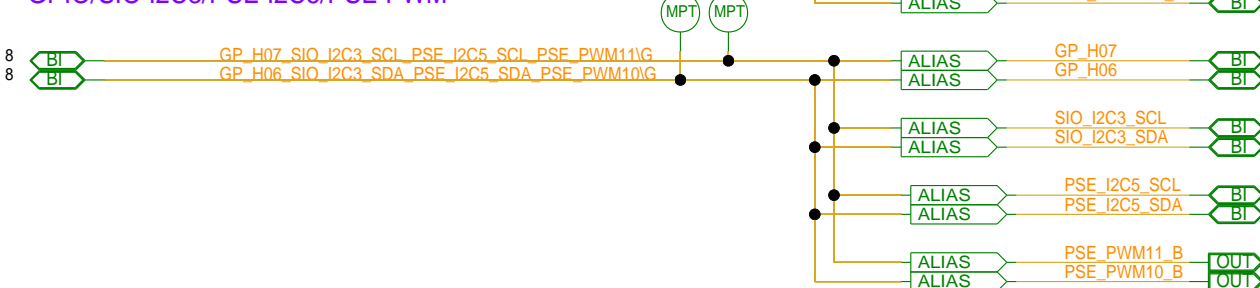
GPIO/PSE I2C0/PSE TGPIO



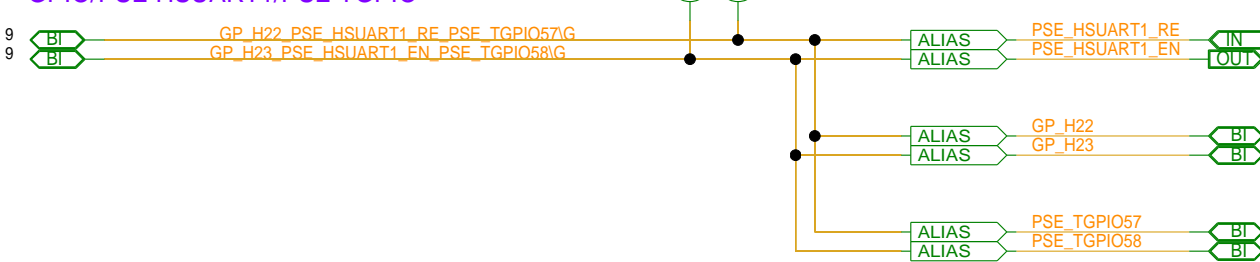
GPIO/PSE I2C1/PSE TGPIO



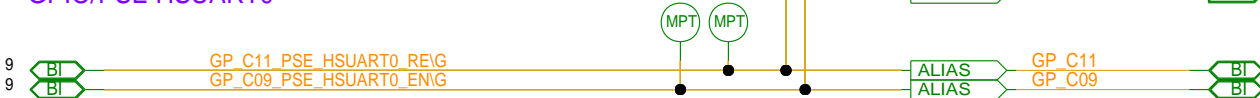
GPIO/SIO I2C3/PSE I2C5/PSE PWM



GPIO/PSE HSUART1/PSE TGPIO



GPIO/PSE HSUART0



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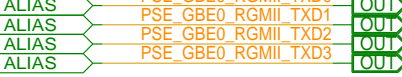
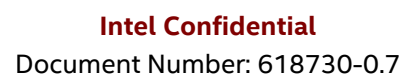
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