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Operating Instructions For Model LP-770

THREE FAMILY LOGIC PROBE

DESCRIPTION

This Kurz-Kasch Logic Probe is designed for fast servicing of integrated logic systems. With the unique multilamp readout at the probe tip, the LP770 visually displays the presence of correct logic levels by illumination of readouts marked "1" and "0". A LED marked "P" indicates pulses or logic transitions. An incorrect logic level, or open pin is shown by the absence of illumination.

Three (3) switches are provided, enabling the operator to select any one of three (3) factory programmed thresholds for use in servicing TTL, C/MOS, or HTL Logic Systems. The last switch selects stretch or memory.

GENERAL SPECIFICATIONS

1. Operating Power

Vcc	TTL	C/MOS	HTL
	4.75 to 5.5 VDC	5.0 to 15.0 VDC	12.0 to 15.0 VDC
Standby Current	35	B5 @ 5.0V 60 @ 15.0V	55
Max. Operating Current	50	50 @ 5.0V 75 @ 15.0V	70

2. Loading Factor

Load presented to circuit under test at logic "1" or "0" — 10 megohms (all modes)

3. Nominal Logic Voltage Response

	TTL	C/MOS	HTL
Logic "0" Lamp On	0 to 0.8V	0 to 30% VDD	0 to 1.5V
Logic "1" Lamp On	2.4 to Vcc	70% VDD to VDD	10.5V to Vcc

4. Overvoltage Protection at Probe Tip — 140 VDC continous

5. Power Lead Reversal Protection

Maximum Reverse Voltage — 100V

6. Power Lead Overvoltage

Overvoltage shut down protection operates at 16.0V — Protected to 50.0V

MEMORY/STRETCH

The slide switch near the tip of the probe permits pulse detection in either "stretch" or "memory" modes. In the "stretch" mode (switch off) the "P" indicator illuminated for 50 milliseconds in response to each single pulse (positive or negative going) of 10 nanoseconds, or greater, duration. In the "memory" mode (switch slide to mem. position) the "P" indicator is illuminated indefinately after the first pulse or logic transition, until reset by sliding the switch to OFF. To use the "memory" mode, first slide the switch to OFF, then connect the probe tip to the point being examined. This initial contact will cause the "P" indicator to flash. Following the initial "P" flash, the switch should be slid to mem. position. Now the probe is ready to operate in the "memory" mode.

GATING MODE

Probes with "gating" closely simulate a 2-input oscilloscope, in that two inputs are provided, and the "P" indicator will illuminate only when the gate input(s) are in coincidence.

THE PROBE IS PROVIDED WITH A PLUG-IN ASSEMBLY HAVING THE FOLLOWING ADDITIONAL LEADS:

Black Wire-Ground--Although this lead is common with the black power lead, it should be terminated at a ground point next to where the measurement is being taken. This is necessary for minimizing time delay. This lead should be grounded when testing high speed logic>50 MHZ.

White Wire-Gate Inputs--The maximum input at either of these leads should not exceed +5.5 VDC. Each input equals 1 - TTL load.

NOTE: The two white gating leads must be separated to avoid "cross-talk" falsely triggering the "P" LED.

TO CHECK PROBE

1. Connect black power lead to ground, red to VCC.
2. Touch probe tip to +Vcc, and "1" readout should be illuminated.
3. Touch probe tip to -Vcc, and "0" readout should be illuminated.

OPERATION OF THE PROBE

The "1" readout will remain illuminated only during the time period when logic level "1" is present at the probe tip. Similarly, the "0" readout will remain illuminated only during the time period when logic level "0" is present at the probe tip. The "P" readout will illuminate as the result of a transition in logic levels. Therefore, typical operating situations likely to be encountered are as follows:

1. With probe tip touching symmetrical clock source, "0" and "1" indicators will both be illuminated at one-half brilliance, and "P" indicator will be illuminated at full brilliance.
2. With probe tip touching positive-going high-speed pulses of short duty cycle, "0" and "P" indicators will be illuminated, "1" indicator will be illuminated on duty cycles greater than 10%. An indication of symmetry can be obtained from the relative brilliance of the "0" and "1" indicators.
3. With probe tip touching negative-going high-speed pulses of short duty cycle, "1" and "P" indicators will be illuminated, "0" indicator will be illuminated on duty cycles greater than 10%. An indication of symmetry can be obtained from the relative brilliance of the "0" and "1" indicators.

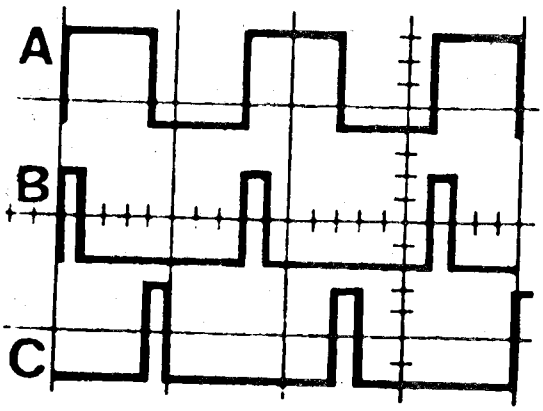

FIGURE 1

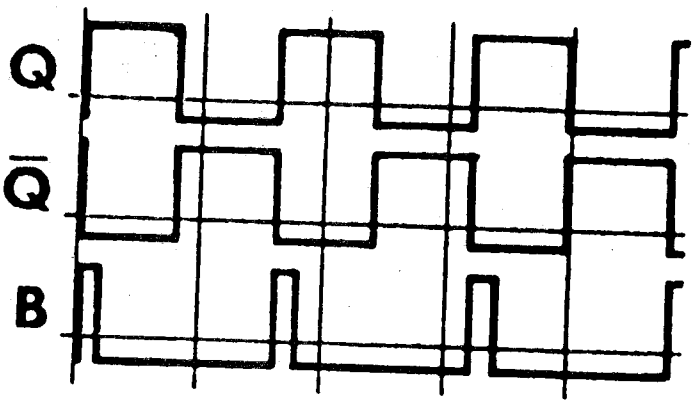

FIGURE 2

TYPICAL OPERATION OF THE GATING FEATURE

A. In Figure 1 above, "A" is the input to one of the white gating leads.
B. If "B: is the input to the other white gating lead, the "P" lamp will be illuminated indicating coincidence.
C. If "C" is the input to the other white gating lead, the "P" lamp will not be illuminated indicating non-coincidence.

USE OF THE GATING FEATURE TO VERIFY TIMING RELATIONS

A. Figure 2 represents a typical digital system with square wave as flip-flop output "Q" and "$\bar{Q}$". "B" is generated each time "Q" goes positive. This relationship may be verified by connecting one input gate (white wire) to flip-flop "Q" and using the second input gate (other white wire) at "B" as follows:

1. Connect one white gate lead to "Q" on flip-flop.
2. Connect other white gate lead to "B" in circuit.
3. "P" indicator will be illuminated verifying that during the time "Q" and "B" are positive the two pulse trains are in coincidence.
4. Reconnect the gate lead that was connected to "Q" in step 1 on previous page to "$\bar{Q}$" and repeat step 2.
5. The "P" indicator will not be illuminated verifying that "B" is not generated during the time "$\bar{Q}$" is positive or non-coincidence.

USE OF THE GATING FEATURE IN PHASE TESTS

1. Refering to Figure 2, connect one of the input gates (white lead) to "Q".
2. Connect the input of the other gate (white lead) to "$\bar{Q}$".
3. The "P" lamp will not be illuminated indicating 180 degrees out-of-phase relationship between "Q" and "$\bar{Q}$".