NANOFAST

INSTRUCTION MANUAL

FOR

THE 536B TIME INTERVAL METER

NANOFAST, INC.
416 West Erie Street
Chicago, Illinois 60610
PHONE: 312 - 943 - 4223

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MODIFICATIONS TO THE SMITHSONIAN
536B TIME INTERVAL METERS
SERIAL NUMBERS 1834, 1835 & 1836

1. The range of the 536B Time Interval Meters were extended on both the high and low ends to provide a full scale reading of 999,999,999.97 nanoseconds. In addition to the 1/10thsNS digit which reads in 10th nanosecond increments, the 100th NS position reads either 0. 2. 5. or 7 corresponding to readings of .000, .050 and .075.

2. The reset input on the front panel accepts positive 10 microsecond wide Reset pulses occurring at least 100 microseconds before the start pulse.

3. Separate start and stop control gates for the start and stop channels are brought out to rear panel BNC connectors. If these pins are left open or grounded the start and stop channels are open. If the pins are returned to +3 the channels are closed.

4. Positive going trigger monitor pulses occurring nominally 60 NS after the inputs are available on rear panel BNC connectors for the start and stop channels. The outputs go from ground to approximately +2.5 volts when driving a 500 ohm load.

5. When overflow occurs the left hand neon turns on, the unit stops and in addition does not reset but holds a consistant identifiable number.

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GENERAL DESCRIPTION

1. The 536B Time Interval Meter is a high resolution Time Interval Meter with a resolution of 1/10th nanosecond and a range of 9,999,999.1 nanoseconds. Additional or fewer digits may be optionally selected. The 536B Time Interval Meter measures the time from the occurrence of triggering on the start input to the occurrence of triggering on the stop input when measuring between separate start and stop inputs. If pulse width or period are being measured equivalent start and stop signals are produced by the Plug-In and provided to the Time Interval Meter.

2. The 536B Time Interval Meters accept all the Standard Time Interval Meter Plug-Ins including the A3, B3, 1/2 Max, etc.

3. The proper sequence of operations for the Time Interval Meter is first of all, receipt of a reset pulse, then a start pulse and then a stop pulse. The reset pulse may be generated either manually by the actuation of the front panel push button, or externally by providing a six volt 10 microsecond negative reset pulse to the reset BNC on the front panel, or automatically by placing the reset switch in automatic. The reset selector switch selects the manual, automatic or external reset positions. The manual push button however, operates in all positions. The display con-

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trol in the upper righthand corner when provided, controls the time of visual display and binary coded decimal readout before reset when the unit is in automatic reset. The display operates only when the reset switch is in the automatic position.

4. In normal operation, then, an external reset pulse is applied to the reset input and external start and stop pulses to the start and stop inputs. The unit will then display and provide at the rear readout connector the value of the time between the detection level of the start and stop pulses and will hold this until the unit is reset once again. In this mode of operation then the proper sequence of reset, start and stop always occurs. One may also apply start and stop pulses either singley or repetitively to the start and stop inputs and place the reset switch in automatic or manual. The unit will usually read the proper number. However, since the reset may occur between the start and stop pulses an occasional reading will not be correct in this mode of operation.

5. After an initial reset the time between the first start and stop pulse is measured, then successive start and stop pulses are locked out until another reset signal is provided either manually or automatically. The start

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and stop pulses are gated on when the rear Jones Terminal "Gate" input is at zero volts or open, and are gated off when the input is at +3 volts. Accordingly, this feature allows one to select a given start and stop pulse from a continuous train of start and stop pulses. Gate response time is better than 20 nanoseconds.

6. For test purposes a set of test pulses are created on two rear BNC's. The test pulses are actually identical pulses split on two identical internal coaxial cables. The two pulses may be brought to the front start and stop inputs on equal length coaxial cables and the input Plug-In may be set up to detect the two pulses. The pulses rise from approximately -.3 of a volt to approximately +2.5 volts with a rise time of 10 to 15 nanoseconds, and with somewhat of a slope at the top of the pulse. The pulses are created immediately after the unit resets and accordingly the unit may then be placed in the automatic position and started once and then run continuously. Eventually then the unit will be reset, the two pulses will be created, the time between the two will be measured and displayed on the Nixies, and the unit will then hold the display until the display circuitry times out, in which case the unit will automatically be reset to zero and another set of pulses created.

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OPERATING PROCEDURE

1. Plug the line cord of the Time Interval Meter into a 115 volt 60 hertz power line. Allow 30 minutes for warmup. Connect the start and stop inputs to the test pulse BNC connectors at the rear of the unit through equal length coaxial cables.

2. For checkout, using the internal pulses, place the slope switches in positive and position the start level potentiometer and the stop level potentiometer at approximately 20 degrees clockwise from the vertical. Place the reset switch in automatic and push the manual reset button once. The unit will read the difference in time between the discrimination level on the start and stop channels. This should be close to Zero. Adjust the stop potentiometer a little bit one way or the other so that the unit reads .1 nanosecond and Zero. Since the digital resolution of the unit is 1/10 nanosecond the unit can read a given reading to within 1/10 nanosecond. Delay lines may be then added to the stop channel or the rise time of the pulses may be checked by varying the stop discrimination level.

3. For use with external pulses, reset the unit either by applying an external negative six volt reset pulse, 200 microseconds or more before start, or reset automatically or manually if slow or single shot operation is

consistent with the rate of the start and stop pulses to be applied externally. Then place the start and stop slope switches and level setting potentiometers at the desired triggering level. Apply the input start and stop pulses to the input start and stop BNC's respectively. If the inputs have undesired DC components they may be AC coupled. As an example, the DC pulses may be riding on a +2.5 volt DC level on x1, since the inputs are DC they will saturate and thus obscure the input pulses. Before the desired start and stop transitions occur, the DC level of the start and stop input signals must be smaller than the required triggering level. Apply the external start and stop triggering pulses or transitions. The Time Interval Meter will measure and visually display the time between the discrimination level of the start signal and the discrimination level of the stop signal. If after being reset a start signal is applied within a time equal to full scale, the over-run light at the left of the Nixie display will turn on indicating over-run has occurred. If the stop pulse is applied and no start pulse is applied the Nixies will read an arbitrary number and the unit must be reset again before the next reading is made.

4. The Basic clock used may be either the internal 10 MHz crystal, or optionally, an external 1 MHz source, or an external 10 MHz as selected by the

optional rear panel switch. The 1 MHz and 10 MHz rear panel inputs require 1 volt RMS sinewave with noise down greater than 70 DB into 50 ohms.

5. If no stop occurs, or if the stop occurs after full scale, the over-run neon at the left of the display will turn on. If the stop occurs before, but within 10 nanoseconds of the start, the negative neon, at the left of the display, will turn on.

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DETAILED DESCRIPTION

1. The 536B Time Interval Meter measures the time between the occurrence of detection on the start input channel and the occurrence of detection on the stop input channel. The 536B operates by turning on and off a high speed binary with signals derived from the start and stop input signals. The binary then gates on and off a stable crystal oscillator for a period of time proportional to the time between the start and stop inputs. In addition the time between the leading edge of the start pulse and the next clock pulse that occurs and the time between the leading edge of the stop pulse equivalently and the next clock pulse that occurs are measured and respectively added to and subtracted from the main measurement.

2. The board layout, circuitry etc. of the 536B Time Interval Meter are shown on the 536B block diagram and the schematics. In addition the input and output waveform of all boards are shown on the waveform sheet. The Time Interval Meter system signal waveform sheet shows the basic operation of the unit. The Time Interval Meter is initially reset either manually, externally or manually creating a positive Reset pulse that goes from approximately -4 to +3 volts and resets all the counters, binaries in the system. The Reset pulse appears at pin 29 of the Reset board. Approximately 100 microseconds later a Recycle pulse occurs on pin 31 of the Reset Board. This is a positive pulse going from -1 to +3 volts. The Recycle pulse opens up the lockout gates for the start and stop channels so that input signals will be accepted but will not be accepted during the time that the Reset pulse is resetting binaries, decades etc. As indicated in the system signal waveforms a start and stop signal is then applied to the start and stop inputs of the Time Interval Meter. The major portion of the time between the start and stop signal is then counted in units of 100 nanoseconds with the 10 megahertz clock signal appearing on pin 6 of board 9 and as shown on the system signal waveform. In addition the time between equivalently the leading edge of the start signal and the first negative 10 megahertz clock transition that occurs after the start signal is measured and added to the basic time that is measured in units of 100 nanoseconds. Also the time between the leading edge of the stop signal and the next negative transition of the 10 megahertz clock that occurs is measured and subtracted from the basic measurement made in units of 100 nanoseconds. The times between the start and the first clock transition and the stop and the

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next clock transition and the basic long period timing signals is shown on the system signal waveform sheet.

3. The 10 megahertz clock signal is derived from the Internal or External Clock on the Clock Board and applied to pin 6 of the Control Board. The timing signals for the Control Board are shown on the Control Board signal waveform sheet. The 10 megahertz clock is a zero to +3 squarewave appearing at pin 6 of the Control Board. Binary B1 of the Control Board consisting of transistors Q3 and Q4 and associated input transistors controls the basic long term time measurement. Binary B1 is initially reset by the R1 or positive Reset Pulse of the Time Interval Meter. When the start input pulse is detected a positive going 0 to +3 volt pulse appears on pin 5 of the Control Board. Binary B1 then thru the following inverter, enables the transistor gate consisting of transistors Q9 and Q10. When the stop pulse occurs a positive 0 to +3 volts pulse appears at pin 3 of the Control Board and actuates a 200 nanosecond monostable delay. At the end of this time the delayed output turns off binary B1 thus stopping the count. Because of the added 200 nanosecond delay an additional 2 counts of 100 nanoseconds each are counted by the system. The following binary B2 and B3 are used to subtract the first two counts that occur so that the overall count to the system is proper. The final gated output from the Control Board appears on pin 27 and is shown on the waveforms for the Control Board. The signal goes from 0 to +3 at a 10 megahertz rate. The Control Board is used for a variety of other indications. If there is no stop pulse the unit will run over and the positive transition from the last counter will be applied to pin 28 of the Control Board. This signal will flip the overflow binary consisting of integrated circuit I5 and will actuate the overflow neon and cause a positive nominal 3 volt level to appear on pin 48 of the rear panel connector. The neon drive is a high voltage transistor with bias so that the neon does not light until the transistor is actuated. In addition the output of the overflow binary drives a monostable consisting of resistive and capacitively cross coupled stages in integrated circuit I6. The output of the monostable is then inverted and drives pin 27 of the Reset Board thus causing reset of the overall system except for the overflow binary and those stages enabled by the Recycle signal. Accordingly the unit will remain in the overflow condition with the input gates closed until an external, manual or automatic Reset

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pulse is again applied to the Time Interval Meter. In addition after the end of the measurement binary M3 consisting of resistively cross coupled stages in integrated circuit I4 is actuated creating a +3 volt approximately 200 microsecond wide print command that appears on pin 8 of the Control Board. This signal drives pin 45 of the rear panel 50 pin Amphenol connector.

4. The basic clock signals for the Time Interval Meter are provided by the Clock Board. The input to the Clock Board is either the internal 10 megahertz oscillator in a porportional oven or an external 10 megahertz signal or an external 1 megahertz signal. The inputs are selected by the rear panel 3 position switch. The 3 position switch is a two pole 3 position switch selecting either the external 1 or 10 megahertz or the internal 10 megahertz. The external 1 and 10 megahertz are applied thru the rear panel BNC connectors. The external inputs should be a minimum of 1 volt RMS into 50 ohms with noise down at least 40 DB.

5. In the external 1 megahertz position the signal is applied to emitter follower Q35. The output of Q35 drives the following amplifier, Q34 which squares the input signal. The signal is then buffered by the following emitter follower Q33 and further squared in the stages consisting of Q32 and Q31. The large amplitude signal swinging from ground to close to +15 is then buffered by Q30 and applied to 3 series tuned circuits. The 1st & 2nd tuned circuit filters out the 1 megahertz and 3 megahertz components of the squarewave while the last tuned circuit provides a high impedance for the 5 megahertz component of the original 1 megahertz squarewave applied to the filter string. The 5 megahertz is buffered by Q29 and applied to amplifier Q45 whose collector is tuned to 5 megahertz. The resulting 5 megahertz sinewave is buffered by Q44 and applied to the differential amplifiers Q43 and Q42. The collectors of Q43 and Q42 consist of clipped inductive loads which create short pulses 180 degrees out of phase at a 5 megahertz rate. The 2 signals 180 degrees out of phase are then buffered by emitter followers Q41 and Q40 and then are applied to the doubler circuit consisting of Q38 and Q39. The collector of Q38 and Q39 is tuned to 10 megahertz. The resulting input signal drives the 10 megahertz load producing

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a 10 megahertz sinewave. The 10 megahertz is buffered by Q37 and then drives the following 10 megahertz filter. The LC filter at 10 megahertz is buffered by Q36. The output of Q36 is then applied via pin 30 to the rear panel 1 megahertz external switch. Accordingly the second pole of the rear panel 1 megahertz switch is actually driven by a 10 megahertz signal when in the 1 megahertz position.

6. When the 3 position switch is in the 10 megahertz external the externally supplied 10 megahertz signal is utilized. When the switch is in the 10 megahertz internal the signal is derived from the internal porportional oven containing the internal 10 megahertz crystal controlled oscillator. The oscillator consists of a single stage crystal controlled oscillator whose output is buffered by an emitter follower and applied to the appropriate position of the rear panel switch.

7. In each of the positions then the second pole of the rear panel switch selects a 10 megahertz approximately 3 to 5 volt sinewave input. In the 10 M internal position the signal at pin 5 of the Clock Board is a sinusoidal 10 megahertz signal going from -4 to +1 volt.

8. The input at pin 5 of the Clock Board is then buffered by the following emitter follower, Q4 which in turn drives the following 10 megahertz filter. The resulting sinwave is buffered by the emitter follower Q5 and then applied to the differential amplifier consisting of Q6 and Q7. The resulting squarewave at the collector of Q7 is divided down and buffered in emitter follower Q8 and applied to Q9 arranged as a switch. The output of Q9 drives Q10 and the emitter follower Q14. Q14 drives the following LC delays which in turn drive transistor Q15 arranged as a switch. The output of Q15 is inverted once again in Q16 and applied to the emitter follower Q17. Q17 provides a 0 to +3 volt 10 megahertz squarewave at pin 19 for driving the remainder of the system.

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9. In addition Q10 which was also driven by Q19 drives emitter follower Q11 and the following emitter follower and Q12 and Q13 arranged as a emitter follower and switch respectively. The output of Q13 drives Q1, Q2 and Q3 which provide 25% duty cycle pulses going from approximately +4 to 0 volts. These appear on pins 6, 4 and 3. In addition the output of Q9 drove emitter follower Q28 which in turns drives the differential amp consisting of Q27 and Q26. The differential amp has inductive loads in both collectors which are clipped by fast diodes. The resulting 10 megahertz positive pulses are 180 degrees out of phase within each other and are applied to emitter followers Q25 and Q22. Q25 and Q22 drive the following push pull amplifier consisting of Q23 and Q24. Q23 and Q24 drive a 20 megahertz tuned circuit in their collector. The resulting 20 megahertz signals is buffered by emitter follower Q21 and applied to inverters Q20 and Q19. The output of Q19 drives the emitter follower Q18 which in turn provides the 50% duty cycle 20 megahertz continuous signals going from approximately +3 volts to ground and appearing at pin 20 of the Clock Board.

10. The 536 line of Time Interval Meters accepts a wide range of Plug-Ins. Some of the Plug-Ins require a Recycle signal. The Recycle signal going from -1 volt to +3 volts and then decaying expendentially appears on pin 4 of the Plug-In 24 pin connector. After reset a start and stop input are usually applied to the Plug-In. The resulting start output appears on pin 23 of the Plug-In 24 pin connector. The start signal is a negative going signal starting at +2 volts and going to -2 volts with a width of approximately 3 microseconds. Similarly the stop output is a negative signal going from +2 to -2 volts and with a width of approximately 3 microseconds. as shown on the Plug-In waveform sheet. The propagation time between the application of the start input and the occurrence of the start output and the application of the stop input and the occurrence of the stop output are both stable and fixed.

11. The start and stop signals after passing thru short delays on the Delay Board or Board One drive the start and stop gates located on the 3S1 and 3S2 Boards. The gates composed of transistor stages Q1, Q2, Q3 and Q3A are enabled by negative signals. In addition to the input signals the

start and stop gates are enabled by the lockout binary for each of the start and stop channels, the prime binary for both the start and stop channels and an optional external gate. The external gate control is available at the rear panel Jones Terminal strip. If the input is left open or is returned to 0 volts the gate is open. If the gate control level is brought to +3 the gate is closed. Normally both the start and stop gates are controlled by a single input. Optionally separate controls for the start and stop channel gate may be provided.

12. The lockout binary for the start and the stop 3S1 Boards are turned on by the Recycle pulse as shown on the waveform for the 3S Board. The Recycle pulse occurs approximately 100 microseconds after the internally, manually or externally generated Reset pulse. The lockout binary consisting of Q30, Q31, Q32, Q33 and Q34 is turned on by the Recycle pulse and provides an enabling signal after reset. This signal persists until after the occurrence of a gated start and a gated stop individually for both channels. When all of the gate inputs are enabled and the start or stop pulse occurs a positive signal occurs at the collector of Q1 of the input gate. This positive signal is buffered in emitter follower Q4, Q5 and Q6. The positive output from Q6 drives Q33 thus turning off the lockout binary. This occurs after a delay determined by the RC network into Q34. Accordingly within 100 to 200 nanoseconds after the occurrence of the gated start or gated stop the lockout binary closes the input gate and thus inhibits the measurement of any other sets of starts and stops until the unit is reset again. The response time of the start and stop input gates to an external signal is between 10 and 15 nanoseconds. Accordingly this feature can be used for measuring phase, measuring exact set of pulses out of the repetitive train etc.

13. The Converter Boards are reset by the R1 positive reset except for the prime binary. The prime binary is located in the stop Converter Board. The prime binary is reset by the Recycle pulse to an off condition. Accordingly a positive level appears at pin 6 of the stop Converter Board and drives the start and stop input gates on the start and stop 3S1 and 3S2 Boards respectively. On occurrence of a start pulse the negative transition from pin 10

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of the Delay Board drives pin 8 of the stop Converter Board. This signal is differentiated and in turn flips the prime binary consisting of transistors Q1 thru Q6 on the Converter Board. Accordingly the start and stop input gates are then enabled if the rear panel enable input is either open or at 0 volts. Accordingly a gated start or stop output will appear at pin 10 of the 3S Boards. The gated output is a fast rising pulse from 0 to +4 volts with an exponential decay. In addition a positive 3 volt signal is applied to the Control and Converter Board. The gated outputs also close the lockout binary so that the start and stop gates are closed after detection of the start and stop independently. The Converter Boards produce a pulse going from 0 to +4 volts and appearing at pin 23 which are porportional to the time between the initiating signal and the 10 megahertz edge that is gated in the Control Board. These signals are applied to the UD1 Board. The 20 megahertz squarewave signal derived from the Clock Board is also applied to the UD1 Board on pin 9. This signal goes from 0 to +3. The add and the sub inputs to the UD1 Board are combined in such a way that a count is obtained only for add and not sub. The resulting signal gates the 20 megahertz input from pin 9.

14. The positive going add signal on pin 6 of the UD1 Board and the inverted subtract signal on pin 8 of the UD1 Board are applied to the following "and" circuit in integrated circuit I1. Similarly the subtract and the inverted add is applied to the "and" circuit in integrated circuit I1. Accordingly the digital result is add and not subtract or subtract and not add. After inversion these outputs then provide the gating signal for the inverted 20 megahertz input on pin 9 of the UD1 Board. The resulting outputs are then further shaped and the gated 20 megahertz signal of either one drives the following "and" circuit in integrated circuit I3. This gated output then drives a following binary which toggles on every transition. In addition the outputs by-pass the binary and are selected by the binary having previously been in a 0 or 1 state. This is repeated three times resulting in a division by 8. The resulting signal is then applied to the divide by 10 circuit in integrated circuit I10. I10 provides carry and borrow signals to the next board. To compensate for 0 and differences of delay between the start and stop channels the least significant digits on the UD1 Board are pre set to numbers that are selected such that the 0 actually is 0 when identical pulses are applied to the actual input of the unit. For the original

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0 calibration of the unit a pre set number is selected for the divide by 10 circuit by wiring a jumper to ground to one of the 10 2.7k's located in a row on the UD Board and shown in a circular pattern on the schematic. The pre set number is in a decimal form. 0 thru 9 may be selected by a unsoldering the jumper to ground and connecting it to the selected number. Accordingly if the number 7 is desired the wire to ground is unsoldered and tacked on to the number 7 resistor. The outputs of the resistors are applied to integrated circuits I11, I12, I13, etc. in accordance with the small letters shown on the schematic. Effectively the 10 line representation is converted to a 1-2-4-8 binary coded decimal form by the "and" circuits shown. The resulting 1-2-4-8 binary coded representation is then provided as a parallel input to the decade and loaded into the decade as a pre set number on the occurrence of the system reset. The parallel 1-2-4-8 binary coded decimal number that finally remains in the board appears on pin 27, 28, 29 and 30 and drives the corresponding high voltage nixie drive integrated circuit on the front panel DDNT Board. In addition the 1-2-4-8 binary coded decimal output to the rear panel appears on pins 1, 2, 3 and 4 of the board. The two most significant bits of the divide by 8 circuitry are also decoded to provide a 0, .25, .50 and .75 representation for driving display and readout if desired. These appear on pins 23, 22, 21 and 24.

15. The carry and borrow outputs of the UD1 Board on pins 25 and 26 then drive pins 6 and 8 of the next most significant UD Board. In this board the divide by 8 circuitry is omitted and the carry and borrow signals drive the decade directly. The decade is also reset as desired from 0 thru 9 by soldering the jumper wire to the appropriate one of the 0 thru 9 decimal coded 2.7k resistors located in a line. The 10 line decimal code is converted to 1-2-4-8 binary coded decimal in I11, I12 and I13 and applied as a parallel BCD input to the decade. The decade divides the input by 10 and provides carry and borrow signals on pins 25 and 26. The front panel 1-2-4-8 binary coded decimal signal to the display drive integrated circuit appear on pins 27, 28, 29 and 30. The 1-2-4-8 binary coded decimal readout to the rear panel 50 pin connector appears on pins 5, 6, 7 and 8 of the board.

16. The carry and borrow inputs to the UD5 Board appear on pins 25 and 26. These

drive the following divide by 10 circuits directly. The divide by 10 circuits are reset to 0 only. After the time is measured the resulting 1-2-4-8 binary coded decimal representation of the number for the front panel display appears on pins 30, 29, 28 and 27 respectively. In addition the 1-2-4-8 readout to the rear panel connector appears on pins 31, 32, 33 and 34. The nixie display drive parallel readout consists of a 0 volt signal for a 1 and approximately +3 for 0. A 1 and a 0 are represented respectively by +3 and 0 volts for the rear panel readout. Any overflow that may occur is detected after the end of the add and subtract by the detection circuitry and monostables I4, I5, I6, I7 and I8. These consist of binaries driving "and" gates such that a output occurs only after the end of a transition. These drive the following monostables which create a set of sequential times that are spaced far enough apart that high speed operation is not required. In addition to containing the up down counting circuitry the UD5 Board contains the divide circuit for the 10 to the second power nixie counting and display circuitry. This input is a positive transition going from approximately 0 to +3 volts on pin 9 of the UD5 Board. The signal at this point is a 10 megahertz signal and is inverted in the following integrated circuit inverter. The resulting negative transition then drives the divide by 10 circuit. The 1-2-4-8 binary coded decimal output to the front panel integrated circuit nixie display drive is then presented on pins 10, 11, 19 and 20. The 1-2-4-8 binary coded decimal readout to the rear panel connector appears on pins 21, 22, 23 and 24. The output of the SN7490 decade then is inverted and appears as positive going transition on pin 8 of the UD5 Board. A positive output occurs on pin 6 after the end of add and subtract which then drives pin 20 of the Control Board, initiating the printout nominally 200 microsecond wide pulse that appears on the rear panel 50 pin connector. This signal indicates that all data is ready to be readout into external registers. Note that for those conditions when the stop is close to the start pulse or not much more than several hundreds microseconds away the add signals completely inhibit the subtract signals because of the add not subtract circuitry at the front of the UD1 Board. Accordingly the subtract outputs of the UD1 and UD5 Board do not show negative transitions for this condition.

17. The positive going edge of the negative appearing pulse on pin 8 of the UD5 Board then drives the front panel DDNT decade dividers.

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18. The Reset Board controls the reset and recycle signals to the rest of the Time Interval Meter. The front panel switch selects either manual, automatic or external reset. In the manual position actuation of the front panel reset pushbutton causes the binary consisting of Q27 and Q28 on the Reset Board to switch to the opposite condition creating 1 and only 1 transition. The resulting transition is selected by the 3 position reset switch and fed to Q8 and Q12. Q12 is the input to Q14 and Q15 which provides the basic Reset pulse for the whole Time Interval Meter. In addition Q13 always is actuated by the front panel pushbutton even if the front panel switch is not in manual. The internal automatic reset is controlled by Q3 and Q6 arranged as a free running astable multivibrator. The exact time is controlled by the 50k potentiometer when present. The resulting transitions are squared and amplified in Q10 and Q11 and applied to the auto position of the reset switch. The resulting positive transitions are again detected in Q8 and Q12 and actuate the reset monostable. The Reset pulse is inverted and buffered by emitter follower Q18 and presented on pin 19 of the Reset Board as a positive going pulse going from approximately -1 to +3 volts with a nominal duration of 20 microseconds.

19. In addition the output of the monostable from Q14 is squared and inverted in Q21 and Q22 and differentiated by the input circuitry of Q23. The output of Q23 drives Q24 which then drives Q25 and Q26. The lagging edges of Q24 are used to drive Q25 and Q26 and thus the resulting signal at the emitter of Q25 and Q26 which are arranged as emitter followers occurs after the end of the lagging edge of the reset pulse. The signal appearing on the emitter of Q25 and appearing on pin 32 is the positive going Recycle pulse when then opens the lockout binaries that control the input start and stop gates.

20. In addition when reset occurs the binary consisting of transistors Q29 thru Q32 is turned on. The 1 nanosecond position counter and display is pre set to a number that is nominally 7 or 8 nanoseconds. This is to compensate for the 0 thru the start and stop channels. However, when the unit is reset this decade and the four adjacent least significant decades are brought to a 0 for the front panel display only, by the inhibit binary. The inhibit binary drives

the following two inverters which thru the following high voltage diode pull down the 0 of the front panel nixie displays to approximately -30 volts thus causing the 0 to lite. Meanwhile the rear panel 1-2-4-8 binary coded decimal output is at approximately 7 or 8 nanoseconds when the unit is reset. When the unit measures the actual time between the start and stop the numbers on all digits is the proper number. When the data is ready to be read out and displayed the negative going signal on pin 33 of the Reset Board turns the inhibit binary off thus allowing the front panel nixies to display the proper number.

21. The front panel DDNT Board contains the nixie drive circuits for all of the displayed digits, the counting circuit for the 10 to the third power thru the most significant digits, and the 1-2-4-8 binary coded decimal drive for the 10 to the third power thru the highest digits to the rear panel 50 pin connector. A 1 and a 0 to the 960 nixie drive front panel integrated circuits is represented by 0 and +3 respectively. The counters on the DDNT Board are reset by the positive Reset pulse. They then receive negative going pulses from the 10 to the second power circuitry via pin 8 of the UD5 Board. Each 958 integrated circuits divides its input by 10 and drives the following divide by 10 circuitry. If no stop occurs before full scale the positive transition derived from the last counter circuit is applied to pin 28 of the Control Board and thus actuates the overflow binary, lighting the front panel left hand overflow neon and actuating the rear panel overflow output.

22. Approximately 200 milliseconds after occurrence of the Reset pulse a positive going signal from pin 21 of the Reset Board drives pin 3 of the Test Board. The relatively slow going signal is successively squared in the Test Board while maintaining isolation from extraneous noise and finally producing a pair of low noise pulses which are split on 2 equal length coaxial cables and brought to the rear panel test output via pins 25 and 31 of the Test Board. These pulses may be used for zeroing the unit or measuring cables.etc. In addition a variety of circuitry useful for initial test of the unit are included on the Test Board. This includes multivibrators, squaring circuits for producing sharp edges from the multivibrators etc.

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23. The power for the Time Interval Meter is provided by the RP4C Power Supply. The Power Supply provides highly regulated +5, ±15, ±30, -37 and +225 volts to the Time Interval Meter. The transformer outputs are full or half wave rectified and filtered in the following capacitors as indicated on the schematic. For the regulated portion differential pair feedback amplifiers provide the feedback control while series pass transistors provide the power handling capabilities. Power and AC line voltage are transmitted thru the power supply 16 pin Amphenol connector. Extensive filtering is used on all input lines to eliminate spurious line and environmental pickup and triggering.

SAO SUPPLEMENT

NANOFAST COUNTER
(MODEL 536B TIME INTERVAL METER AND MODEL A3 PLUGIN UNIT)

1. GENERAL

The Nanofast counter can measure time intervals, pulse widths, and period measurements in the range of 10^8 to 10^{-2} nanoseconds to an accuracy of ±0.1 nanoseconds. Display of this actual measurement is by eleven Nixie tubes: the least significant character is displayed as one of four adjusted values, such that 0.00, 0.02, 0.05, and 0.07 nanoseconds represent a true reading of 0.00, 0.025, 0.050 and 0.075 nanoseconds respectively. All the characters, with the exception of the least significant, are also read out in BCD format from a rear panel mounted Amphenol connector.

Timing reference for the counter can be selected from either an internal 10 MHz crystal oscillator maintained to an accuracy of 1 part in 10^8 in a temperature controlled oven, or externally by separate 1 MHz and 10 MHz inputs. The input requirements for the external clock inputs are 1V rms into 50 ohms with all spurious frequencies being at least 70 db's below the level of the fundamental frequency. Choice of either channel for external clock is by a switch labeled "10 M INT, 10 M EXT, 1 M EXT".

Start and stop signal inputs to the counter, labeled A and B, which are 50 ohm impedance, are made via BNC connectors in the A3 plug-in unit mounted in front of the counter. Associated with each input is a continuously variable threshold or Level Control, graduated in increments of 0.1 volt, which range from -1.0 Volts to +1.0 Volts, an input polarity switch used in conjunction with the Level Control, an input attenuator with control

settings of 1, 2, 5, 10, 20, 50, 100, times which allows up to a maximum of 100 Volts for signal input. Absolute maximum input ratings are:

PULSE:			DC or RMS:
ATTR	Max. Volts	Input Pulse Width	3.5 V max.
X1	10 V	not greater than 1μS	
X100	200 V	not greater than 25nS	

The mode of measurement between inputs A and B are selected by a 3 position switch labeled TIME A - B, WIDTH A, and period A which allow measurements of the time difference between inputs A and B and also width and period of a pulse at input A.

Resetting of the counter can be by a manual pushbutton, automatically by the counter itself, or externally via a BNC input connector labeled EXT. This input is mounted beneath a three position RESET switch labeled MAN., AUTO, EXT., and is TTL compatible (pulse +4.5 V, 10 microseconds wide).

Remaining BNC connections to the instrument are mounted on the rear panel of the counter. A Jones strip, which carries some identical outputs to the BNC connectors, is also mounted on the rear panel. This particular connector is unsuitable for secure coaxial connections and was therefore, replaced by BNC connections. As a result, it is redundant and not used.

The remaining outputs can be grouped into two functions:

A. Test and calibration.

Two test signal outputs, which are in parallel and labeled TEST, provide the test pulses needed to calibrate the A and B channels for zero delay balance and short term stability of the counter. Calibration monitoring outputs labeled CM START and CM STOP, enable points within the counter to be monitored on an oscilloscope during short term stability calibrations. The last two outputs should only be monitored with the high impedance inputs on an oscilloscope.

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B. Outputs associated with some particular occurrence within the counter.

An output which occurs at the instant the counter is started is provided at the BNC connector labeled LATCH. This particular output which is being converted from a level shift to a 2 microsecond + 4 volt pulse by an SAO modification within the counter is used to latch the laser clock. A similar unused output which occurs at the instant of a stop pulse being received by the counter is labeled STOP GATE. Other outputs labeled START and STOP are redundant and disconnected.

2. THEORY OF OPERATION

2.1 GENERAL

It is not apparent when reading the circuit description in the manual how the Nanofast Counter works, as a result the theory of operation is given here. Also brief descriptions of each circuit card in the counter are given to help in the overall picture of how the counter operates and as an aid for fault finding. The following descriptions are intended to supplement details given in the manual.

2.2 OPERATION

Unlike the Eldorado Counter which has two oscillators of differing frequencies and uses the Vernier principle to make its measurements, the Nanofast counter operates quite differently. Like all counters it uses a clock to provide a reference time base of 100 nanosecond period (10 MHz). It makesuse of two counters (called in this description the primary and secondary) to totalize the time between the start and stop of the time interval. The primary counter measures the time differences between the start and the next 100 nanosecond marker and the stop and the next 100 nanosecond marker of the time base. These differences are translated

into a number of counts of a higher frequency: The secondary counter measures the number of 100 nanosecond periods that have occurred during the time interval and is dependent upon the primary for initiation of its counting cycle, i.e., when the measuring period between Start Stop and the time markers exceeds 100 nanoseconds, the secondary counter is enabled.

In order to obtain the measuring resolution of ±0.1 nanoseconds using the method of counting a number of cycles proportional to a time interval would require a frequency of 10 GHz. However, by extrapolating the time base period by many orders of magnitude, a lower frequency can be used. In fact the 100 nanosecond time base is extrapolated to 400 μsec. The width is dependent upon the instant within the time base period of 100 nanseconds that the counter is actually started or stopped. Two such pulses are generated: one each for the start and stop channels of the counter. This variable width pulse is used to gate a 20 MHz signal derived from the clock frequency by multiplication in the primary counter. Hence, the total number of clock pulses at 20 MHz (50 ns period) that can occur within a gate width of 400 μs is 8000 for the 100 ns period or 8 for 0.1 ns. This count of 8 is further subdivided to give the readings of 0, 0.02, 0.05, 0.07 ns in the least significant readout. The relative times between the Start, Stop and the next clock pulse is added and subtracted respectively to the secondary counter total. Each counter has its own series of Nixie readouts. Periods greater than 100 ns are totalized in the secondary counter and displayed in the readouts for 10^2 through 10^8 nanoseconds while the output from the primary counter are displayed in readouts showing 10^1 through 10^{-2} nanoseconds.

3. A3 PLUGIN DRG. #C-2052

3.1 GENERAL

The A3 plug-in is the interface between the main counter and external signal inputs. It enables both positive and negative going levels of differing amplitudes (up to X100 selectable attenuation is provided) to be accepted by common input circuits and converts them to Starting and Stopping pulses for the counter. Negative and positive edge triggering may also be selected. Start and Stop inputs are used only for measuring time intervals. For PERIOD and WIDTH measurements only, the START input is used and from this input the plug-in generates the counter Start and Stop pulses. Drawing LA 138 is an overall simplified version of Nanofast drawing # C-2052. It shows the essential signal path and control logic sequence for the A-B, Width and Period Modes.

3.2 INPUT CIRCUITS

The input circuits for the Start and Stop channels are identical and consist of standard transistor differential amplifier pairs, one side of which can be level biassed to accept positive or negative going inputs. Inputs are fed via 50 ohm switchable attenuation (having ratios of X1, X2, X5, X10, X20, X50, and X100) to one side of the differential pair. The output side is fed to I1A and I1B an MC1692L which is an Emitter Coupled Logic (ECL) line receiver. These devices in turn drive buffers I2A and I2B which in conjunction with the SLOPE switch allow triggering on the positive or negative edge of the input pulse to be selected.

With the exception of I14 and I15 which are TTL, all IC's in the Plug-in are ECL. It is not the intention to describe ECL here as it is done quite adequately in the Fairchild and Motorola Data Volumes on ECL at all SAO laser stations. The only reason for its choice over TTL is its very high speed (some ECL devices can work up to 500 MHz clocking rates). Logic operating

speeds are the main constraint on the higher repetition rate of input signals acceptable by the plug-in; hence, the fastest logic is chosen.

3.3 LOGIC OPERATION

The logic basically consists of NOR gates: They are used as gating functions controlled by Set Reset Flip Flops (SRFF) toggled sequentially to allow time interval, pulse width and period measurements to be made. These are made on all inputs to the Start Channel with the initial edge of the Start pulse selected by the SLOPE switch starting the counter. The MODE switch controls the steering logic and selects which measurement on the pulse will stop the counter. Two gates in I2A and I2B controlled by the SLOPE switches determines which input edge is used as the starting reference, while the third gate provides inverted and non-inverted signals to I7 and I10. Starting from counter RESET, logic operation will be described.

The first pair of gates in IC4 is reset by the Reset pulse and set by one output of one shot I15 when it is triggered by the Recycle pulse which occurs approximately 50 microseconds after the start of the Reset pulse. The second pair of gates in IC4 is also reset by the Rest pulse and set by the first pair of gates in IC4 via I7A. This in turn generates level V5 which via I10B enables I10A. I7A is controlled by the positions selected in the MODE Switch. Both Start and Stop channels are now in readiness for the appropriate input pulses.

For A-B operation, the first edge of the input pulse at Channel A is converted into positive and negative going edges by I2A which are applied to I7C(16), I7B(11), I8A(9) and (16). I7C(16) has already been enabled by the reset pulse-V1 via I4D and an input at I7C(1) sets I5B which in turn provides a level change at V2 to enable I10A. This in turn enables I10(C) ready to receive a stop pulse from Channel B input. The negative going edge applied to I7D(14) now sets

I5D SRFF which via I8C and the RC network at its output drives buffer I9 to pass the Start pulse into the Start Channel of the counter at pin 22 of the Amphenol connector (30pin).

The other output I5D enables I8A to receive the next positive going edge from I2A which is generated by the trailing edge of the input pulse, I8A now sets I6B SRFF to give output level V3. This IC has a dual function as follows: If a pulse width measurement is being made, it will toggle the input to I12B(15) which is the gate for the WIDTH measurement. This is effectively the Stop pulse which in turn stops the counter, showing the measured width on the display. This, of course, will only happen if I12B has been enabled by the proper selection of WIDTH in the mode switch. The output of I6B enabled by the next positive edge is passed through I8B(1) to set I6D SRFF and generate output level V4. This will toggle the input to I12C which is the gate for the PERIOD mode of measurement and if selected allows the stop pulse to stop the counter for a period measurment.

If operation is in the A-B mode then by the appropriate selection of the MODE switch the input to I12A is enabled. When the Stop pulse is applied to channel B, I10C which has been enabled (active low) by V2 (I10A9) sets I11B and D to toggle the input of I12A and stop the counter.

In some counters the capacitors C_P,C_W and C_{A-B} shown on the drawing at the input to I13 will be found. Their function is to equalize the delay paths of all three mode signals, as I13 is common to all three. The reference delay path chosen has the most delay and further delay using capacitors is added to the other two for equalization.

4. BOARD DESCRIPTION

4.1 GENERAL

All circuits in the Nanofast counter are contained on thirteen circuit cards. Twelve are readily extractable from the connector back plane; each card has a 70 pin connector and is held in place by a card guide and clamp. The thirteenth card, the DDNT board is mounted on the back of the front panel on stand-offs and is connected to the connector backplane by a cable harness.

The power supply components are mounted in the right hand side of the mechanical frame.

Two 'muffin' fans, one blowing directly on the power supply while the other draws air out over the circuit cards, provide cooling for the counter.

4.2 DELAY BOARD

The board contains no active circuits, only cascaded LC Pi filters organized in groups to give three separate delay lines. The function of the delay lines are:

1. To allow the Start pulse from the A3 plug-in to be used as a trigger for the Prime binary which is set and provides one of the enable lines to the input gates on the 3S board. The delayed Start is applied to the input gate of the 3S1 board.
2. Delay the Stop pulse to allow the 3S1 and Start AC converter to complete operation before the 3S2 and Stop AC converter commence operation.
3. Delay the Stop pulse which is passed to the Control board to reset the input binary Q3 and Q4 in readiness for the next start pulse.

4.3 3S1 AND 3S2 BOARD, DRG. #C2004-RA

These boards, one each for the Start and Stop channel, accept the Start and Stop pulses from the A3 plug-in and initiates counter operation. The input gate on the board is controlled by three inputs: 1) External counter gate which is not used in our system. 2) Control from the Lockout binary which is set in one state by the Recycle pulse and reset $\approx$ 200 ns after a Start or Stop pulse has been received, thereby shutting out any subsequent Start or Stop pulses until the counter is reset and the next Recycle pulse is received. 3) A further lockout binary or 'Prime Binary' as it is called in the manual, which is located on the Stop Converter Board, Card V enables the input gate of the 3S cards and is set by the direct Start output from the plug-in while this signal is also being delayed on the Delay Board, Card 1 to trigger the 3S1 card. The Stop output to the 3S2 board is also delayed in a similar fashion.

With all of the control lines to the input gate enabled, a Start or Stop pulse is directed through a number of buffers and pulse shapers and then passed to the Start and Stop converter cards 536A Converter Boards (Cards III and V). This pulse also toggles binary B101 which comprises Q8 and Q9. B101 in turn controls Q15 which is an emitter follower whose input is the 10 MHz clock. The output of Q15 is passed to 5082 module whose details are considered as proprietary information by the manufacturer and therefore not given. It is possibly a delay line as subsequent circuits control this clock output to the AC converter boards, and the clock initiated by the Start pulse which also drives the AC Converter must not arrive at converted cards until the converter circuit is ready. The gated clock is shut off when the output taken from Q23 resets B101 binary.

4.4 536 AC CONVERTER DRG. #C-2053

Like the 3S boards this card contains sealed modules whose contents are considered proprietary information by the manufacturer and its operation is only an estimate. The board has two functions 1) It contains the Prime Binary which provides one of the three enables needed by the input gate of the 3S1 and 3S2 cards. The Prime Binary is located only on the Stop converter card. It's control signal comes from the delay board and is identical to the delayed Start pulse fed to the 3S cards and allows operating time for the Prime Binary. The Prime Binary remains set until the next Recycle pulse occurs at which state it is reset ready for the next start and stop cycle. 2) The second function of the AC converter card is to take the interval between the Start and Stop pulses and the next 10 MHz clock and convert it into a pulse of expanded but proportional interval.

This actual pulse appears on Pin 23 on the card and is the same as the CM Start and CM Stop pulse viewed on the oscilloscope when calibrating the short term stability of the counter. The jittering pulse width seen is due to the counter being triggered (by the internally generated test pulses) on or about the same time the 10 MHz clock pulse is applied to pins 3 and 33. Therefore, the width is proportional in one instant to Starting and Stopping in coincidence with the 10 MHz rate when it will be at a minimum and the other instance is just after the 10 MHz clock pulse has occurred when it will be at a maximum.

In a quiescent state, i.e., no start or stop signals being received, the output at pin 23 remains low. Reset signals have 1) set Q8 in the OFF state which subsequently via Q12 appears as a 'low' output on 23, and 2) set Q26 collector in the OFF or HIGH state which appears at Q21 base as a low turning that transistor off. Modules 5078 and 5077 do not function.

On reception of Starting and Stopping pulses, the following sequence occurs: 1) the gated start pulse changes the state of Q26 which places Q21 in the ON state and module 5078 and 5077 operate. The inhibiting input on Q11 is removed which results in Q12 being turned off and the output at 23 goes high. This state remains until the next clock pulse arrives at which time the state of Q8 is reverted and the output of Q12 goes low. Thus the time between the starting pulse and the next clock pulse is recorded. The operation of the AC converter card for the Stop channel is identical. Hence, at pin 23 we see pulses of varying widths depending upon when start or stop occurs. These signals are passed as carry and borrow inputs to the up down counters on the UDIH board and commence the count of the primary counter.

4.5 CLOCK (BOARD VI) DRG. #D-2004

The function of the clock board is to accept external 10 MHz, 1 MHz or internal 10 MHz clock frequencies and convert them to (a) 10 MHz pulses of two different duty cycles for general use as system clocking (b) 20 MHz pulses for clocking the UDIH board (Board VII) which measures the 0.1 and 0.01ns increments of the time interval. The choice of external and internal signals is by switch selection. The board can be broken down into three segments 1) A X10 multiplier which converts an external 1 MHz to 10 MHz, 2) A X2 multiplier which converts 10 MHz to 20 MHz, 3) circuits which provide 10 MHz signals of 25 and 50 percent duty cycle. The former are used on the 3S1, 3S2 and test boards (Boards II, IV) where narrower 10 MHz pulses are required and the latter for general purpose system clocking. (SAO counters use only the ext 10MHz clock freq's.)

4.5.1 EXTERNAL 1 MHz CLOCK

The sine wave input is passed via the selector switch through a series

of pulse shapers, X5 multiplication buffers and filters which produce a 5 MHz signal. Subsequent X2 multiplication, amplification, and buffering produces a 10 MHz sine wave of a similar level required of the external 10 MHz signal. This signal is directed to the selector switch.

4.5.2 EXTERNAL 10 MHz CLOCK

The sine wave signal from the station reference oscillator via the distribution amplifier appears on another contact of the selector switch.

4.5.3 INTERNAL 10 MHz CLOCK

The output from the internal 10 MHz oscillator is connected to a third contact of the selector switch.

Experience has shown the internal oscillator to be an unreliable frequency source and it is not used. Also by using the station Cesium as a frequency source our counter is referred to an oscillator of known drift rate.

When any of the preceeding clock inputs are selected, they are passed to the third section of the board. Initially the signal is bufferred and filtered by a 10 MHz LC filter. It is then passed through a series of buffers, shapers, and a switch driver for distribution to:

1. The X2 multiplier to produce 20 MHz (Q28 thru Q18).
2. Output drivers to provide 10 MHz 25% duty cycle pulses for the 3S1, 3S2 and test boards at pins 6, 4 and 3 respectively.
3. A series of delay lines which in turn feed buffers and output drivers to distribute 10 MHz to the rest of the counter.

The X2 multiplier is the same type of circuit as used in the X10 multiplier and consists of a phase shifter driving a differntial switch whose output circuit is tuned to 20 MHz. Subsequent buffering and switch/drivers produce a 20 MHz pulse stream which is fed to the UDIH board via pin 20.

4.6 PRIMARY COUNTER (UDIH, UDID AND UD5E BOARDS)

4.6.1 GENERAL

This name has been chosen to help in the overall description of the Nanofast and is not used in the actual manual text. The primary counter consists of four separate counters which are mounted on three separate boards connected in series to drive each other and give the .01, .1, 1.0 and 10 nanosecond counters. They are the UDIH (0.01, .1 ns) UDID (1.0 ns) and UD5E (10 and 100 ns) boards respectively. Also located on the UD5E board is a fifth counter which provides the 100 nanosecond counts from the 10MHz input. The UDIH board derives the least significant digit first of all and then initiates the next significant and so on through all three boards. Overflow of the 100 nanosecond counter on the UD5E board initiates operation of the secondary conter located on the DDNT board which is positioned at the back of the front panel of the counter. Each board provides BCD outputs to the Nixie decoder drivers on the DDNT board and also to the 50 pin Amphenol Connector at the rear of the counter. Balancing of delays in the Start and Stop channels of the counter is done by biassing the count of the 0.1 and 1.0 nanosecond counters so that the Nixie displays a zero counter when both the Start and Stop channels are triggered simultaneously. The range of the biassing is 0 to 0.9 ns in 0.1 nanosecond increments and 0 to 9 ns in 1.0 nanosecond increments.

All counters are reset by either externally or internally generated counter reset pulses.

4.6.2 UDIH BOARD DRG. NO. D-2009

This board consists of a divide by 8 counter made up from combinatorial logic and JK flip flops, which in turn drives a DM 8560 Decade Up/Down Counter to provide the carry and borrow signals for the next counter board. As mentioned earlier this board provides the hundredth and tenths of nanosecond readout.

Arrival of the start pulse from the Start Converter Board, Board III (which can have a width change of up to 400 μs) enables the divide by 8 counter which is toggled by the 20 MHz clock.

Remembering the time base is 100 nanoseconds which in turn is represented by a Start Pulse width change of 400 μs, then the Nanofast time base period is translated (using a 20 MHz clock) into 8000 counts of 50 ns or 1 ns equals 80 counts and 0.1 ns is 8 counts. One division by 8 of the clock will toggle the 'clock up' input of the Up/Down counter which in turn divides by ten.

Therefore, a complete division of 80 made by the two counters is equivalent to 1 ns and will cause the UP/DOWN counter to generate a carry signal which triggers the counter on the UDID board. When the time interval being measured exceeds 100 ns the carry signal will cease. Arrival of a counter stop causes a stop pulse to be received from the Stop Converter board (V). The sequence of operation is repeated except the up/down counter is now primed at the count down input and every divide by 80 will produce a borrow signal which is passed to the UDID board until the next 100 ns marker occurs.

Adjustment for zero delay between the Start and Stop channels for 0.1 ns increments is made by a decimal to binary converter (IC's 11, 12, and 13) which permanently bias the data input of the Up/Down counter so that the data output will give a zero reading in the 0.1 nanosecond Nixie readout. Note, the stability of this reading reflects the short term stability of the counter which is ± 0.1 nanoseconds.

The decimal to binary conversion is effected by grounding any one of ten 2.7 KΩ resistors which are individually tied to the inputs of the gates which form the converter. Delay counts can be adjusted to 0.1 ns increments. If zero delay cannot be achieved, when any of the 0 thru 9 taps is selected,

then adjustment of the tap one step forward or backwards in an identical circuit on the UDID board must be made. This adjustment is in 1.0 ns increments, and now allows the tap on the UDIH board to be moved to the full range of 0 to 9. Note: Some counters have arrived from the manufacturer without any of the taps being used and the grounding wire will be missing. This is because satisfactory zero balance was obtained without adjustment. However if failure occurs of any component in the Start and Stop channels, particularly active components which require replacement, then use of the taps may become necessary and a grounding strap must be added to the circuit.

The hundredth of nanosecond readouts are obtained from the Q, $\overline{Q1}$, Q2 and $\overline{Q2}$ outputs of I7 and the Binary to BCD conversion logic of I15 and I14. Here the 16 possible states are converted into 0, 2, 5 and 7 to signify 0, .025, 0.05 and 0.075 ns. Transistors Q34 through Q37 provide the necessary drive to the 0.01 nanosecond Nixie readout. The data from this output is not fed to the data connector for printout because of its questionable accuracy, the values being a factor of ten lower than the prescribed accuracy of the counter. The display of the data was included mainly for appearances when the Nanofast was designed.

4.6.3 UDID BOARD DRG. NO. B-2013

The UDID board is very similar to the UDIH board except that it does not contain the divide by 8 counter. It uses the DM8560 divide by 10 Up/Down counter and the count up and count down inputs are toggled by the carry and borrow signals from the UDIH board. Connection for zero delay are made by a decimal to binary converter using the same method described for the UDIH board. The 0 through 9 data output from the up/down counter is passed via transistor drivers to both the decoder driver of the Nixies and the 50 pin

Amphenol Data Connector. Carry and Borrow output are passed via transistor drivers to the UD5E board.

4.6.4 UD5E DRG. NO. C-2050

This is the last board in the Primary counter and performs two functions: 1) provides the tens and one hundreds of nanosecond read-out and 2) generates delay and gating pulses, that allows the secondary counter to operate and the whole time interval measurement be completed on a nonreal time basis. The two functions operate in parallel. Initiation of the delay and gate circuits is from the 3S Start and Stop boards which also starts the Primary Counter operation via the Start Converter board. The delay and gate circuits consist of nand gates connected so that control of the delay circuits is relinquished the moment a STOP signal is received, pulse delay and gating is provided by retriggerable one shots connected in cascade to provide continuous delay and gating while clocking pulses from the 3S1 board are being received. Receipt of a stop pulse from the stop converter board inhibits the input from the 3S1 board, the retriggerable one shots run their course and on completion generate an END of shift pulse, which signifies the time interval measurement is completed, and subsequently triggers the Print Command circuit on the control board. Operating in parallel is the DM8560 divide by 10up/down counter. The carry and borrow signals from the UDID board are applied to the count up and down inputs respectively and the tens of nanosecond data is then taken from the data output of the counter and fed to both the Nixie readouts and the 50 pin Amphenol connector. The carry and borrow output of the tens of nanosecond counter are also passed to another DM 8560 up/down counter which generates shift pulses dependent on

the number of 10 nanosecond periods measured by the first up/down counter. These shift pulses are passed to the control board where the 10 MHz clock is gated back to the UD5E board for subsequent division by 10 in a 7490 counter to produce a) 100 nanosecond readout data and b) initiate the secondary counter with a 1 MHz clock input on the DDNT board should the ÷10 counter overflow.

4.7 SECONDARY COUNTER (DDNT BOARD)

4.7.1 GENERAL

This title like the primary counter will not be found in the main text of the manual and is only used to distinguish between the two separate counters in the Nanofast. The counter is located on the DDNT board mounted on the rear of the Nanofast front panel.

4.7.2 DDNT BOARD DRG. NO. C-2051

All the Nixie displays and decoder drivers are located on this board. The drivers for the 0.01 ns to the 100 ns readouts derive their data from the UDIH, UDID and UD5E boards, while the drivers for the 1µs through the 100 millisecond readouts obtain their inputs from the secondary counter. This counter comprises 6 stages of 958 decade counters (I8, I10, I12, I14, I16, I18) connected in cascade and is driven by a 1 MHz clock generated in the UD5E board. Parallel outputs from the counter are passed to the decoder drivers (I7, I9, I11, I13, I15, I17) and also the 50 pin Amphenol connector. An overflow output is taken from the final decade counter and passed to the control board to initiate a primary and secondary counter reset. An overflow condition is signified by a permanent count of 1000.00 shown by the Nixie display and also an overflow neon is lit. Resetting an overflow condition is made by the Recycle pulse generated on the Control board.

4.8 CONTROL BOARD (BOARD IV) DRG. #C2006-RA

4.8.1 FUNCTIONS

1) Controls the time necessary for the counter to complete the time interval measurement. After reset and an initiation of a start pulse from 3S1 board (Board II) a control flip flop enables a gate which passes the 10 MHz clock after shaping to the UD5E board (Board VIII) for division by 10 to eventually drive the counters on the DDNT board (Display and Nixie Tube Board). 2) Reception of a Stop pulse via the delay board (Board I) from the 3S2 board (Board IV) inhibits the 10 MHz gate. It also initiates a 200 ns delay which allows the sequence of counting to be completed. This additional time of two counts of the clock is automatically subtracted at initiation of the start pulse. Integrated circuit I1 toggled by the first 10 MHz clock pulse sets an RS Flip Flop I2, which inhibits the 10 MHz output to the UD5E board. On completion of its count, I1 resets I2 which in turn enables the 10 MHz output. 3) Generates a 200 μs print command pulse from I4 on instruction from the UD5E board when the operation of the primary counter is completed. 4) If a stop pulse is not received, the secondary counter overflows and the output of the last stage of the counter sets the overflow set/reset flip flop I5 to enable the overflow neon circuit. It also disables the print command output and inhibits the input flipflop B1 (Q3 and Q4) which prevents any further starting of the counter by noise pulses before the arrival of the next Start pulse.

A reset pulse is also initiated which is passed to the reset board (Board X) for redistribution to the rest of the counter. The readouts in the overflow condition freeze at a reading of 1000 μs and the overflow neon remains illuminated until the Recycle pulse generated by the system reset pulse arrives, resetting the overflow binary.

4.9 RESET BOARD DRG. NO. C2003

As the name implies this board provides all the Reset pulses for the Nanofast counter. Operation of the board can be initiated manually, externally or automatically by an internally generated pulse. Both positive and negative reset pulses are generated by the board for general device resetting throughout the counter together with additional reset and enable pulses used at times other than general reset.

MANUAL: Operation of the MANUAL reset button on the front panel triggers the manual reset binary generating a one time pulse which is amplified and buffered by transistor amplifiers which are shared by all three reset functions and distributed to the remainder of the counter. Normal reset is effective no matter what reset switch selection is made.

EXTERNAL: This arragement allows the user to reset the counter when so desired. in our case the external Reset pulse is the LCU reset ($\approx$ 500μs at +5V).

INTERNAL: An internal astable FF generates the Reset pulse when the RESET function switch is set to AUTO. The rate at which reset occurs is preset in some counters, in others it is controlled by a trim pot on the front panel.

The other reset pulses generated are:

1. Recycle pulse $\approx$100 μs after the Preset pulse which a) Enables the lockout binaries on the 3S1 and 3S2 boards thereby allowing the Start and Stop channels to receive signals. b) Enables the Prime Binary on the Stop Converter board which in turn enables the input gate to the 3S2 board c) Resets the overflow neon control circuit.

2. Units, tenths and hundredths nanosecond display reset. Because of the delay imbalance between the Start and Stop Channels, the counters for the units and

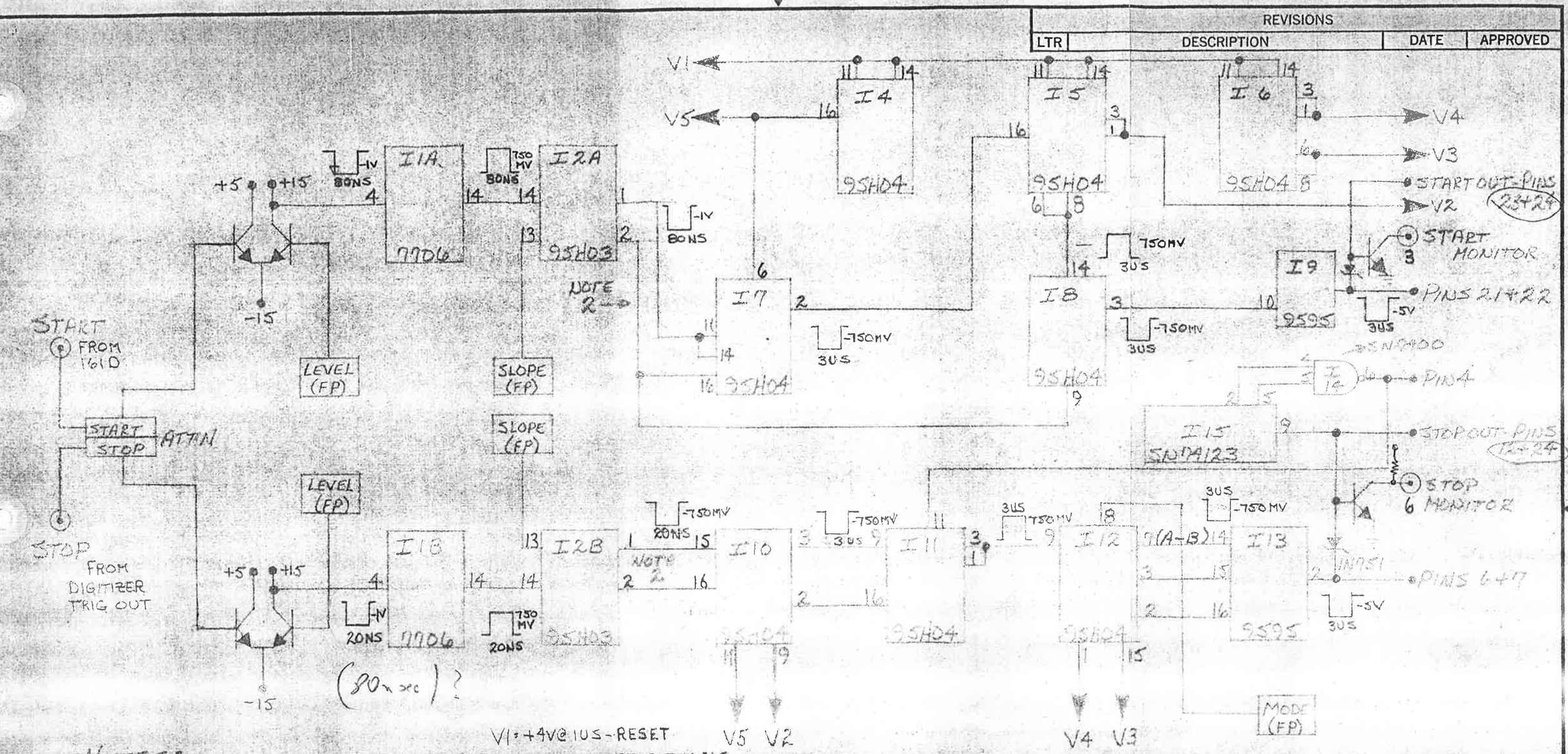
tenth nanoseconds are biassed so that the count is effectively zero (see UDIH, UD5E, boards). This means that in the absence of inputs to the start and stop channel the bias count will be displayed in the units and tenths readout. This is prevented by a reset pulse initiated by the 'end of shift' pulse from the Control board and generated by the Inhibit Binary on the Reset board which sets the units and subsequent least significant readouts to zero. This ensures that the next time readout will be correct and will not totalize with the new time interval. The data readout however, retains the bias as this is a permanent part of each time interval measurement.

4.10 TEST BOARD C2005-RA

The Nanofast counter provides its own test pulses for the purpose of zero and short term stability calibration of the counter and these are available on two BNC connectors located at the back of the counter.

On receipt of the Reset pulse from the reset board, the test board using a number of binaries, pulse buffers and shapers, produces two test pulses which are fed to two parallel emitter followers whose outputs feed the two BNC connectors previously mentioned. The need for the many stages is to produce a clean test pulse free from noise and ripple with fast rise and fall times.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



(80 nsec) ?

V1: +4V @ 1US - RESET
V2: -1V @ 3US - STOP ENABLE
V3: +1V @ 3US - WIDTH
V4: +1V @ 3US - PERIOD
V5: -1V @ 3US - STOP INHIBIT

NOTES:

1) PIN OUTS ARE FOR NEG. TRIG. CIRCUITRY
2) OUTPUTS ARE COMPLEMENTARY
3) MONITOR DRIVER XTERS ARE 2N2222
4) V1-V5 FREQ'S DEPEND ON REP RATE USED.
5) PINOUTS ARE FOR A-B OPERATION

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ± DECIMALS .XX± .XXX± ANGLES ±

MACH FIN:	✓
HT TR:	
FIN:	
MATL:	

DR RG	CHK
DATE 6 MAY 79	DATE
DSGN APPD	
DATE	
ENGR APPD	
DATE N.L 11/26/79	
PROJ APPD	
DATE	
OTHER APPD	
DATE	

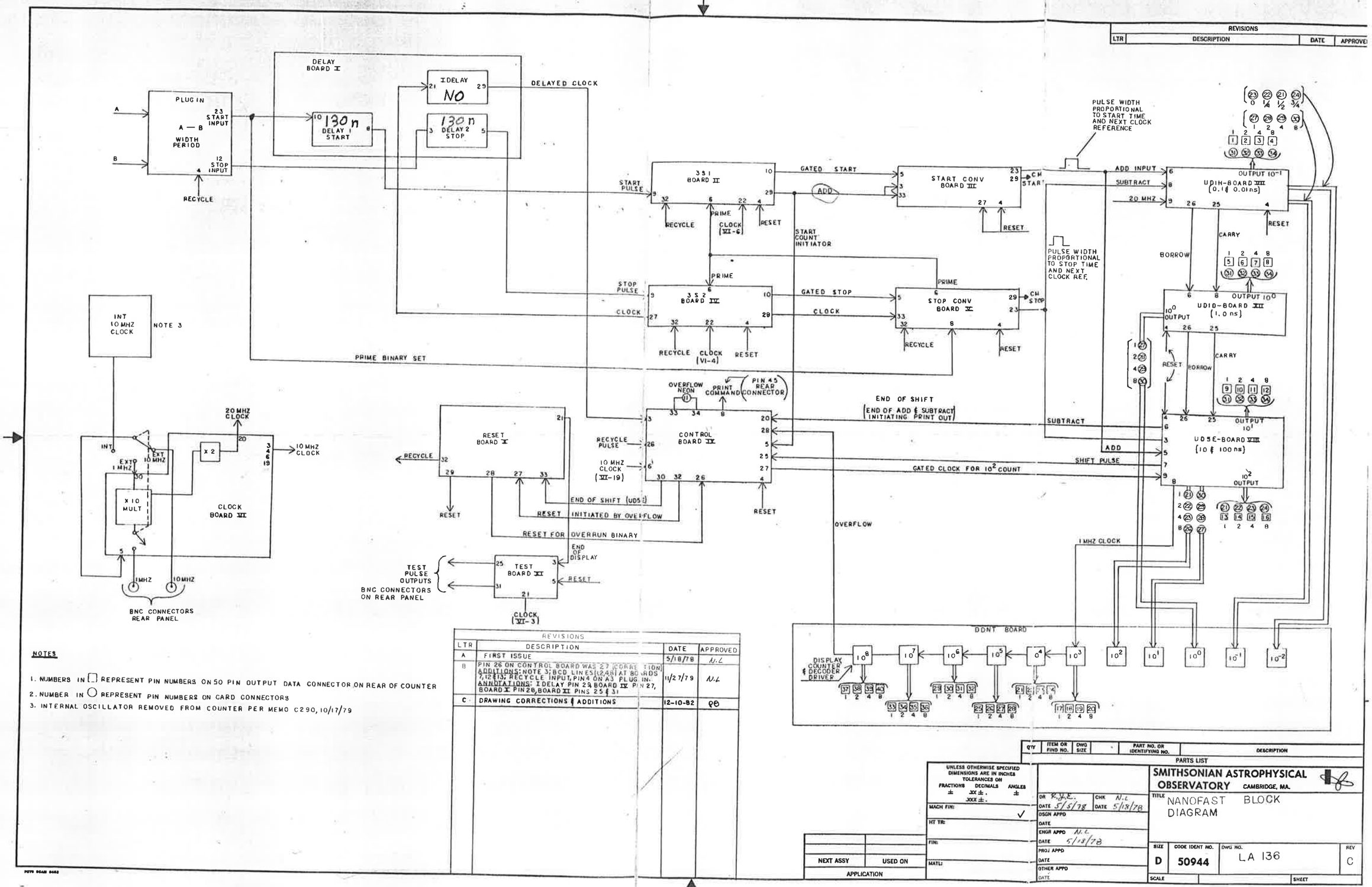
SMITHSONIAN ASTROPHYSICAL OBSERVATORY CAMBRIDGE, MA.

TITLE: NANOFAST - A3 PLUG-IN

SIZE	CODE IDENT NO.	DWG NO.
B	50944	LA 138

SCALE | SHEET

OTO BEAM 5453



NOTES

1. NUMBERS IN [ ] REPRESENT PIN NUMBERS ON 50 PIN OUTPUT DATA CONNECTOR ON REAR OF COUNTER
2. NUMBER IN ○ REPRESENT PIN NUMBERS ON CARD CONNECTORS
3. INTERNAL OSCILLATOR REMOVED FROM COUNTER PER MEMO C290, 10/17/79

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	FIRST ISSUE	5/18/78	N.L
B	PIN 26 ON CONTROL BOARD WAS 27 (CORRECTION) ADDITIONS: NOTE 3; BCD LINES (1,2,4,8) AT BOARDS 7,12 & 13; RECYCLE INPUT, PIN 4 ON A3 PLUG IN. ANNOTATIONS: 1 DELAY PIN 29 BOARD IX PIN 27, BOARD X PIN 26, BOARD XI PINS 25 & 31	11/27/79	N.L
C	DRAWING CORRECTIONS & ADDITIONS	12-10-82	PB

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED

PARTS LIST

QTY	ITEM OR FIND NO.	DWG SIZE	PART NO. OR IDENTIFYING NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MACH FIN: ✓
HT TR:
FIN:
MATL:

NEXT ASSY | USED ON
APPLICATION

DR R.J.E. 5/5/78 | CHK N.L 5/18/78
DSGN APPD | DATE
ENGR APPD N.L. 5/18/78 | DATE
PROJ APPD | DATE
OTHER APPD | DATE

SMITHSONIAN ASTROPHYSICAL OBSERVATORY CAMBRIDGE, MA.

TITLE NANOFAST BLOCK DIAGRAM

SIZE	CODE IDENT NO.	DWG NO.	REV
D	50944	LA 136	C

SCALE | SHEET