A Photonic Front-End Processor in a WDM ATM Multicast Switch

H. J. Chao, *Senior Member, IEEE*, L. Wu, *Member, IEEE*, Z. Zhang, S. H. Yang, L. M. Wang, Y. Chai, J. Y. Fan, and F. S. Choa

***Abstract*—Dense wavelength-division multiplexing (DWDM) technology has provided tremendous transmission capacity in optical fiber communications. However, switching and routing capacity is still far behind transmission capacity. This is because most of today's packet switches and routers are implemented using electronic technologies. Optical packet switches are the potential candidate to boost switching capacity to be comparable with transmission capacity. In this paper, we present a photonic asynchronous transfer mode (ATM) front-end processor that has been implemented and is to be used in an optically transparent WDM ATM Multicast (3M) switch. We have successfully demonstrate the front-end processor in two different experiments. One performs cell delineation based on ITU standards and overwrites VCI/VPI optically at 2.5 Gb/s. The other performs cell synchronization, where cells from different input ports running at 2.5 Gb/s are phase-aligned in the optical domain before they are routed in the switch fabric. The resolution of alignment is achieved to the extent of 100 ps (or 1/4 bit). An integrated 1×2 Y-junction semiconductor optical amplifier (SOA) switch has been developed to facilitate the cell synchronizer.**

***Index Terms*—Cell delineation, optical memory, optical packet switch, optical synchronization, optical VCI-overwrite.**

I. Introduction

THE recent advances of optical technology, such as add–drop multiplexing [1], [2], reconfigurable photonic switching [3], and dense wavelength-division multiplexing (DWDM) [6], have not only provided tremendous transmission capacity, but have also created a paradigm shift for the next generation network. For instance, the success of early multiwavelength optical network (MONET) trials [4] has stimulated network providers to widely deploy WDM networks to meet the exponential growth of Internet traffic, where a number of optical cross-connect switches [5] are interconnected by DWDM channels and are dynamically configured by network management. Moreover, the industry is considering carrying IP packets directly over the WDM layer to eliminate bandwidth and processing overhead between different layers, such as IP to ATM, ATM to synchronous optical network (SONET), and SONET to WDM. The optical cross-connect switches in the emerging WDM networks are usually configured in a larger time scale, e.g., a few tens of minutes, a few hours, days, or even longer. Because of the fluctuation of IP traffic and the need to meet different quality of service requirements for various multimedia traffic, IP routers are still required in the backbone network to route users' traffic at a per packet basis. However, the capacity of today's ATM switches and IP routers is far behind optical transmission capacity. Building a large-capacity packet switch using only electronic technology can potentially lead to a system bottleneck when interconnecting a number of electronic devices or modules into a large system. This is mainly caused by the enormous number of interconnection wires and the electromagnetic interference they would generate.

We have explored the possibility of switching ATM cells in the optical domain by prototyping a WDM ATM Multicast (3M) switch [7]. Other optical ATM switch architectures can be found in [15]–[18]. By taking advantage of both optical and electronic technologies, we propose to route ATM cells through an optical switching plane, while extracting and processing their headers in an electronic plane that, in turn, controls the optical devices and routes the cells to the proper output port(s). Although today's optical packet switching technology is still very primitive and cannot compete with electronic switching technology, optical packet switches have great potential to scale up their switching capacity as the technology of some key optical devices becomes mature. This paper addresses such key devices and presents our early results toward making the optical packet switches more competitive than electronic switches.

The 3M switch consists of a photonic front-end processor and a switching fabric. The switching fabric is basically an optical shared memory [8]. The 3M switch uses the broadcast and select method to achieve the switching and multicast functions by using the wavelength converters and tunable filters at the input and output ports.

The photonic front-end processor consists of cell delineation, VCI-overwrite, and cell synchronization units. The cell delineation unit identifies cell boundaries. Cells are transmitted back-to-back and not carried in SONET frames. Not using SONET frames eliminates the possibility of having variable gaps between or within cells caused by the need to carry SONET transport and path overhead ranging from 1 to 49 bytes. We adopted the ITU-T standards to perform cell delineation by finding the correct cyclic redundancy check (CRC) at the fifth byte position of cell headers. A similar method has

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H. J. Chao and L. Wu, are with the Department of Electrical Engineering, Polytechnic University, Brooklyn, NY 11201 USA (e-mail: chao@poly.edu).

Z. Zhang is with Fujitsu Network Communications, Inc., Pearl River, NY 10965 USA.

S. H. Yang is with Transcomm Technology System, Inc., Fremont, CA 94538 USA.

L. M. Wang is with Corning, Inc., Corning, NY 14830 USA.

Y. Chai is with Tyco Submarine Systems, Ltd., Holmdel, NJ 07733 USA.

J. Y. Fan is with Nanovation Technologies, Inc., Evanston, IL 60602 USA.

F. S. Choa are with the Department of Computer Science and Electrical Engineering, University of Maryland Baltimore County, Baltimore, MD 21250 USA.

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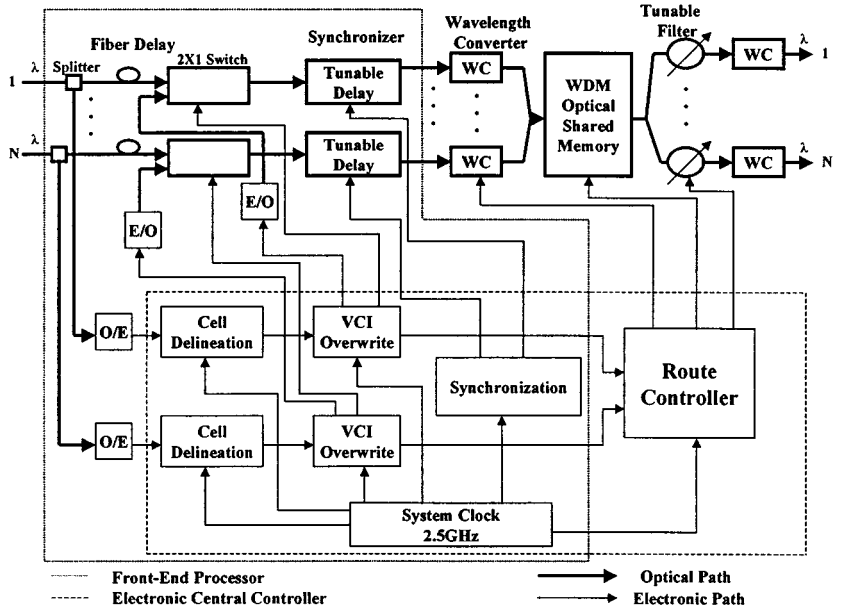


Fig. 1. Architecture of the WDM ATM multicast (3M) Switch.

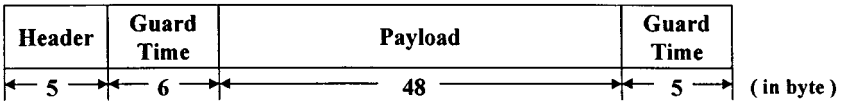


Fig. 2. Cell format adopted in the system.

also been proposed to identify packet boundaries for IP over WDM [9]. Once cell boundaries are identified, the VPI/VCI and header error control (HEC) fields are replaced optically with the new values by the VCI-overwrite unit. These two units have been implemented and demonstrated at the data rate of 2.5 Gb/s.

The cell synchronization unit is used to align the phases of incoming ATM cells in the optical domain. The synchronization issue is also addressed in [19]. Zucchelli and Burzio have implemented a two-stage cell synchronizer [10], [11], coarse and fine synchronizer, at the rate of 622 Mb/s. The former uses a few slow thermooptic 2×2 switches to control the cells through different fiber delay lines. The latter uses a tunable wavelength converter to convert the wavelength of the cells to finely adjust the delay along a highly dispersive fiber. In our design, we adjust the phases of optical cells at 2.5 Gb/s to a reference cell clock with the adjustment range from 1 to 511 bits and with a precision of 1/4 bit (or 100 ps). We have adopted a novel sampling method to achieve 100-ps precision without using a 10-GHz clock.

In this paper, Section II presents an overview of the enhanced 3M switch and the optical random access memory. Section III describes the architecture of the photonic ATM front-end processor. Section IV shows the implementation and testing results. Section V presents the conclusions.

II. An Overview of the 3M Switch

Fig. 1 shows the architecture of an enhanced $N \times N$ 3M switch, where incoming cells running at 2.5 Gb/s are optically split into two paths. Cells on the top path remain in the optical domain and are routed through the optical switch plane.

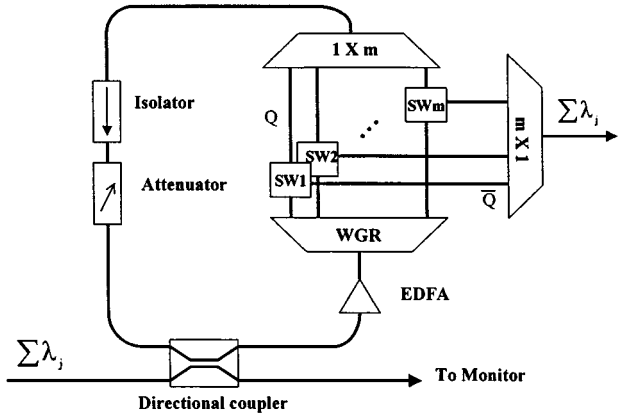


Fig. 3. An optical random access memory.

Cells on the bottom path are converted to the electronic domain, where their headers are extracted for processing (e.g., finding the output ports for which the cells are destined and finding new VPI/VCI values to replace the old VPI/VCI values). An electronic central controller, as shown in Fig. 1, performs cell delineation, VCI-overwrite, cell synchronization, and routing. The first three functions are implemented in the photonic ATM front-end processor, while the last one is handled by a route controller that routes cells to proper output ports.

As shown in Fig. 2, the cell format adopted in our system has 64 bytes with 5 bytes of header, 48 bytes of payload, and 2 guard time fields (with all ones), which are 6 and 5 bytes

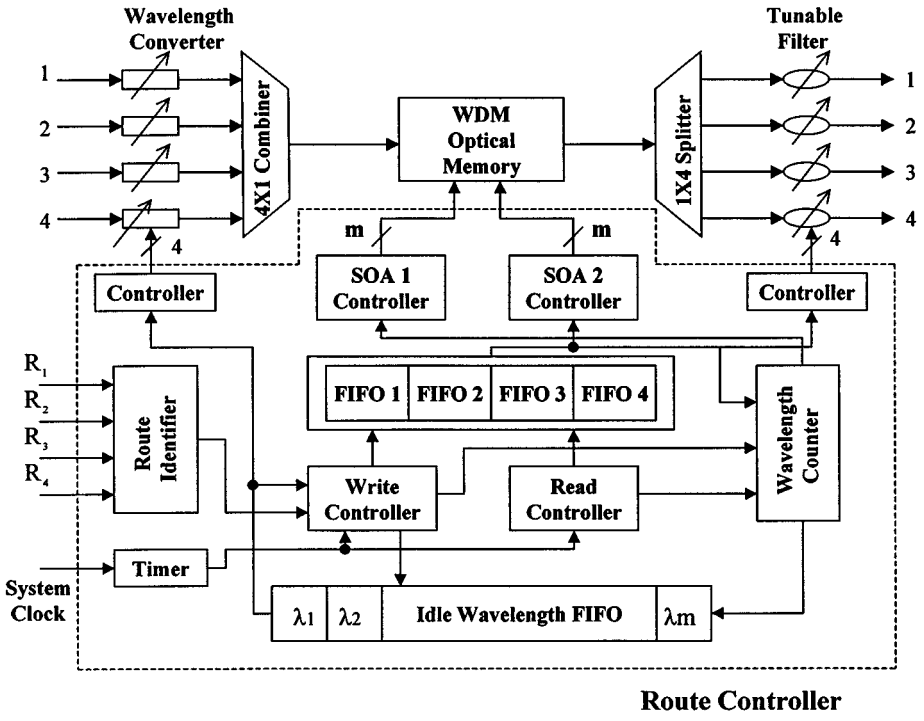


Fig. 4. An optical shared memory controlled by a route controller.

long, respectively. The guard times are used to accommodate the slow switching of optical devices, such as optical tunable filters. The lengths of the guard times between the cells, and between the cell header and the payload were arbitrarily chosen to demonstrate the feasibility of the technology.

The incoming optical cells are first delayed by fiber lines, processed for their headers, and synchronized in the front-end processor before they are sent to the switch fabric. In the switch fabric, cells are converted to different wavelengths by wavelength converters (WC's) that are controlled by the route controller, which keeps track of the available wavelengths in the WDM optical shared memory. It is a fiber loop memory, as shown in Fig. 3, and is used to store optical cells until they are ready to be transmitted to the next node. Using a 3-dB directional coupler, cells are coupled into the optical memory and coexist with the existing cells. Accessing cells in the optical memory is done by controlling the 1×2 space switches (SW's), e.g., semiconductor optical amplifier (SOA) gate. The maximum number of cells (i.e., wavelengths) simultaneously stored in this memory is m, which has been demonstrated to be 23 circulations at 2.5 Gb/s (see Section IV for details). Cells read from the WDM optical shared memory are broadcast to all N output ports by a $1 \times N$ splitter and selected by the destined output port (or ports, if multicast) through tunable filters that are tuned by the route controller at a per-cell basis. The final wavelength converter stage converts cells to their predetermined wavelengths. Other optical loop memory can be found in [20]–[22].

Fig. 4 shows how the shared memory is controlled by a route controller. R_1–R_4 signals carry the output port addresses for which the cells are destined. An Idle Wavelength first-in–first-out (FIFO) keeps track of available wavelengths in the memory. When up to four incoming cells arrive, free

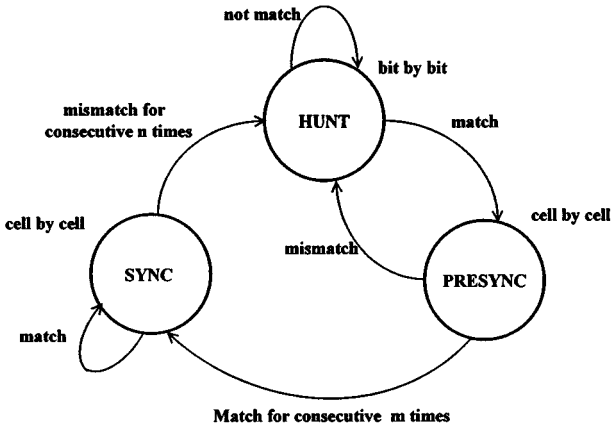


Fig. 5. State diagram of cell delineation.

wavelengths are provided by the Idle Wavelength FIFO, and are used to convert incoming cells' wavelengths so that they can be written to the loop memory at the same time. These wavelengths are stored in the FIFO's (FIFO 1–FIFO 4) according to the R_1–R_4 values. Since the 3M switch supports multicasting, the same wavelength can be written into multiple FIFO's. All the FIFO's (including the idle wavelength FIFO) have the same depth, storing up to m wavelengths. While the wavelength values are written sequentially (up to four writes in each cell slot) to the FIFO's, the wavelengths of the head-of-line cells of the FIFO's are read simultaneously so that up to four cells can be read out simultaneously. They are, in turn, used to control the tunable filters to direct the cells to the proper output ports.

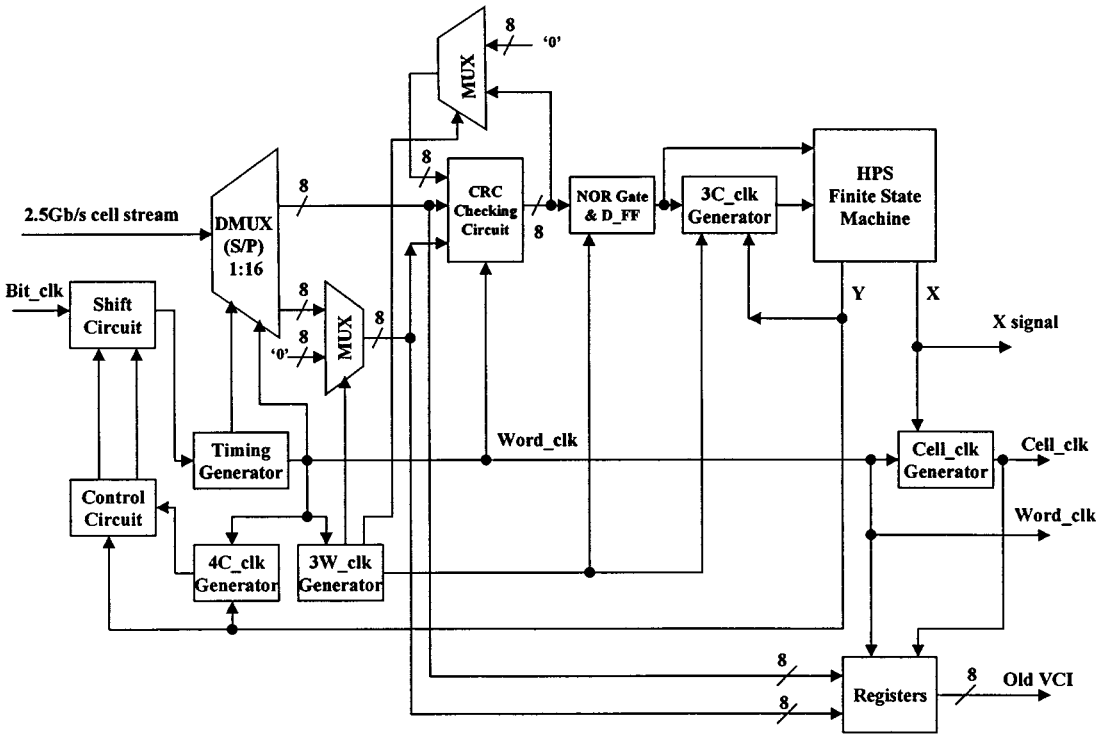


Fig. 6. Block diagram of the cell delineation unit.

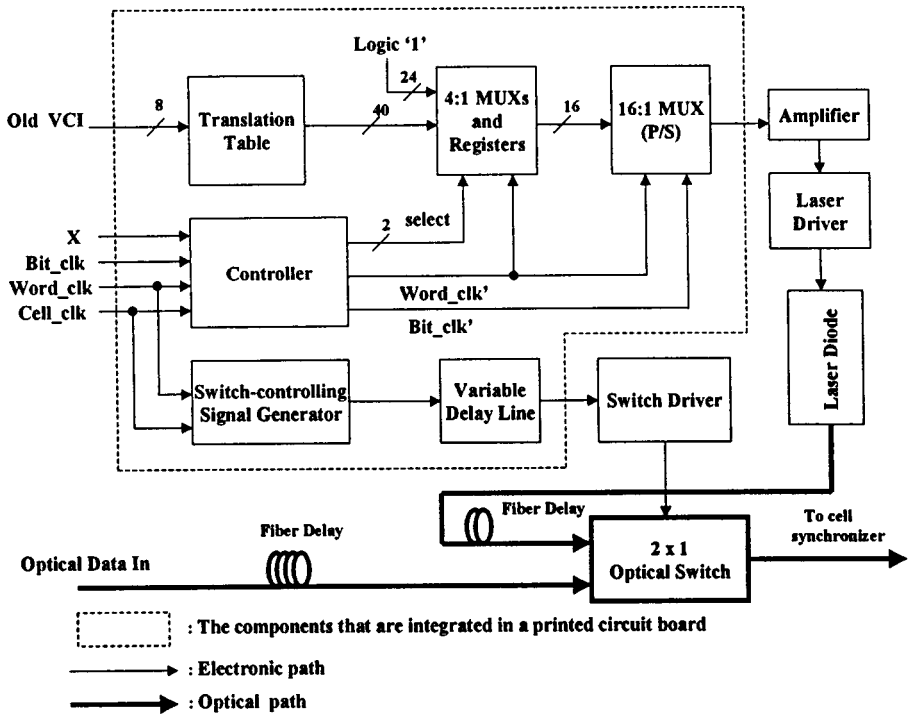


Fig. 7. Block diagram of the VCI-overwrite unit.

The write controller and read controller generate proper signals to coordinate all functional blocks.

The jitter from the high-speed control circuits (2.5 GHz) has been minimized by taking some careful steps, such as optimizing circuits design at 2.5 GHz, using high-speed ECL and GaAs chips, Getek PCB material.

III. The Architecture of the Photonic ATM Front-End Processor

The header of an ATM cell carries all necessary routing information. The photonic ATM front-end processor is designed to extract cell headers and perform cell delineation, VCI-over-

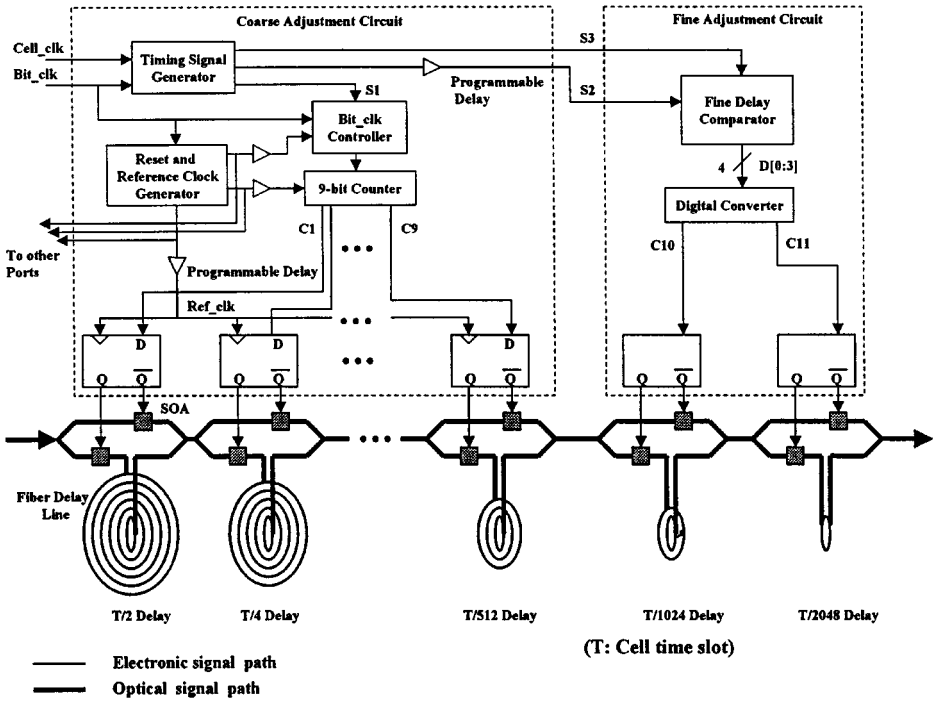


Fig. 8. Block diagram of the cell synchronization unit.

write, and cell synchronization. The front-end processor presented in the paper is used for an OC-48 line. The optical devices in the system need to have flat gain over wide bandwidth to accommodate WDM applications. The gain of the optical switches used in the system is kept just enough to overcome the insertion loss while input power is sufficiently high to suppress the ASE noise.

A. Cell Delineation Unit

As shown in Fig. 1, an optical cell stream is tapped from each input line, converted to electronic format, and sent to the cell delineation unit. Cell delineation is a process used to identify cell boundaries so that the incoming cell stream can be further processed at the cell level by the following units, such as VCI-overwrite.

We adopted the standardized HEC checking mechanism to find cell boundaries. It takes advantage of the inherent Cyclic Redundancy Check (CRC) coding correlation between the cell header to be protected (the first 4 bytes) and HEC byte (the fifth byte of the cell header). Fig. 5 shows the state diagram of cell delineation. Initially, a cell boundary is arbitrarily assumed and checked by performing a polynomial division bit-by-bit in the HUNT state (Fig. 5). If the remainder (i.e., syndrome) for a complete calculation is zero, then this boundary is assumed to be correct. Otherwise, shift a bit from the data stream and repeat the operation until the syndrome is zero. Once a cell boundary is determined, it has to be confirmed cell-by-cell for eight consecutive times in the PRESYNC state before the cell boundary is claimed to be found. It then goes to the SYNC state. Once in the SYNC state, the cell boundary is claimed to be lost when seven consecutive mismatches occur. As a result, the above procedure for cell delineation will start over again (from the HUNT state).

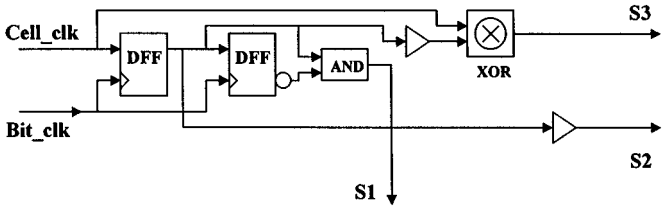


Fig. 9. Block diagram of the timing signal generator.

As shown in Fig. 6, to reduce the high-speed circuit requirement, the serial bit stream at 2.5 Gb/s is first converted to 16-bit parallel words (155 Mb/s) through a serial to parallel converter. A 16-bit parallel format of the CRC circuit is used to perform polynomial division and the syndrome is checked every three word clock cycles. An HPS (HUNT, PRESYNC, and SYNC) finite state machine performs the state transition between HUNT, PRESYNC, and SYNC states in Fig. 5. If a syndrome equals zero, then the finite state machine goes to the PRESYNC state from the HUNT state and disables a set of control and shift circuits by a signal Y. Otherwise, the finite state machine informs the control and shift circuits to inhibit a bit or a byte every three cell clock cycles. Once the cell boundary is confirmed, the state machine goes to the SYNC state and sends a signal X to create a cell clock, which indicates the location of the cell boundary. The cell clock and signal X are passed to the VCI-overwrite unit together with the old VPI/VCI and the word clock. In our design, the cell boundary can be identified within 72 cell time slots from a random bit stream.

Identifying cell boundaries for a back-to-back cell stream at 2.5 Gb/s without using SONET frames is much more difficult than the case where cells are carried over SONET frames. In our design, when an error HEC is detected in the HUNT state,

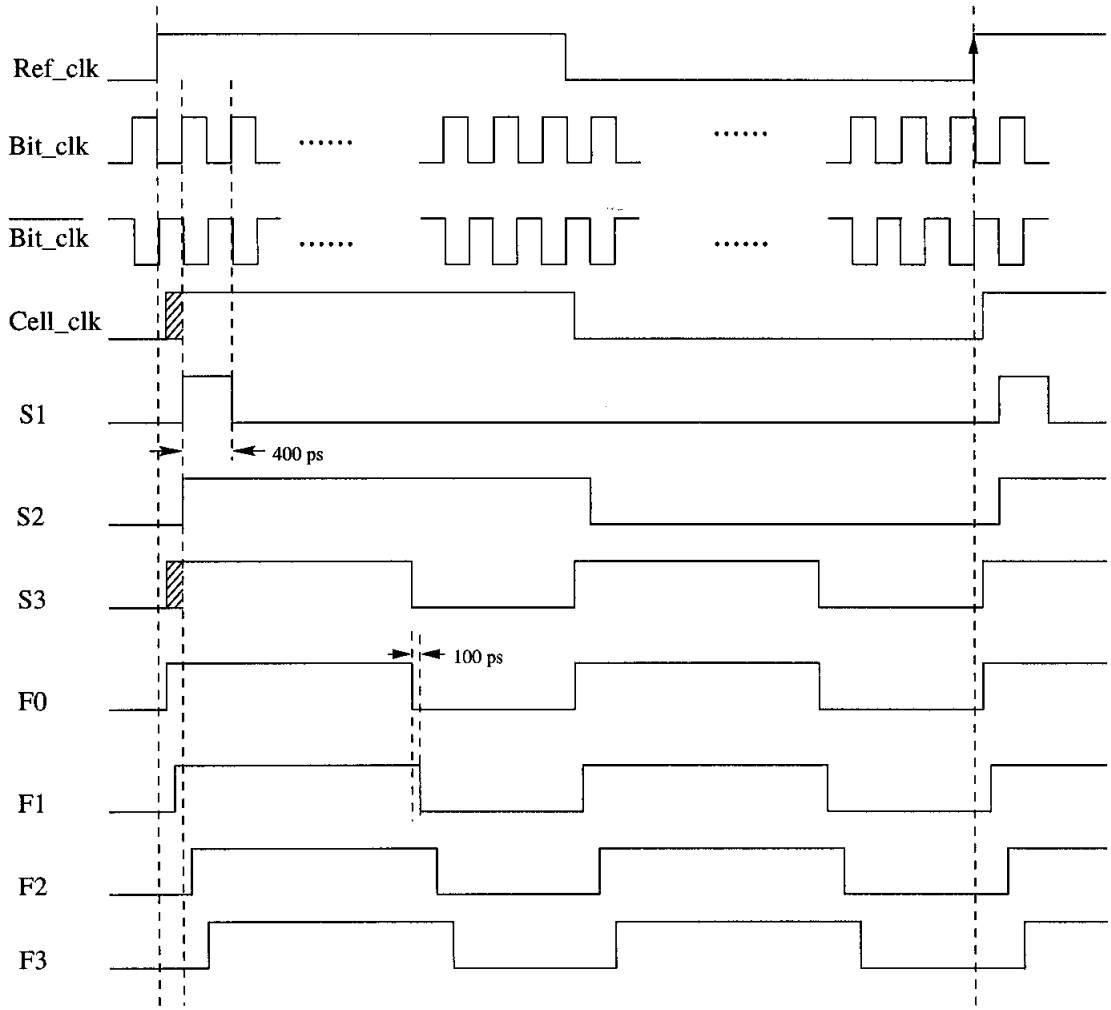


Fig. 10. Sample timing of the fine adjustment circuit (1/4 bit).

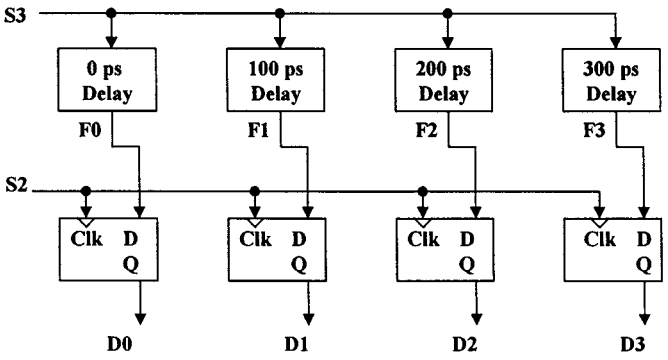


Fig. 11. Fine delay comparator.

the system clock (2.5 GHz) is shifted by one bit to restart the HEC hunting process as opposed to shifting one byte in the case where cells are carried over SONET frames. This is achieved by masking a clock pulse at 2.5 GHz (or 200 ps), which is very challenging.

B. VCI-Overwrite Unit

Once cell boundaries are recognized and confirmed by the cell delineation unit, the state machine moves to the SYNC state and enables the VCI-overwrite unit with the cell clock and signal X, as shown in Fig. 7. The main function of this unit is to overwrite the VPI/VCI field of the incoming cell header in the optical domain. The VCI-overwrite unit performs table lookups in the electronic domain, converts the new VPI/VCI to an optical signal, and replaces the old VPI/VCI by using a 2×1 optical switch. The routing table (i.e., VCI/VPI translation table) is pre-programmed manually for permanent virtual connections (PVC's) and not by UNI and PNNI signaling protocols that are used for switched virtual connections (SVC's). The challenge is how to handle the high-speed overwriting at the bit rate of 2.5 Gb/s with each bit only 400 ps. We resolve it by (a) replacing the whole cell header instead of just the VPI/VCI fields, and (b) using electronic variable delay lines (programmable delay) to compensate for the time difference between the old header and the new header.

As shown in Fig. 7, the new header obtained from the table lookup is converted to a serial format by a parallel to serial converter. It is then used to control a laser driver to drive a DFB laser diode that generates the cell header in the optical domain. The new header replaces the old one using a 2×1 optical switch that is controlled by a 6-byte wide pulse in every cell time slot.

TABLE I
CONVERSION TABLE BETWEEN [D0, D1, D2, D3] AND [C10, C11]

D0 (0 ps)	D1 (100 ps)	D2 (200 ps)	D3 (300 ps)	C10	C11
0	0	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	1
1	1	1	0	1	0
1	1	1	1	1	1

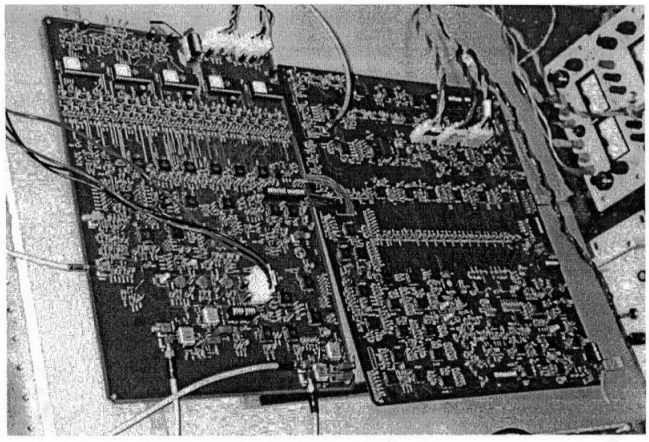


Fig. 12. The PCB's of the cell delineation and VCI-overwrite units.

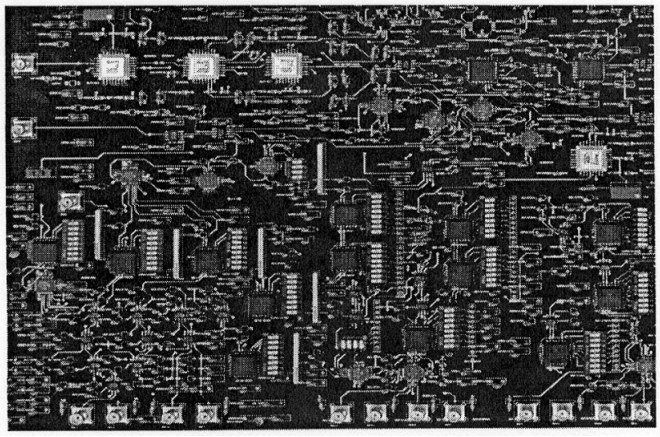


Fig. 13. A portion of the PCB of the cell synchronization unit.

TABLE II
SUMMARY OF THE PRINTED CIRCUIT BOARDS

Board Name	Cell Delineation	VCI-Overwriting	Cell Synchronization
Size (inch)	15 x 13	15 x 10	15 x 20
Number of Layers	8	7	10
Material	Getek	Getek	Getek
Maximum Operation Speed	2.5 Gb/s	2.5 Gb/s	2.5Gb/s
Power (watt)	40	25	41
Number of IC	95	94	61+36/N*
Components	Motorola's ECLinPS Family NEL GaAs IC NEL SST ECL Logic IC Vitesse's MUX/DMUX GaAs IC Atmel's AT27C256R EPROM		

* There are 36 chips in the Reset and Reference Clock Generator shared by all N input ports.

The successfully overwritten cells are sent to fiber delay lines in the cell synchronization unit.

The switching speed of the 2×1 optical switch is 1 GHz, which is sufficiently fast for our application. The time delay of the VCI-overwrite Unit is mainly caused by the VPI/VCI table lookup and is negligible as compared to the propagation delay between switch nodes.

C. Cell Synchronization Unit

In the 3M switch, synchronization is done at two levels. The cell contention resolution, VCI/VPI overwrite and cell read/write from/to the loop memory are executed at the cell level while the interaction between electronic and optical signals is at the bit level. For instance, cell header overwrite optically is done at the bit level. Furthermore, synchronization among the incoming optical cells is achieved at 1/4 bit.

The cell synchronization unit in Fig. 8 is used to optically align cells from different inputs to the extent of $1/4$ bit (100-ps or 2-cm optical delay line at 2.5 Gb/s) before they are further processed in the switch fabric. Because of the stringent timing requirement, we divide the control into two steps. A coarse adjustment circuit controls the first nine stages of the optical delay elements and adjusts the phases of incoming cells down to the bit level. A fine adjustment circuit controls the last two stages and further adjusts the phase down to $1/4$ bit.

Each stage of the optical delay element consists of a Y-junction SOA gate, a combiner, and a fiber delay line with a delay of $T/2^n$ (where T is one cell time and n is from 1 to 11). There are challenging issues in the optical delay line fabrication, such as polarization, noise reduction, coherent crosstalk, and power stabilization. We have fabricated InP-based semiconductor Y-junction switches for the delay units.

The cell clock generated in the cell delineation unit indicates the cell boundaries. By comparing the cell clock to a reference clock generated by the system, a 9-bit digitized timing difference can be obtained by using a 9-bit counter in the coarse adjustment circuit. Signals C1 to C9 control the nine switching stages (each consisting of two SOA gates) to determine if each cell should pass the fiber delay line or not. As shown in Fig. 9, three important timing signals S1–S3 are generated by the Timing Signal Generator. S1 shown in Fig. 10 is used to enable the 9-bit counter at the beginning of the Cell_clk. As the 9-bit Counter is incremented by the bit clock, its output is sampled and latched at the next rising edge of the Ref_clk. Thus, the latch value (C1–C9) indicates the phase difference between the Cell_clk and the Ref_clk at bit level.

However, to identify the timing difference for less than one bit is challenging. A novel sampling technique is adopted to adjust the phase down to 100 ps without using a 10-GHz clock. S2 signal, a variant Cell_clk that is aligned with the bit clock as shown in Fig. 10, is used as a sample clock to determine the phase difference between the Cell_clk and the Ref_clk at the sub-bit level. S3 signal mimics the Cell_clk but with a shorter duration and is used to produce four similar signals (F0–F3), each separated by 100 ps. S2 signal then samples the F0–F3 signals as shown in the fine delay comparator (Fig. 11). The sampled outputs D0–D3 show the phase difference within a bit. For instance, the sampled value in Fig. 10 is "1100," corresponding to the phase difference of 100 ps. Note that the actual phase difference can be between 100 to 200 ps. Since the resolution is

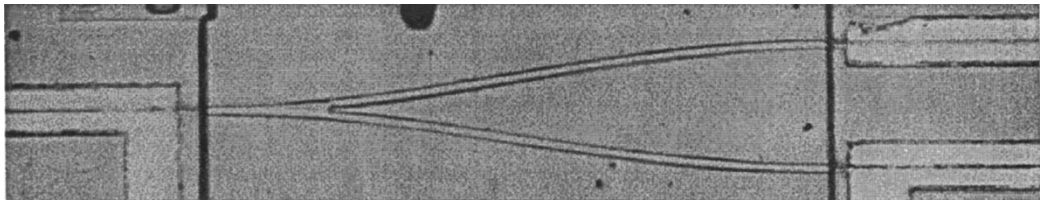


Fig. 14. A fabricated 1×2 SOA gates switch.

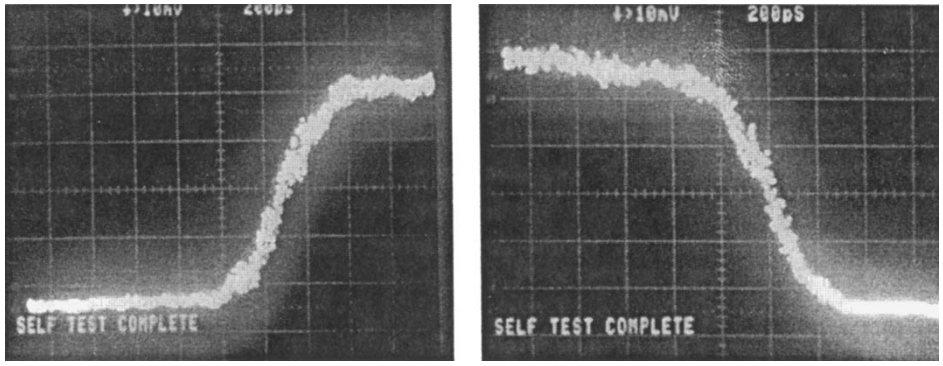


Fig. 15. Switching characteristics of an SOA switch (200 ps/div.).

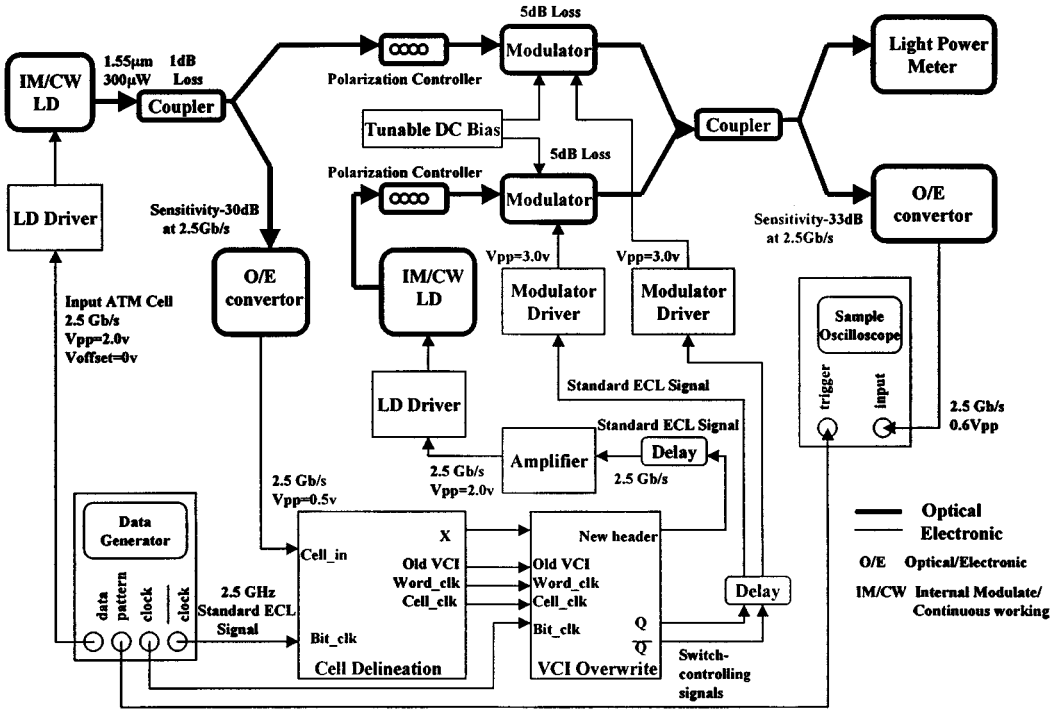


Fig. 16. Testing setup of the cell delineation and the VCI-overwrite units.

100 ps, the phase adjustment error is limited to 100 ps. Table I shows the mapping of the fine sampled value (D0–D3) to the last two bits of the delay line control (C10, C11).

With different combinations of C1 to C11, the optical delay elements are tuned to insert the desired delay needed to align the phase of incoming cells. For example, with [C1, C2,. . ., C11] = [1, 0, 1, 0, 0, 0, 0, 0, 0, 0, 1], a total delay of $T/2 + T/2^3 + T/2^{11}$ (the last term is $1/4$ bit), is added by the cell synchronization unit.

IV. Implementation and Testing

A. The Printed Circuit Boards

The photonic front-end processor system has been implemented using off-the-shelf ECL or GaAs chips on three printed circuit boards (PCB's). They perform cell delineation, VCI-overwrite, and cell synchronization, respectively.

In the cell delineation PCB, a 16-bit demultiplexer performs serial-to-parallel conversion and converts a 2.5-Gb/s serial

bit stream to 16-bit parallel words at 155 Mb/s, reducing the number of high-speed components and implementation costs. A number of EPROM chips are used for VCI translation in the VCI-overwrite PCB. A 16-bit multiplexer performs parallel-to-serial conversion for the cell headers and overwrites the old VCI optically. In the cell synchronization PCB, several programmable delay chips are used to adjust the phase of some signals in the coarse and fine adjustment circuits. The delay adjustment range varies from 1390 to 3630 ps with approximate 20-ps delay step resolution.

Fig. 12 is a photograph of the cell delineation and VCI-overwrite PCB's. Fig. 13 shows a portion of the cell synchronization PCB. Table II summarizes the characteristics of these three PCB's.

B. 1×2 *SOA Switches*

We have developed the integrated 1×2 Y-junction SOA switches that are used in optical delay elements of the cell synchronization unit and the WDM optical shared memory.

Fig. 14 shows our integrated 1×2 Y-junction SOA photonic switch that is 2×0.5 mm. It can be fabricated on an InP substrate by wet etching and regrowth processing. The Y-junction passive waveguide, with a stripe width of 3.75 μm, has a buried rib structure with two output ports separated by 250 μm. The total length of the passive waveguide is 1200 μm. The SOA active regions are located at both the input and output sides of the device to overcome the insertion loss. Each one of the SOA's has a length of 400 μm. They are made of InGaAs–InGaAsP multiple quantum well around 1550 nm. After the antireflection coating, the ripple in the spontaneous emission spectrum is smaller than 0.2 dB at the working bias current.

Fig. 15 shows the switching characteristics of the fabricated SOA switches. An optical "dc" signal is switched on and off by the SOA gates controlled by external electrical signals. Both the rising and falling times are around 600 ps, which is partially limited by the driving electronics. Further improvement of the speed by reducing the area of the electrical contact 5 to 10 times is possible. However, since guard times between cells are employed, the subnanosecond switching speed of the device is good enough for our applications. By using the fabricated 1×2 SOA switch, we have demonstrated the data-block switching operation.

C. Testing of the Cell Delineation and VCI-Overwrite Units

Testing is divided into two parts, one demonstrating cell delineation and VCI-overwrite, and the other demonstrating cell synchronization.

We integrate two PCB's (cell delineation and VCI-overwrite units) with the necessary optical devices as shown in Fig. 16. A data generator generates the 2.5-GHz Bit_clk and a series of 2.5-Gb/s back-to-back cells. To simplify the test, the generated cells with the format shown in Fig. 2 have a random payload but an identical cell header pattern, which is {00001010, 11001100, 11101110, 11110000, 10100000}. We assume that only the third byte (representing VCI) and the fifth byte (HEC byte) are updated in the VCI-overwrite unit.

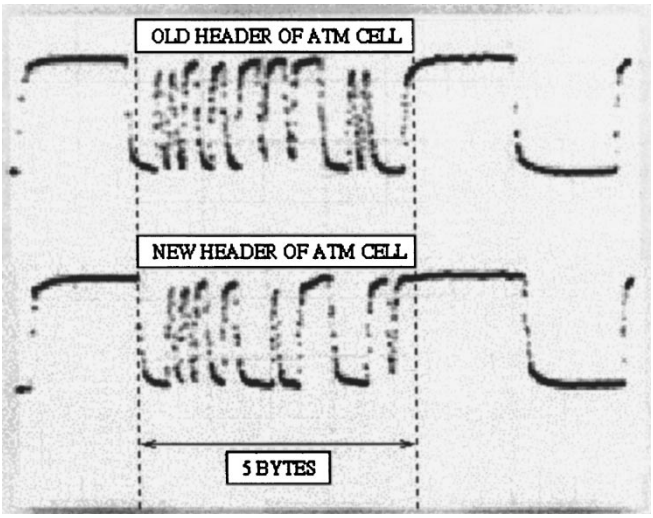


Fig. 17. Testing result of the cell delineation and VCI-overwrite units (3.6 ns/div).

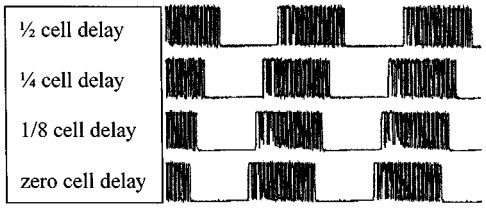


Fig. 18. Coarse delays adjustment.

Since inputs and outputs of two PCB's have standard ECL voltage levels, with $V_{\rm pp} = 0.9$ V, which is different from that of the laser driver ($V_{\rm pp} = 2.0$ V), an amplifier is needed. The 2×1 optical switch is accomplished by two modulators and drivers that are controlled by the VCI-overwrite unit. A high-speed oscilloscope is used to examine the overwritten cell stream, which is converted from optical format to electronic format by an O/E converter.

When the system is powered on, the data generator provides a cell stream and a Bit_clk to the system. Depending on the position of the first cell boundary selected by the cell delineation unit, the correct updated cells can be obtained and monitored in the oscilloscope.

Fig. 17 shows the testing results of the cell delineation and VCI-overwrite units. The new header becomes {00001010, 11001100, 00010001, 11110000, 01110111}, which meets our expectation.

D. Testing of the Cell Synchronization Unit

The cell synchronizer PCB controls the 11 stages of optical delay elements through C1 to C11 signals that turn on or off the 1×2 Y-junction SOA switches. The fiber delay length varies from $1/2, 1/4, \ldots$ to $1/2^n$ of an ATM cell, where n is the number of delay stages.

Fig. 18 illustrates the $1/8, 1/4$, and $1/2$ cell delay by using appropriate fiber length for an optical cell with a 400-ns length at 2.5 Gb/s. The fiber-to-fiber insertion loss of the SOA switch is currently at 5 dB.

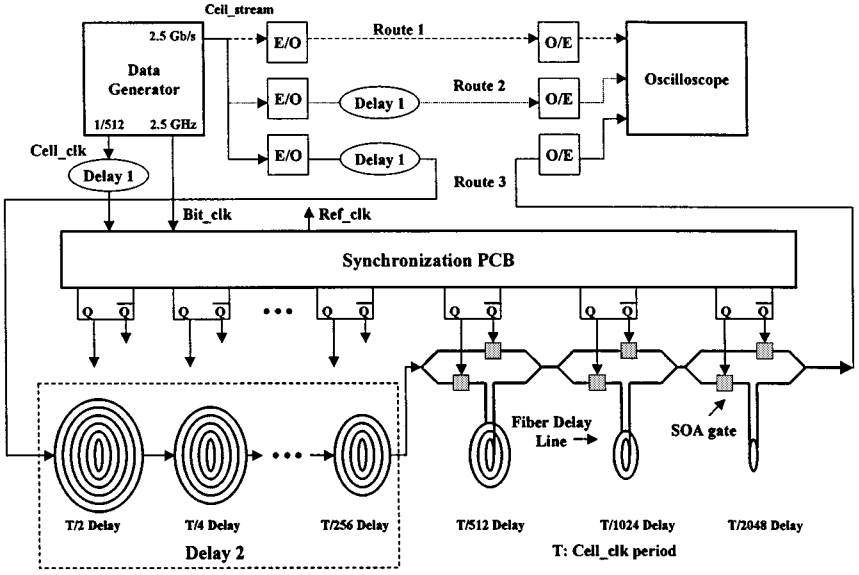


Fig. 19. Testing setup of the cell synchronization unit.

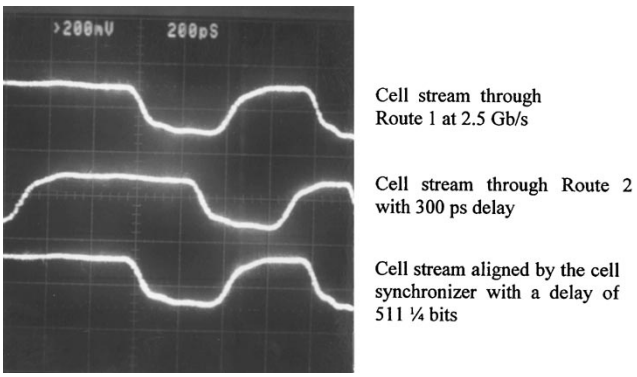
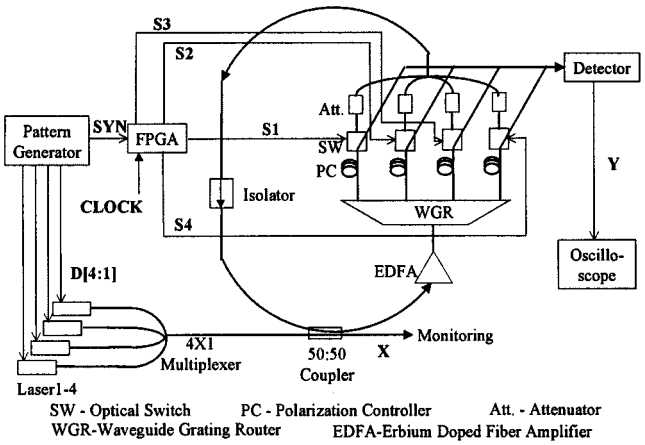
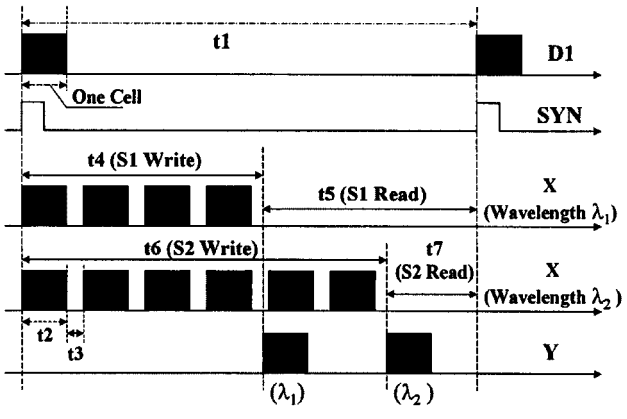


Fig. 20. Fine delay adjustments (200 ps/div).

The testing setup shown in Fig. 19 generates three cell streams at 2.5 Gb/s through Routes 1, 2, and 3. To simplify the testing, instead of using the Cell_clk derived from the cell delineation unit, we use the Cell_clk from the data generator with a frequency of $1/512$ of the bit clock (2.5 GHz). Since the most challenging part of the experiment is to adjust the phase of the incoming cells to the neighborhood of one bit, we only control the last three stages of the delay elements, while the first eight stages are replaced by a fiber line (Delay 2) with a delay of 510 bits. In our setup, we let the Ref_clk synchronize with the Cell_clk. By varying the length of fiber delay line (Delay 1), the phase of the cell stream is set to $1/4, 1/2$, or $3/4$ bit behind the reference clock. The cell synchronizer has correctly delayed the cell stream to align with the reference clock according to the injected delay (Delay 1). Fig. 20 shows the waveform of three cell streams through Routes 1, 2, and 3. The Delay 1 element is set to 300 ps ($3/4$ bit). The cell stream of Route 3, with a pattern of 11010010...1010 (64 bytes), has been shown to delay by 511 $1/4$ bits.



(a)



(b)

Fig. 21. Testing setup for an FPGA-controlled WDM loop memory. (a) Function block diagram and (b) timing diagram.

E. Testing of an FPGA Controlled WDM Loop Memory

We have demonstrated a WDM loop memory controlled by a field programmable gate array (FPGA) chip. The FPGA chip generates various control signals to flexibly configure the loop memory into different setups, e.g., the number of wavelengths,

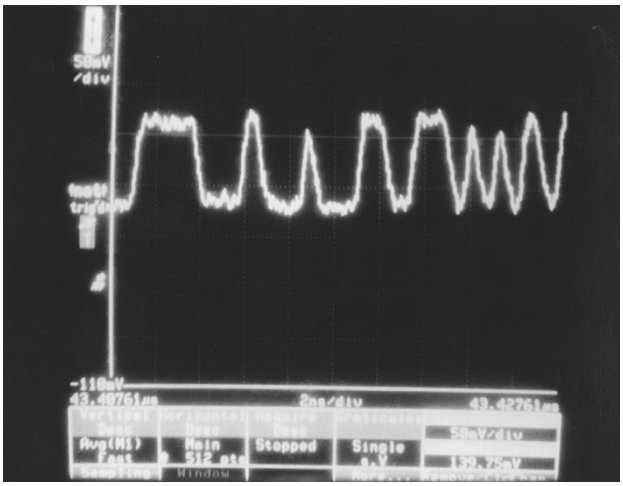


Fig. 22. X-axis: time, 2ns/div; Y-axis: relevant voltage. A partial PRBS pattern of a cell operating at 2.5 Gb/s and circulating up to 23 loops with the wavelength of 1556.5 nm.

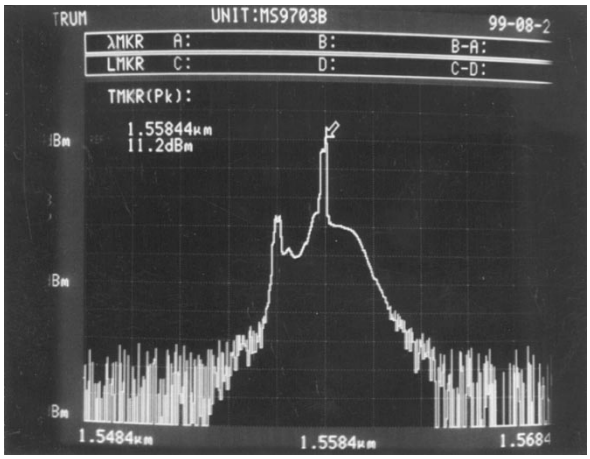


Fig. 23. X-axis: wavelength; Y-axis: relevant power. The optical spectrum of the two WDM cells operating at 2.5 Gb/s.

and the number of circulations of the ATM cell in the loop memory.

The testing setup is shown in Fig. 21. Four bit streams are generated from the Pattern Generator and carried by four different wavelengths. At the rate of 2.5 Gb/s, each consists of a 64-byte cell followed by a string of zero bits. The cell is generated according to pseudorandom binary sequence (PRBS) and its duration (t2) is 205 ns. These four wavelengths are multiplexed by a 4-to-1 multiplexer. Through a coupler, 50% of the power is fed to the loop memory and the other 50% is used for monitoring. The waveguide grating router (WGR) splits the multiplexed wavelengths into four separate paths, each passing a polarization controller (PC), optical switch (SW), and attenuator. The erbium-doped fiber amplifier (EDFA) is used to compensate for the power loss due to multiple circulations in the loop memory. The four optical switches are controlled by the FPGA chip with S1–S4 signals according to the operation modes, e.g., writing cells into the loop memory, reading cells from the loop memory, and circulating cells in the loop memory. Fig. 21(b) shows one of the input bit streams, D1. Two cells carried by λ_1 and λ_2 are monitored at point X, and their waveforms are shown in Fig. 21(b). When these cells are read, they appear at point Y.

In Fig. 21(a), SYN is an input signal to the FPGA chip and synchronizes the control signals to the bit streams $(D[4:1])$ generated from the Pattern Generator. CLOCK is an external clock signal to the FPGA controller, which is independent from the bit streams $(D[4:1])$. The duration of the S1 signal (t4 and t5) corresponds to the write and read cycles, respectively, as does t6 and t7 in the S2 signal. The duration can be adjusted flexibly by the FPGA chip and the adjustment precision is 9 ns. The guard time, t3, is 13%–20% of t2.

Fig. 22 shows a partial PRBS pattern of a cell operating at 2.5 Gb/s and circulating up to 23 loops with the wavelength of 1556.5 nm. Fig. 23 shows the optical spectrum of two WDM cells operating at 2.5 Gb/s, and their corresponding wavelengths (λ_1, λ_2) are 1558.4, and 1556.5 nm, respectively.

To store cells in loop memory for an arbitrary time, a dynamic refresh controller is required to periodically restore the circulating cells to overcome the accumulation of spontaneous emission noise of the optical amplifier. The refresh function for one wavelength has been realized in our previous work with a pulse generator [12]. Based on the above testing results, an enhanced refresh controller for multiple WDM channels in the loop memory is being designed with FPGA chips.

V. Conclusion

We have described an architecture of the photonic ATM front-end processor used in the WDM ATM multicast (3M) switch. It consists of cell delineation, VCI-overwrite, and cell synchronization units. The cell delineation unit identifies cell boundaries. Once cell boundaries are identified, the VPI/VCI and header error control (HEC) fields are replaced optically by the VCI-overwrite unit. The cell synchronization unit is used to align the phases of incoming ATM cells in the optical domain.

The method of performing cell delineation we adopted follows the ITU-T standards by finding the correct cyclic redundancy check (CRC) byte at the fifth byte position of a cell header. We have demonstrated the ATM cell header replacement (including VPI/VCI and HEC bytes) in the optical domain through the integration of the cell delineation and VCI-overwrite units. The subsystems have correctly operated at 2.5 Gb/s.

We have also demonstrated the cell synchronization unit, which adjusts the phases of optical cells at 2.5 Gb/s to a reference cell clock with the adjustment range from 1 to 511 bits and with a precision of $1/4$ bit (or 100 ps). We have adopted a novel sampling method to achieve the 100-ps precision without using a 10-GHz clock. A 1×2 Y-junction SOA switch has been developed and used as the space switch in the cell synchronizer and the WDM loop memory.

The WDM loop memory has been demonstrated to be able to store two WDM cells and circulate them up to 23 turns at 2.5 Gb/s. A dynamic refresh controller for multiple WDM channels in the loop memory is being designed with FPGA chips.

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H. J. Chao (S'82–M'85–SM'95) received the B.S.E.E. and M.S.E.E. degrees from the National Chiao-Tung University, Taiwan, R.O.C., in 1977 and 1980, respectively. He received the Ph.D. degree in electrical engineering from The Ohio State University, Columbus, in 1985.

He is Professor of the Department of Electrical Engineering at Polytechnic University, Brooklyn, NY, which he joined in January 1992. His research interests include terabit IP routers, optical packet switches, and quality of service control in IP/ATM networks. From 1985 to 1991, he was a Member of Technical Staff at Bellcore, NJ, where he conducted research in the area of SONET/ATM broad-band networks. He was involved in architecture designs and ASIC implementations, such as the first SONET-like Framer chip, ATM Layer chip, and Sequencer chip (the first chip handling packet scheduling).

Dr. Chao received the Bellcore Excellence Award in 1987. He served as Guest Editor for the IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS (JSAC) with special topics on "Advances in ATM Switching Systems for B-ISDN" (June 1997) and "Next Generation IP Switches and Routers" (June 1999). He is currently serving as an Editor for the IEEE/ACM TRANSACTIONS ON NETWORKING.

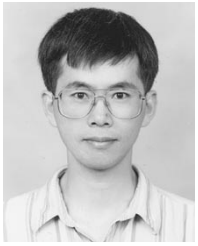
L. Wu (M'97) received the B.S., M.S., and Ph.D. degrees in electronic engineering from Tsinghua University, Beijing, China, in 1988, 1991, and 1997, respectively.

He was a Senior Lecturer in the Department of Electronic Engineering, Tsinghua University from 1994 to early 1997. After his research and development work on multimedia DSP chips in 1997, he joined the Center for Advanced Technology in Telecommunications, the Department of Electrical Engineering, Polytechnic University, Brooklyn, NY, as a Postdoctoral Fellow, working on design and implementation of high-speed digital control circuits and systems utilized in WDM ATM Multicast optical switching systems. He is also working on ASIC design of the ATM switch chips. His current interest is on high-speed digital circuits and systems utilized in optical fiber communications and ASIC design of ATM switch chips and DSP chips.

Dr. Wu received the Tsinghua University Excellence Graduate Award and Medal in 1988.

Z. Zhang was born in Liaoning, China, in 1967. He received the B.Sc. degree in electronic engineering and the Ph.D. degree in opto-electronics from Tsinghua University, China, in 1989 and 1996, respectively.

During 1996, he was with the Department of Electronic Engineering at Tsinghua University, working on optical time-division and wavelength-division multiplexed ATM switching system. From late 1996 to 1998, he was a postdoctoral Fellow with the Department of Electrical Engineering at the Polytechnic University, Brooklyn, NY, working on photonic ATM front-end processor and 3M (WDM, ATM, Multicast) optical switching system. Since early 1999, he has been a Hardware Design Engineer at Fujitsu Network Communications, Inc., Pearl River, NY, working on ATM switching systems. His research interests are in ATM network, photonic packet switching and optical WDM network.



S. H. Yang received the B.S. degree in physics from Soochow University, Taiwan, R.O.C., in 1987, the M.S. degree in electro/optical engineering from the National Chiao-Tung University, Taiwan, in 1989, and the Ph.D. degree in electrical engineering from Polytechnic University, Brooklyn, NY, in 1999.

In 1999, he joined the Transcomm Technology System, Inc., Fremont, CA, where he works in the area of access networks. His research interests are in the area of ATM switches, IP routers, and access network systems.

L. M. Wang received the B.S. degree in physics and the M.S. degree in Optics from the University of Electronic Science and Technology of China, Chengdu, Sichuan, China, in 1985 and 1991, respectively. He received a second M.S. degree in physics from Indiana University–Purdue University at Indianapolis, IN, in 1996. He received the Ph.D. degree in electrical engineering from the University of Maryland Baltimore County (UMBC), Baltimore, MD, in May 1999.

From July 1996 to May 1999, he worked on the opto-electronic devices and their applications in optical access networks and all-optical packet switches. He joined Corning, Inc., Corning, NY, in May 1999, as Senior Scientist in fiber communications. His current interests are dispersion-managed fibers and soliton transmissions.

Y. Chai received the B.S., M.S., and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1986, 1988, and 1992, respectively.

He was a Lecturer and an Associate Professor in the Department of Electronic Engineering, Tsinghua University, Beijing, China, from 1992 to 1996. He joined the faculty of the Department of Computer Science and Electrical Engineering, University of Maryland Baltimore County (UMBC), Baltimore, MD, as a Research Associate from 1996 to 1999. He is now with Tyco Submarine Systems, Ltd., Eatontown, NJ. He worked on tunable semiconductor lasers, laser frequency stabilization, optical FDM transmission, high-speed WDM transmission system, and optical packet switching networks. He has more than 60 publications and presentations, and holds two patents. His current interest is on undersea optical WDM transmission systems and gain-flattened broad-band EDFA.

J. Y. Fan received the B.S. degree in physics from the National Tsinghua University, Taiwan, R.O.C., in 1988, the M.S. degree in electro-optical engineering from the National Chiao-Tung University, Taiwan, in 1990 and the Ph.D. degree in electrical engineering from the University of Maryland Baltimore County (UMBC), Baltimore, MD, in 1999. His Ph.D. work concentrated on the design, fabrication, and implementation of high-speed photonic switching in a photonic IP/ATM system and demultiplexing/multiplexing for TDM system, and wavelength converts for WDM system.

He is now with Nanovation Technologies, Inc., Evanston, IL, where he is doing research work in thin-film photonic devices for optical communications.

F. S. Choa received the B.S. degree from the National Taiwan University, Taiwan, R.O.C., and the M.S. and Ph.D. degrees from the State University of New York (SUNY) at Buffalo, NY.

After his Ph.D. research work on femtosecond infrared lasers and detectors in 1988, he joined AT&T Bell Laboratories, in Holmdel and Murray Hill, NJ, where he worked in the area of photonic integrated circuits and chemical beam epitaxy. Since joining the University of Maryland Baltimore County (UMBC), Baltimore, MD, he has been working in the areas of III–V compound semiconductor material growth and processing, RF-photonic devices and systems, photonic IP/ATM switching, ultrahigh capacity WDM communications and networks, and fiber-optic sensors for biomedical sensing. He has authored and coauthored more than 130 refereed journal and conference publications.

Dr. Choa is a Topical Editor for *Optics Letters* and Associate Editor of the *Journal of High-Speed Networks.*