

Two-Module Stage Optical Switch Network

Hideaki Okayama, *Member, IEEE, Member, OSA*, Yutaka Okabe, Toru Arai, Takeshi Kamijoh, *Member, IEEE*, and Taiji Tsuruoka

Abstract—A large-scale optical switch array based on guided-wave technology using two-module-stage network architecture is proposed. Networks are derived from a generalized three-stage switch network. Two types of architecture are demonstrated. In the first, building blocks in each module are $1 \times n$, $n \times m$ nonblocking switches or $n \times r$ switch that can route limited numbers of input signal. In the second, crossbar, Banyan, or four-stage wide-sense nonblocking network is used as building blocks. The interconnection is simpler than for the first type. Network architectures that use Banyan or wide-sense nonblocking network building blocks are classed as thinned-out Banyan networks.

Index Terms—Banyan, optical switch, switch matrix.

I. INTRODUCTION

THE OPTICAL switch array [1]–[3] is a basic component of any system, such as cross-connects or local area networks, routing optical signals in an optical form. These systems require a large-scale optical switch network that handles numerous input and output ports. An optical switch matrix with a large port number is difficult to fabricate in one chip. Many optical switch matrix devices must be connected to attain large-scale optical switch network. In the generalized crossbar optical switch network [4] [Fig. 1(a)], optical switch matrices must be connected in p ranks when network ports p times the number of each optical switch matrix are required. A three-module stage network such as a Clos network [5] [Fig. 1(b)] is used mainly to attain a large port number. The resultant network based on these conventional architectures has high loss due to the relatively high insertion loss of the optical switch matrix device. Low loss network is expected for a two-module-stage network. Only the tree architecture [6] is known for a two-module-stage expandable network. The tree architecture [Fig. 1(c)] has a problem because the numbers of interconnections and modules are huge.

In this report, we propose expandable two-module-stage networks with fewer interconnections and modules. The networks described are derived from a generalized three-stage switch network. Two types of architecture are shown. In the first, the building blocks in each module are $1 \times n$, $n \times m$ nonblocking switches or $n \times r$ switch that route limited number of input signal [4], [7], and [8]. In the second type, a crossbar, Banyan, or four stage wide-sense nonblocking network is used as building blocks [4]. The interconnection is simpler than that in the first type. Network architectures that use Banyan or wide-sense nonblocking network building blocks are classed as thinned-out Banyan networks [9], [10].

II. GENERALIZED THREE-MODULE-STAGE NETWORK

To obtain a two-module-stage network, we start from a generalized three-module-stage network shown in Fig. 2. Matrix switch $n \times m$ is placed at the input and $m \times n$ at the output. The middle stage $r \times r$ switch are grouped into three layers. The lowest layer consists of P $r \times r$ switches. The middle-layer consists of $m/(PQ)$ groups of lowest layer groups. Q is the number of interconnections connected from a $n \times m$ switch to a $r \times r$ switch. The top layer consists of $m/(PQ')$ middle layer groups. Q' is the number of interconnections those are connected from a $r \times r$ switch to a $m \times n$ switch. Each lowest layer group is connected to each output $m \times n$ switch group. The network is strictly nonblocking when P is larger than $2n/Q - 1$ or $(2n/Q' - 1)$ and rearrangeable when $PQ = n$ ($PQ' = n$).

For routing signals, the $n \times m$ switch sends an input signal to a group of P $r \times r$ switch where a routes to desired output is connected. The $n \times m$ switch selects a route which the $r \times r$ switch and interconnections to $m \times n$ switch with desired output is not fully occupied. The $r \times r$ switch sends the signal to desired $m \times n$ switch and $m \times n$ switch routes the signal to the desired output.

With $m = PQ(Q = Q')$ and $Q = 1$ the network becomes a Clos network. There are several ways to select P , Q , and Q' , but in this report we chose $Q = Q' = 1$, which gives a reasonable port number. We name the network based on Clos network type I (Clos-based) architecture and the second type with $Q = Q' = 1$ or $P = 1$ type II. The interconnection pattern differs in these two architectures. To attain a two-module-stage network, we divide the three-stage network at the middle stage $r \times r$ switch and combine each part of the middle stage $r \times r$ switch with first-stage or third(last)-stage switches. The type II architecture is more easy to rearrange the network into two-module stage due to the segregation of interconnections. Switch elements and interconnections in a module are integrated into a optical switch array chip.

III. TYPE I, CLOS-BASED ARCHITECTURE

The Clos network shown in Fig. 1(b) is strictly-nonblocking when m is larger than $2n - 1$ and rearrangeable when m is larger than n . To divide the middle (second) stage switch and combine parts with first- or last-stage switches, the middle-stage switch must be segregated into several parts. An obvious way is to decomposed the middle stage switch into two-stage switches. In Fig. 3(a), the middle-stage switch is decomposed into $q \times r$ and $r \times q$ optical switch matrices. By combining $q \times r$ and $r \times q$ switches with the first- and last-stage switches, the structure of the module in the two-stage-module network becomes that shown in Fig. 3(b). The first module stage consists of $n \times m$

Manuscript received June 9, 1999; revised December 9, 1999.

The authors are with R&D Group, Oki Electric Industry, Company, Ltd., Hachioji, Tokyo 193-8550, Japan.

Publisher Item Identifier S 0733-8724(00)03034-6.

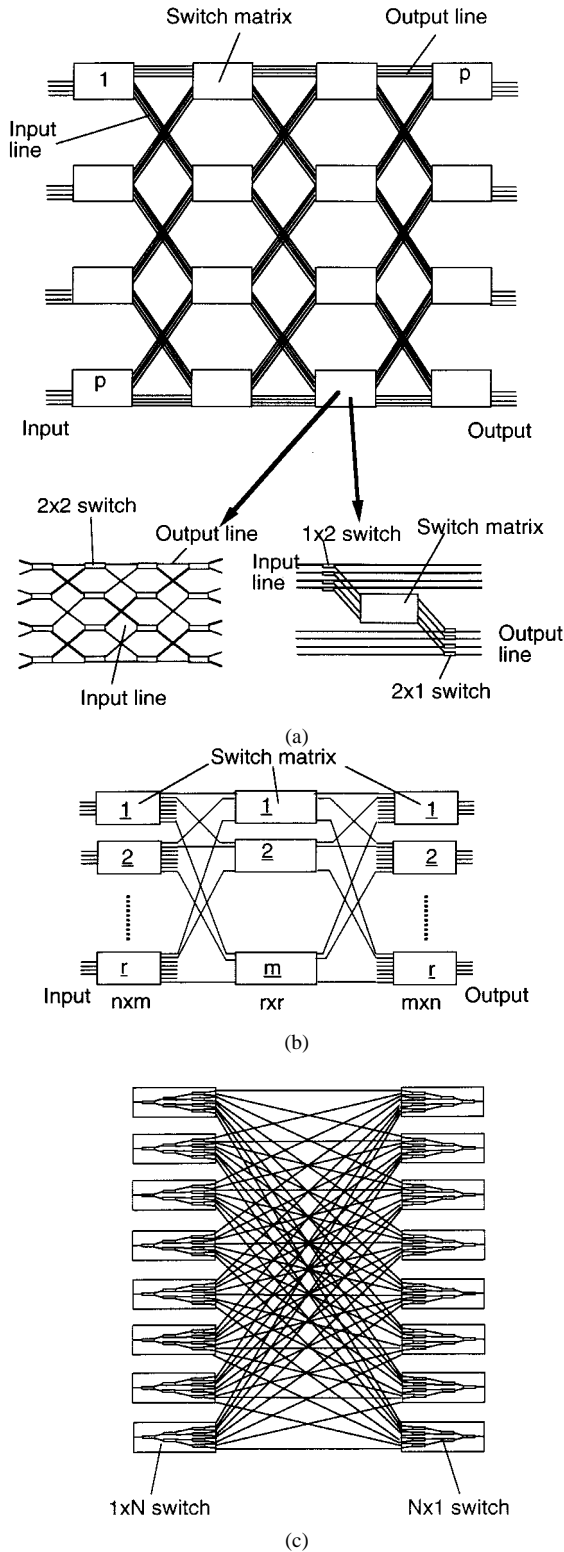


Fig. 1. Conventional multiple module stage architectures: (a) generalized square crossbar, (b) Clos network, and (c) $N \times N$ tree structure.

and $q \times r$ switches. The last module stage is composed of $r \times q$ and $m \times n$ switches.

For the thermo-optic switch [11], the crossbar is preferable for the $n \times m$ and $m \times n$ switches due to power consumption. In the other case, we decompose the $n \times m$ and $m \times n$ switches

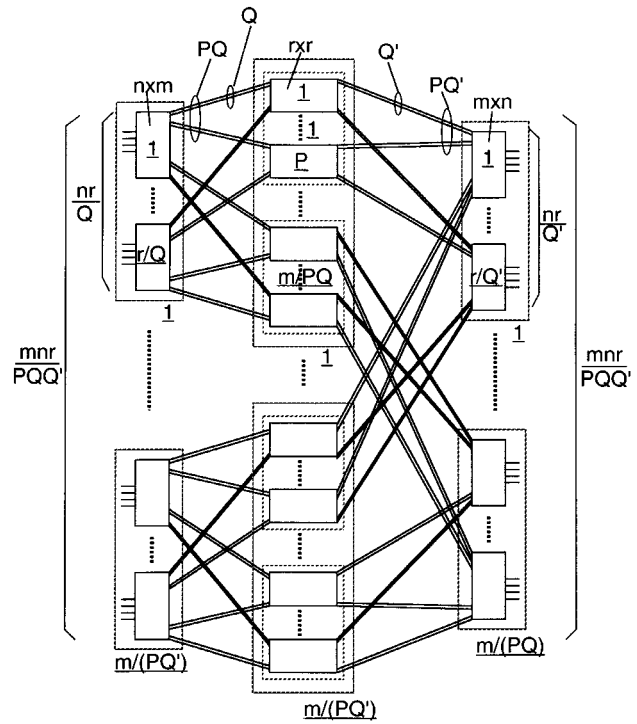


Fig. 2. Generalized three-module-stage architecture.

into a two-stage switch network. We use $q' \times m$ and $n \times q'$ switches in a $n \times m$ switch. The $n \times q'$ and $q \times r$ switches are combined and replaced by an $nq \times q'r$ switch in which only qq' signals are routed (Fig. 4). Due to the limited required permutation of the $nq \times q'r$ switch, the switch structure is simpler than for strictly nonblocking.

For routing signals, $q' \times m$ switch sends input signal to a $nq \times q'r$ switch not fully occupied. Then the $nq \times q'r$ switch sends the signal to a module with desired output. In the output module $q'r \times nq$ switch route the signal to $m \times q'$ switch with desired output and the $m \times q'$ switch sends the signal to the desired output.

A. Architecture with $q = q' = 1$

For $q = q' = 1$, only one signal is handled by the $nq \times q'r$ ($n \times r$) switch. Examples of the $n \times r$ switch routing one signal are shown in Fig. 5. The device in Fig. 5(a) consists a star coupler and optical gates placed at each port. The optical gate at input selects one signal from among various input and the star coupler distributes the signal to all output ports. The optical gate at the output port selects a signal destined for a desired path. The second is a Banyan network [Fig. 5(b)] constructed with \log_2 (output port number) stages of 2×2 switch elements. The Banyan network is capable of routing one signal to any output. The optical switch using an arrayed-waveguide structure [8], [12] [Fig. 5(c)] also routes one signal among many input ports to a destination. A small-scale $q' \times m$ switch is used instead of the $n \times m$ switch in Fig. 3(b). The $q \times r$ ($q = 1$) switch in Fig. 3(b) and $n \times r$ switch in Fig. 4 have essentially the same complexity.

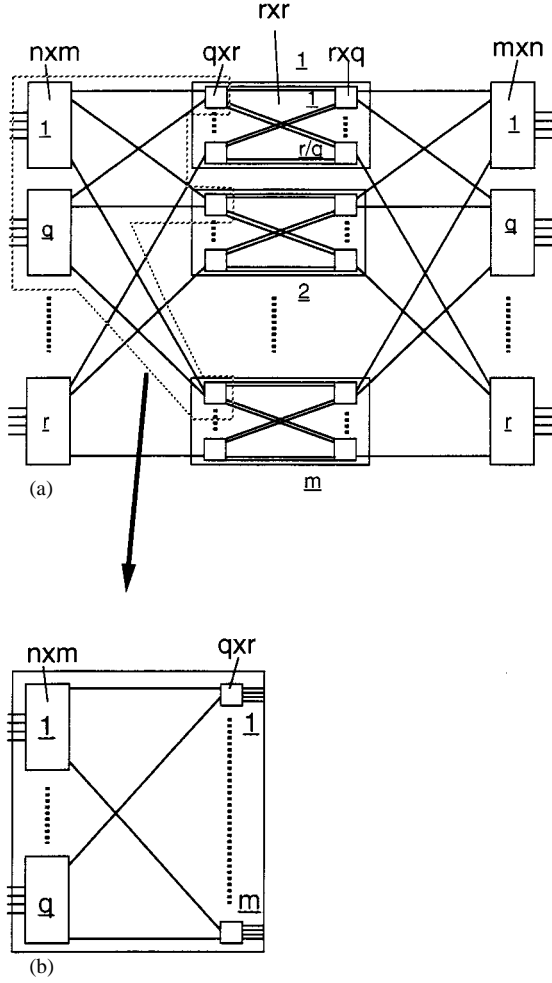


Fig. 3. Type I two-module-stage Clos-based network.

Another application of this network is as a router using combination of electronic and optical routing. Using the electronic router [13] as a $q' \times m$ switch and the optical switch (Fig. 5) as an $n \times r$ switch, we implement a large-scale high-bandwidth router. The total number of electronic routers is $2N/q'$ and optical switches $2mr$. Several optical switches must be integrated to reduce the number of optical switch modules.

B. Architecture with $q = q' = q'' = 1$

For $q = q' = q'' = 1$, the network in Fig. 4 becomes equal to that of [4]–[6]. The network consists of $1 \times m$ and $n \times r$ switches. The device in Fig. 5 is used for both $1 \times m$ and $n \times r$ switches. For $n = r$ the network becomes similar to the extended generalized shuffle (EGS) network [14] with $1 \times m$ fan-out at the input, two stage $r \times r$ switches each routing one signal and $m \times 1$ fan-in at the output. Strictly nonblocking condition for Fig. 4 network with $n = r$ shows much wide range than for the EGS network (Fig. 6).

Since the network is based on a tree architecture, crosstalk is low. Crosstalk generated at $1 \times m$, $n \times r$, and $r \times n$ switches is rejected at the $m \times 1$ switch at the last-stage module. Second-order crosstalk is generated at $n \times r$ and $r \times n$ switches which contribute a little to the crosstalk. The crosstalk of the network

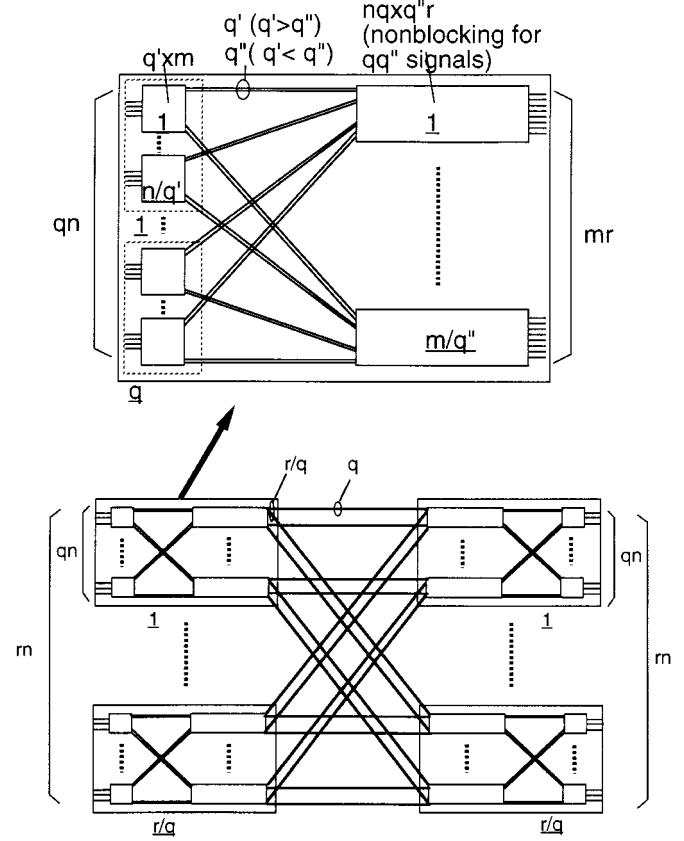
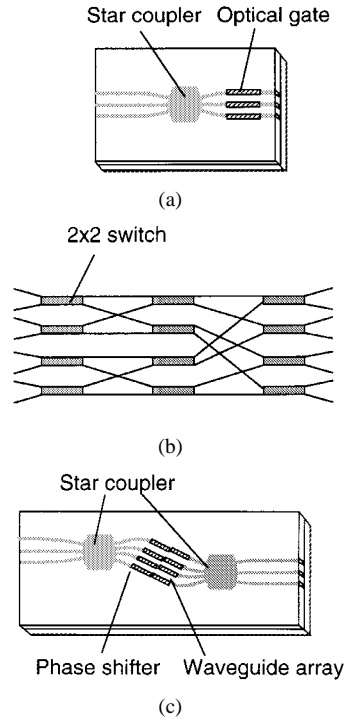
Fig. 4. Type I network using $nq \times q''r$ switch with limited nonblocking.

Fig. 5. Multiple input and output port switches routing one signal.

using devices in Fig. 5(a) and (c) is shown in (1) to a second-order approximation with X_s being the device crosstalk

$$SXR = 2X_s - 10 \log_{10}(n + r + m). \quad (1)$$

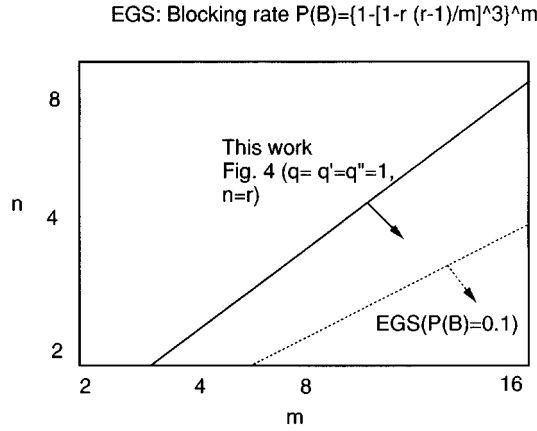
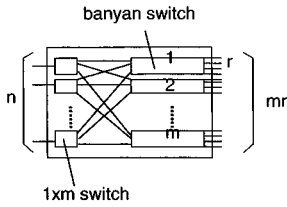


Fig. 6. Comparison between type I and extended generalized shuffle network.

TABLE I
TYPE I FEATURES FOR r NUMBER

| Strictly nonblocking: $m=2n$ | | | | |
|------------------------------|---------------|----------------|----------------|-------------------------------|
| | sw input n | sw output mr | modules $2r$ | Total inter-connection r^2m |
| $m=r$ ($r=2n$) | $(N/2)^{1/2}$ | $2N$ | $2(2N)^{1/2}$ | $(2N)^{3/2}$ |
| $r=n$ | $N^{1/2}$ | $2N$ | $2N^{1/2}$ | $2N^{3/2}$ |
| $r=n/2$ | $(2N)^{1/2}$ | $2N$ | $2(N/2)^{1/2}$ | $2^{1/2} N^{3/2}$ |



By constructing the $1 \times m$ switch with a cascade of 1×2 switches ($\log_2 m$ stages: binary tree) and using the Banyan network as an $n \times r$ switch, the network becomes a thinned-out Banyan network. Several features are changed by selection of r . Features for $r = 2n$, $r = n$, and $r = n/2$ are shown in Table I. The switch input number increases and total interconnection number decreases with decreasing r (module number). The output number remains the same. The total switch number in a module $T_s = n(m-1) + mr \log_2(r)/2$ and increases with decreasing r . With $n = N/r$ and $m = 2n$,

$$T_s = N(2N/r + r \log_2 r - 1)/r. \quad (2)$$

There would be optimum value for r . In our report we select $r = n$. For 64×64 network $T_s = 504$ which is almost equal to the switch element number of 16×16 double crossbar. Module features is shown in Table II compared to a known two-stage-module architecture, i.e., tree architecture. The switch element stage increases for one stage and output ports twice, but total interconnection and module numbers are reduced. The total switch number in the network is $[2 + \log_2(r)]/r$ times that of the tree architecture for very large N .

TABLE II
COMPARISON BETWEEN $N \times N$ TREE AND TYPE I STRUCTURE

| | Tree | This work |
|-----------------------|--------------------|----------------------------|
| SW element number | \triangle | \circ |
| Total interconnection | \times N^2 | \circ $2N^{3/2}$ |
| SW output row | \triangle $N/2$ | \triangle N |
| SW rank number | \circ $\log_2 N$ | \triangle $\log_2 N + 1$ |
| Module number | \times $2N$ | \circ $2N^{1/2}$ |
| Total | \times | \circ |

Banyan nxr switch

\circ Good \triangle Fair \times Poor

The crosstalk of the network using a Banyan is shown in (3). Due to fewer crosspoints with other paths in the binary tree and Banyan network, crosstalk is less than in (1)

$$SXR = 2X_{se} - 10 \log_{10}(\log_2 n + \log_2 r + \log_2 m) \quad (3)$$

where X_{se} is switch element crosstalk.

C. Network for Thermo-optic (TO) Switch ($q = 1$)

For the TO optical switch, which uses refractive index change due to temperature change induced by a heater electrode, the crossbar architecture is desirable to reduce total drive power. The $n \times m$ switch in Figs. 2 and 3 must use a crossbar architecture. In this case the module structure becomes that shown in Fig. 3(b).

Total switch elements in one module become $m(n+r-1)$ for a basic crossbar and $m(2n+r-1)$ for a double crossbar. For a strictly nonblocking N -port network with $m = 2n$, the total switch element number in one module is $2N(N/r + r - 1)/r$ and (4) for basic and double crossbar, respectively

$$T_s = 2N(2N/r + r - 1)/r. \quad (4)$$

For $N = 32$ and $r = 8$, the total switch element number in one module becomes 94% of 8×8 double crossbar devices. For $N = 64$ and $r = 8$, the total switch element number in one module becomes 72% of 16×16 double crossbar devices. For $N = 64$ and $r = 16$, the total switch element number in one module becomes 143% of 8×8 double crossbar devices. The total switch element number of the network is $2r$ times that of each module. For very large N the total switch element number becomes $4/r$ times that of the tree architecture.

The network crosstalk is shown in (5).

$$SXR = 2X_{se} - 10 \log_{10}(n + \log_2 r + m). \quad (5)$$

IV. TYPE II ARCHITECTURE

The three-stage architecture in two extreme cases, $Q = 1$ and $P = 1$ is shown in Fig. 7(a) and (b) respectively. We start with Fig. 7(a) ($Q = 1$) for the type II. It is expected that the network is strictly nonblocking when P is larger than $2n - 1$, following the method of Clos. To make the structure different from the Clos network, m/P should be larger than two. These leads to m larger than $4m - 2$. To obtain a two-module-stage network, we

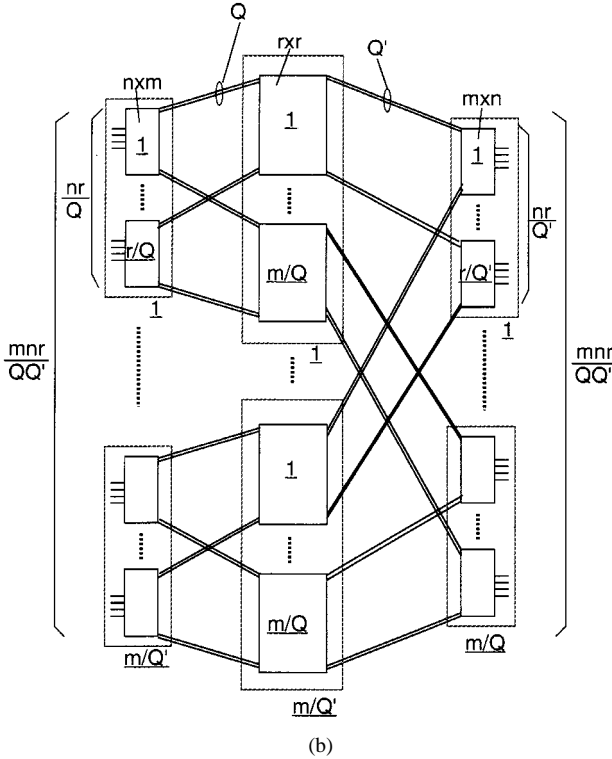
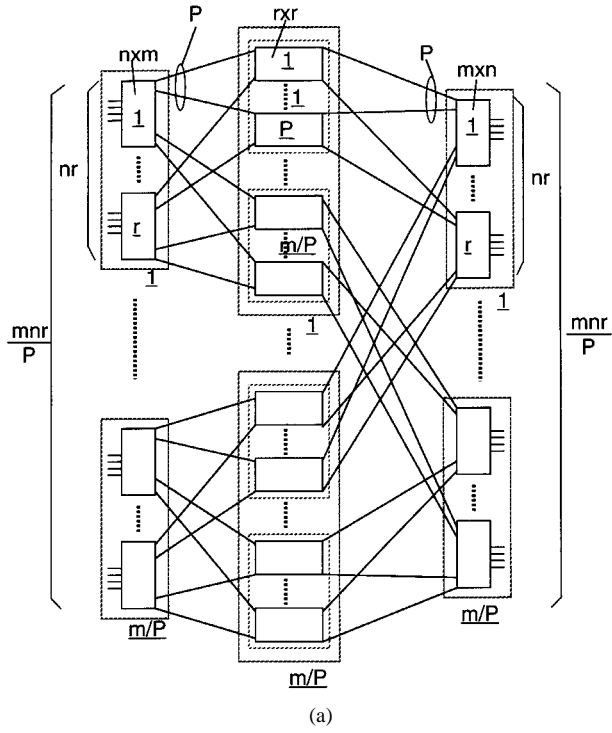


Fig. 7. Generalized three-module stage network used as a basis for type II structure.

simply divide the middle stage $r \times r$ switch in the middle. Half of the $r \times r$ switch is combined with the first-stage $n \times m$ switch to obtain the first module stage (Fig. 8). The remaining half of the $r \times r$ switch is combined with the last-stage $m \times n$ switch to obtain the last module stage. We proceed with two strategies to simplify the structure as of Fig. 8. In the first (Section IV-A), we chose $n = 1$ and use a crossbar or 4×4 wide-sense-nonblocking switch for the middle-stage $r \times r$ switch. In the second

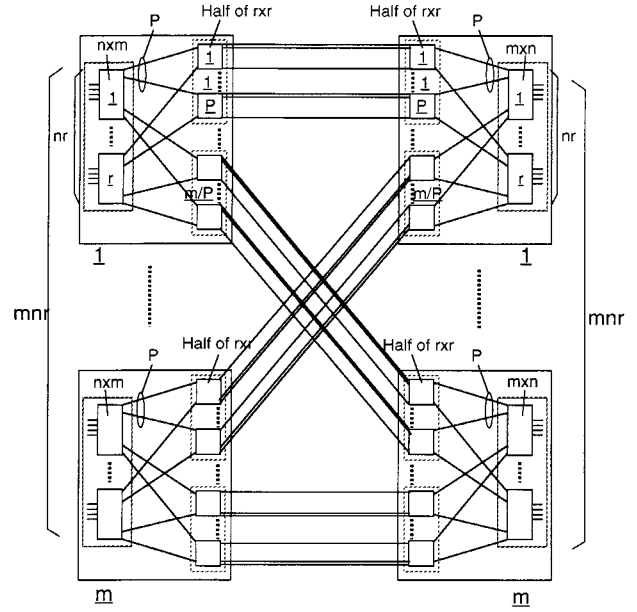


Fig. 8. Type II two-module stage architecture.

(Section IV-B), we replace $n \times m$ and $r \times r$ with switch network composed of $q' \times m$, $n \times 1$ ($n \times m$), and $1 \times r$ ($r \times r$) switches as in Section III.

Routing of the signal in Fig. 8 is done as the same as in Section II. The divided two part of $r \times r$ switches should be operated consistently to route signal as a single $r \times r$ switch.

A. Type II Structure with $n = 1$ ($P = 1$: Strictly Nonblocking)[4]

The $n \times m$ switch becomes a $1 \times m$ switch and a cascaded 1×2 binary tree structure known to be the simplest way of constructing a $1 \times m$ switch can be used. The network started from Fig. 7(b) becomes the same for $n = 1$ and $Q = 1$. The $r \times r$ middle-stage switch is implemented using a crossbar, 4×4 wide-sense-nonblocking, or $r \times r$ tree structure. To implement a low-crosstalk optical switch network, we use a dilated (double) crossbar and 4×4 wide-sense-nonblocking network (Fig. 9). The structure becomes a conventional $N \times N$ tree structure with r groups of $1 \times N$ binary trees integrated into a module when using a tree structure for $r \times r$. For the TO optical switch, a crossbar is preferable in power consumption.

The interconnection pattern is much simpler than that for type I. A patterned bundle fiber is used and the required bundle number is m^2/P , about $2N/r$ for strictly nonblocking.

The switch element number in one module is $r(m - 1) + mr^2/2$ for basic and $r(m - 1) + mr^2$ for a double crossbar. Using $N = mr$, the switch element number is given by (6) (Fig. 10).

$$T_s = N(N + m - 1)/m \quad (6)$$

A 32×32 network is implemented using 16 modules with module complexity almost equal to an 8×8 double crossbar switch. A 32-Clos network requires 24-double crossbar 8×8 switches. A 64×64 network is implemented using 32 modules with module complexity almost half of a 16×16 double crossbar switch. The 64-Clos network requires

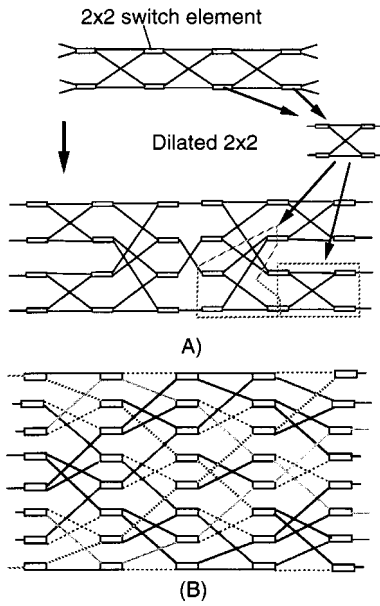


Fig. 9. Dilation of networks. (a) Dilated 4×4 wide-sense nonblocking network. (b) Dilated 4×4 square crossbar.

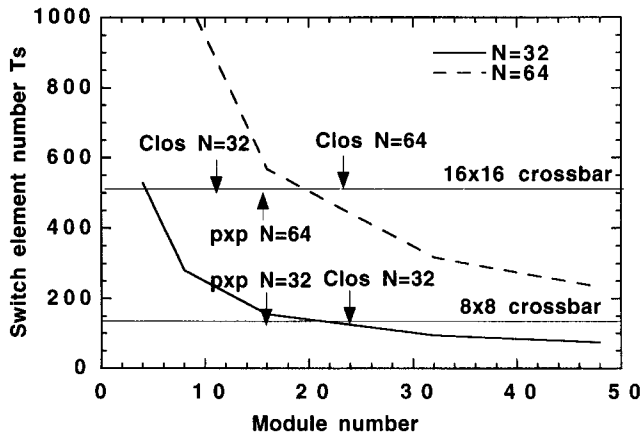


Fig. 10. Switch element number in one module.

24-double crossbar 16×16 switches. The crosstalk is the same as in (5). For $N = 32$ and $m = 8$, the total switch element number in one module becomes 120% of 8×8 double crossbar devices. For $N = 64$ and $m = 8$, the total switch element number in one module becomes 111% of 16×16 double crossbar devices. These numbers are slightly higher than for a Clos-based structure (4). For $N = 64$ and $r = 16$, the total switch element number in one module becomes 62% of 16×16 double crossbar devices. The total switch number in the network is $2m$ times that of a single module. The total switch element number in the network is equal to the tree architecture for very large N .

The 8×8 switch using 4×4 wide-sense-nonblocking network is shown in Fig. 11. The network is a thinned-out-Banyan switch we proposed [10]. The open circle represents $n \times m$ ($n = 1, m = 2$) switch in Fig. 8 and closed circle the $r \times r$ ($r = 4$) dilated wide-sense nonblocking network (Fig. 9). Network features are detailed in [9] ($T_s = 4N - 4$, total interconnection = $N^2/4$). Two types of type II structure is compared

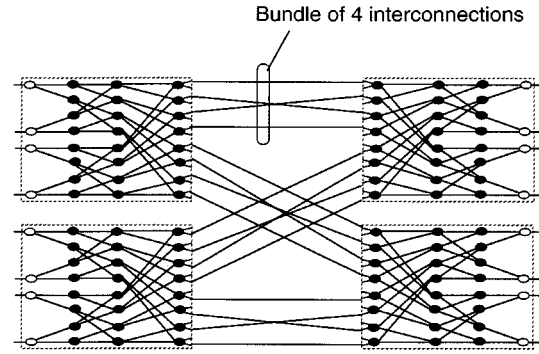


Fig. 11. Wide-sense-nonblocking dilated 8×8 thinned-out Banyan network.

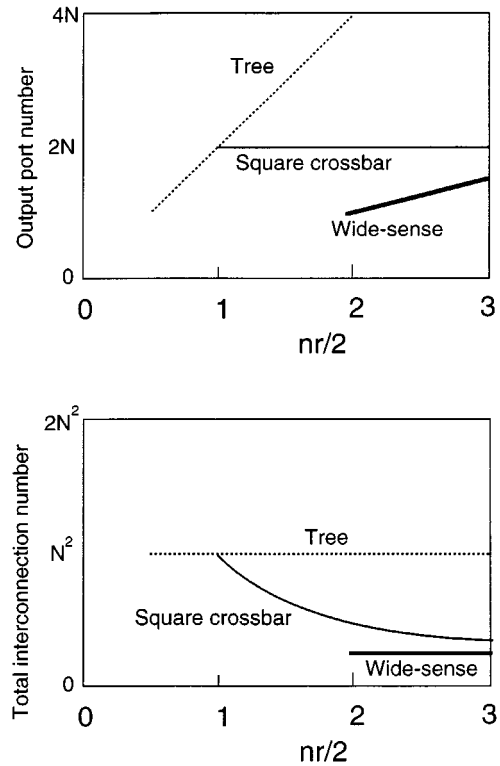
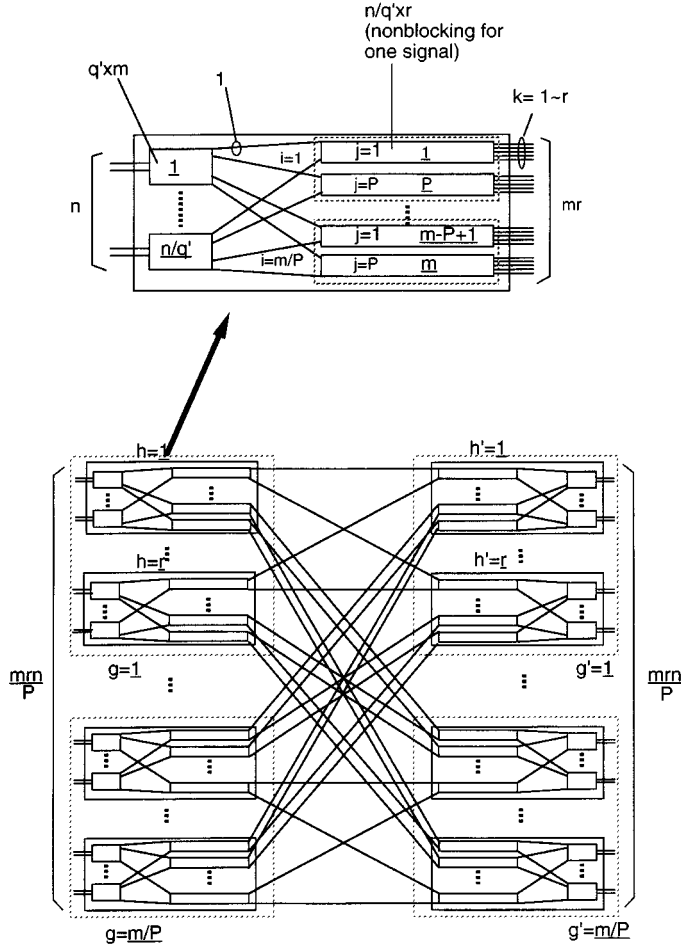


Fig. 12. Characteristics of type II.

with $N \times N$ tree structure in Fig. 12. The horizontal axis shows input port number of a module divided by 2. The tree architecture in Fig. 12 is an architecture composed of integrated array of one to many binary tree switch in a module. The architecture is obtained using tree architecture for $r \times r$ switch in Fig. 8. The module numbers are the same for all the architectures shown in Fig. 12. The interconnection is simplified at the expense of output port number. Architectures using crossbar or wide-sense nonblocking network are more efficient in simplifying interconnections.

B. Type II Structure Using Tree-Structured $n \times m$, $m \times n$, and $r \times r$

The $n \times m$ switch is decomposed into $q' \times m$ and $n \times 1$ switches. The $m \times n$ switch is decomposed into $1 \times n$ and $m \times q'$ switches. The $r \times r$ middle stage switch is decomposed into $1 \times r$ and $r \times 1$ switches. The resulting two-module-stage network is

Fig. 13. Type II structure using $n \times r$ switch with limited nonblocking.

shown in Fig. 13. The $n/q' \times r$ or $r \times n/q'$ switch in which only a single signal is routed, is used similar to Section III-B, but the interconnection between two modules is different.

At the input stage, we denote k (from 1 to r) as output number of $n/q' \times r$ switch. The $n/q' \times r$ switch is grouped into P switches and we denote the switch number in a group as j (from 1 to P). The group number is i (from 1 to m/P). The $m n/q' \times r$ switches and $n/q' q' \times m$ switches constitutes a module. The modules are grouped into r modules. The module number in a module group is h (from 1 to r). The module group number is g (from 1 to m/P). At the output stage, we denote k' (from 1 to r) as input number of $r \times n/q'$ switch. The $r \times n/q'$ switch is grouped into P switches and we denote the switch number in a group as j' (from 1 to P). The group number is i' (from 1 to m/P). The $m r \times n/q'$ switches and $n/q' m \times q'$ switches constitutes a module. The modules are grouped into r modules. The module number in a module group is h' (from 1 to r). The module group number is g' (from 1 to m/P). The connection between output of the input module and input of the output module is done to establish relations $k' = h, h' = k, i' = g, g' = i, j' = j$.

The characteristics of the network are the same as that described in Section III-B.

A module using arrayed waveguide switches with planar waveguide interconnection (Fig. 14), [8] is a modified version

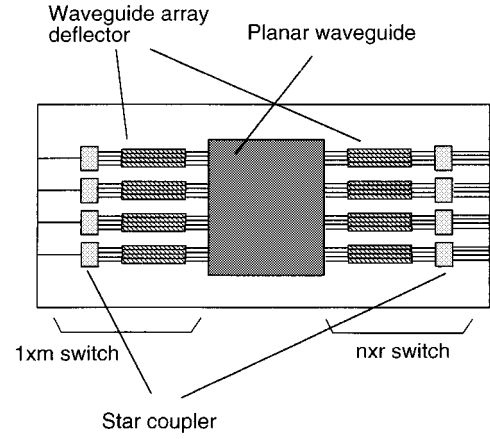


Fig. 14. Module of Fig. 13 using arrayed waveguide switch and planar waveguide interconnection.

of devices of [15] and [16]. $1 \times m$ input switch (deflector) and $n \times r$ switch (deflector) are connected by interconnection using a planar waveguide. Each deflector is composed of a star coupler and waveguide array with phase controller. The input light is divided among waveguide array at the star coupler. By controlling the phase at the waveguide array, the light wave front is tilted and propagation direction in the planar waveguide is directed to a desired $n \times r$ switch. The light fed into waveguide array of the $n \times r$ switch is phase controlled to focus the light power into a desired output at the star coupler. The structure eliminates complex interconnection in a module. Other types of deflectors such as a turning mirror can be used instead of a waveguide array deflector.

V. SUMMARY

A large-scale optical switch array based on guided-wave technology using a two-module stage network architecture is proposed. Two types of network described are derived from a generalized three-stage switch network. Building blocks in each module are $1 \times n, n \times m$ nonblocking, or $n \times r$ switches that route limited numbers of input signals. Crossbar, Banyan, or four-stage wide-sense nonblocking networks are used as building blocks. Network architectures that use Banyan or wide-sense nonblocking network building blocks are classed as thinned-out Banyan network.

Interconnection and module numbers are reduced compared to known two stage module architecture (tree architecture). Among various types the Type II wide-sense nonblocking network (Fig. 9) exhibits smallest T_s , but the module number scale as $N/4$. T_s of the Type II crossbar (Section IV-A) is the largest. The output switch row number in a module is the same for all types. The module output fiber number of type II wide-sense nonblocking network is half of that in other networks. The total interconnection number of the type II wide-sense nonblocking network can be very large but is $1/4$ of the tree structure. For module number larger than $2N^{1/2}$ the total interconnection number of type I Banyan network (Section III-B and IV-B) is less than type II crossbar network. Type I Banyan network is preferable concerning switch number in a module T_s and total interconnection number. However, for the TO switch network

using crossbar architecture (Section III-C) is advantageous concerning power consumption. The module structure can be simplified using one stage light beam steering device such as arrayed waveguide switch or turning mirror.

REFERENCES

- [1] I. P. Kaminow and T. L. Koch, Eds., *Optical Fiber Telecommunications III-B*. London, U.K.: Academic, 1997, ch. 10.
- [2] H. S. Hinton, *An Introduction to Photonic Switching Fabrics*. New York: Plenum, 1993, ch. 3.
- [3] R. A. Spanke, "Architectures for guided-wave optical switching systems," *IEEE Commun. Mag.*, vol. 25, pp. 42–48, 1987.
- [4] H. Okayama, Y. Okabe, T. Arai, T. Kamijoh, and N. Sakamoto, "Optical switch network based on two module stage architecture," *IEICE*, Tech. Rep. SSE98-172, 1998.
- [5] C. Clos, "A study of nonblocking switching networks," *Bell Syst. Tech. J.*, vol. 31, pp. 443–468, 1952.
- [6] R. A. Spanke, "Architectures for large nonblocking optical space switches," *IEEE J. Quantum Electron.*, vol. QE-22, pp. 964–967, 1986.
- [7] H. Okayama, Y. Okabe, T. Arai, and N. Sakamoto, "Optical switch network using two stage module architecture," in *Proc. General Conf. IEICE*, Mar. 1999, B-12-10.
- [8] H. Okayama, Y. Okabe, T. Arai, and T. Tsuruoka, "Waveguide array optical switching element," *IEICE*, Tech. Rep. PS99-5, Apr. 1999.
- [9] H. Okayama, Y. Okabe, T. Kamijoh, and N. Sakamoto, "Optical switch array using Banyan network," *IEICE Trans. Commun.*, vol. E82-B, pp. 365–372, 1999.
- [10] H. Okayama, Y. Okabe, and T. Kamijoh, "Large-scale optical switch array," in *Tech. Digest Photon. Switching*, Sendai, Japan, Apr. 1996, PThB2, pp. 174–175.
- [11] T. Goh, A. Himeno, M. Okano, H. Takahashi, and K. Hattori, "High-extinction ratio and low-loss silica-based 8x8 strictly nonblocking thermooptic matrix switch," *J. Lightwave Technol.*, vol. 17, pp. 1192–1197, 1999.
- [12] M. Bachmann, Ch. Nadler, P. A. Besse, and H. Melchior, "Compact polarization-insensitive multi-leg 1×4 Mach-Zehnder switch in In-GaAsP/InP," in *Proc. 20th European Conf. Opt. Commun.*, Firenze, Italy, Sept. 1994, pp. 519–522.
- [13] S. Keshav and R. Sharma, "Issues and trends in router design," *IEEE Commun. Mag.*, pp. 144–151, May 1998.
- [14] T. J. Cloonan, G. W. Richards, F. B. McCormick, and A. L. Lentine, "Extended generalized shuffle network architectures for free-space photonic switching," in *Proc. Photon. Switching*, Salt Lake City, Mar. 1991, pp. 43–47.
- [15] H. Okayama and M. Kawahara, "Experiment on deflector selector optical switch matrix," *Electron. Lett.*, vol. 28, pp. 638–639, 1992.
- [16] C. R. Doerr and C. Dragone, "Proposed optical cross connect using a planar arrangement of beam steerers," *IEEE Photon. Technol. Lett.*, vol. 11, pp. 197–199, 1999.

Hideaki Okayama (M'94) received the B.S. and the M.S. degrees in applied physics and physics from Waseda University, Tokyo, Japan, in 1981 and 1983, respectively. He received the Ph.D. degree in 1994.

In 1983, he joined the Oki Electric Industry Company, Ltd., Tokyo, Japan, where he has been engaged in research on guided-wave optoelectronics and optical communication subsystems.

Dr. Okayama is a member of the Japan Society of Applied Physics, and the Optical Society of America (OSA).

Yutaka Okabe received the B.S. and the M.S. degrees in applied chemical from Waseda University, Tokyo, Japan, in 1983 and 1985, respectively.

In 1985, he joined the Oki Electric Industry Company, Ltd., Tokyo, Japan, where he has been engaged in research on semiconductor device processing, organic material and guided-wave optoelectronics.

Mr. Okabe is a member of the Society of Polymer Science of Japan and the Japan Society of Applied Physics.

Toru Arai received the B.S. degree in material chemistry from Yokohama National University, Kanagawa, Japan.

In 1987, he joined the Oki Electric Industry Company, Ltd., Tokyo, Japan, where he has been engaged in research on superconductive ceramic, ultrasonic transducers, high-frequency dielectric resonators, and guided-wave optoelectronics.

Mr. Arai is a member of the Ceramic Society of Japan.

Takeshi Kamijoh (M'97) received the B.S. degree in 1976 and the D.Eng. degree in 1982 both from the Hosei University, Japan.

In 1982, he joined the Oki Electric Industry Company, Ltd., Tokyo, Japan, where he is currently Project Organizer of the Advanced Photonic Devices Project. His research interests include optical semiconductor materials and optical device development.

Dr. Kamijoh is a member of the Japan Society of Applied Physics, the Japan Physics Society, and the American Institute of Physics.

Taiji Tsuruoka was born in Tokyo, Japan, on June 16, 1950. He received the B.S. degree in material science from the University of Electro-Communications, Tokyo, in 1974.

He joined the Oki Electric Industry Company, Ltd., Tokyo, in 1974, where he is currently a Research Team Leader of waveguide device team. He had engaged in research in the microwave integrated circuit, bubble memory, thermal printer head, superconductor device, guided-wave optoelectronics.

Mr. Tsuruoka is a member of the Japan Society of Applied Physics and IEICE of Japan.