Pulsed Injection Locking Dynamics of Passively Mode-Locked External-Cavity Semiconductor Laser Systems for All-Optical Clock Recovery

B. K. Mathason and P. J. Delfyett

***Abstract*—The performance characteristics of a pulse injection locked, passively mode-locked (PML) external-cavity semiconductor laser system for all-optical clock recovery are investigated in detail. It is important to characterize the clock recovery dynamics to understand the fundamental capabilities and limitations of the clock recovery system. It is experimentally shown that these devices offer robust clock recovery with low phase and amplitude noise, low injected data power requirements, large frequency locking bandwidth, large phase tracking bandwidth, short lockup time, long dephasing time and immunity to bit-pattern-effects. Harmonic clock generation and subharmonic clock generation are demonstrated for data-rate conversion applications.**

***Index Terms*—Mode-locked semiconductor lasers, optical clock recovery, optical communications, semiconductor optical amplifiers (SOA's).**

I. Introduction

ONE of the most critical components in a high-speed photonic data network is the clocking signal. To perform high-speed all-optical signal processing, including demultiplexing and regeneration, all-optical clock recovery is essential. Techniques for all-optical clock extraction have been demonstrated using self-pulsating laser diodes [1]–[3], passively mode-locked (PML) semiconductor lasers [4]–[9], and fiber lasers using fiber [10], [11] and semiconductor [12], [13] nonlinearities. Of the various techniques demonstrated, PML semiconductor lasers are significant because they typically exhibit less phase and amplitude noise than self-pulsating lasers and less clock latency than fiber based devices.

In this paper, clock recovery dynamics are characterized for PML external-cavity semiconductor laser systems. This study has two purposes: first, to show that PML semiconductor lasers offer promise for all-optical clock recovery by demonstrating their ability to *robustly* synchronize to an external optical data signal by pulse-injection-locking, and second, to characterize the critical performance factors for all-optical clock recovery systems and to provide insight into the experimental techniques for measuring their characteristics.

It is also demonstrated that PML lasers are capable of harmonic clock generation, for synchronization of ultrafast clocking signals with low-speed data signals, and subharmonic clock generation, which may be combined with all-optical switching [14], [7] for all-optical data rate conversion.

Manuscript received October 14, 1999; revised April 17, 2000. This work has been supported in part by the National Science Foundation under Grants ECS-95-22267 and ECS-96-29066.

The authors are with the Center for Research and Education in Optics and Lasers (CREOL), Department of Electrical and Computer Engineering, School of Optics, University of Central Florida, Orlando, FL 32816 USA.

Publisher Item Identifier S 0733-8724(00)06475-6.

II. System Description

Fig. 1 illustrates an experimental schematic for all-optical clock recovery by pulse injection locking of a PML semiconductor laser. The data signal, generated by a hybridly mode-locked semiconductor laser system, is injected into the clock oscillator using a pellicle beamsplitter with small reflectance ($\sim$4%) to minimize cavity losses in the clock oscillator and to minimize insertion loss for the data signal ($\sim$0.2 dB). The clock recovery oscillator consists of a semiconductor optical amplifier (SOA) inside an external optical cavity, with a multiple-quantum-well saturable absorber (SA) located at the back reflector. Objective lenses are used to collect and collimate the output of the SOA. Focusing lenses are used at the cavity mirrors to increase cavity stability. Focusing on the SA, at the backreflector, also provides a higher optical intensity for saturating the absorber and a small spot size to reduce the absorption recovery time through carrier diffusion out of the excited region. It should be noted that in these experiments, the data pulses are injected into the gain element in clock recovery oscillator. As a result, the primary mechanism for clock recovery in these experiments is gain saturation.

The SOA is an AlGaAs angled-striped, gain-guided, double heterostructure device with peak emission at $\sim$830 nm [15]. Devices of 350- and 500-μm length have been used to demonstrate clock recovery. The SOA is dc biased slightly above the threshold for passively mode-locked operation, producing a periodic stream of 5–6 ps pulses with an average output power of $\sim$1.2 mW (4 pJ/pulse).

The clock recovery oscillator is PML by the intracavity multiple-quantum-well SA. The saturable absorber consists of 100 periods of 70-Å GaAs quantum wells separated by 100-Å AlGaAs barriers with 30% aluminum. The sample is grown by MBE on a 500-Å layer of AlAs on a GaAs substrate [16]. The SA is proton-implanted with a single dose of 200-keV protons with a density of $\sim 20^{13}$ cm^{-2} to reduce the absorption recovery time, which is measured to be $\sim$280 ps [17]. The saturable absorber is attached to a high reflector and used as the rear reflector of the laser cavity [18]. The saturable absorber locks the phase of the cavity longitudinal modes, resulting in mode-locked pulse generation. Ultrashort pulses are built-up from the large optical noise transients in the spontaneous emission of the SOA. The

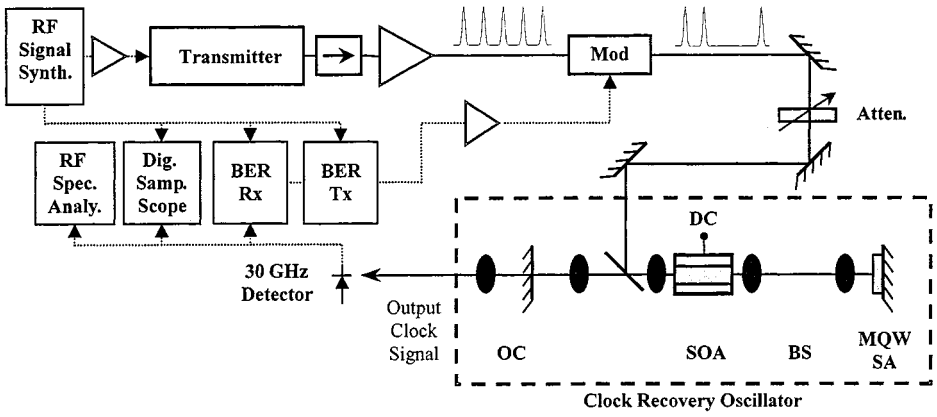


Fig. 1. Experimental scheme for all-optical clock recovery.

pulse repetition rate is determined by the round trip cavity lifetime, $f_{\rm rep} = 1/T = 2L/nc$, where L is the cavity length, T is the period, n is the effective index of refraction and c is the speed of light. The resonant cavity has a round trip lifetime of 3.2 ns, corresponding to a fundamental repetition rate of 311 MHz.

To characterize the optical clock signal, the clock oscillator's output is received by a high-speed photodetector (30 GHz). The output of the photodetector is connected to one of several diagnostic systems (Fig. 1), including an RF spectrum analyzer for spectral analysis, a digital sampling oscilloscope (DSO) for temporal characterization, and a bit-error rate (BER) receiver for signal error analysis. For some experimental measurements on the DSO, the signal is amplified by a low bandwidth amplifier (500 MHz) to minimize aliasing effects due to the high-frequency components (from the short pulsewidth) of the clock signal.

III. Theory of Operation

The mechanisms that establish PML in the clock recovery oscillator are also responsible for phase locking to an injected data signal for clock recovery. The theory of PML with a slow saturable absorber, where the pulsewidth is much shorter than the absorption recovery time, is well understood [19], [20] and models have been presented for pulse injection locking [21], [22] of PML lasers.

In a laser cavity with a saturable gain medium and a saturable absorber, the gain and absorption are saturated by the passing of an optical pulse, such that [23]

$$G(t) = \frac{G_0}{G_0 - (G_0 - 1)\exp\left[-\dfrac{1}{E_{sat}}\displaystyle\int_{-\infty}^{t} P_{in}(\tau)\, d\tau\right]} \quad (1)$$

where $G(t)$ is the instantaneous value of the saturating parameter (gain or absorption), G_o is the initial value of the saturating parameter before the presence of the optical pulse. $E_{\rm sat}$ is the saturation energy of the gain medium or absorber and $\int^t P_{\rm in}(\tau)\, d\tau$ is the fractional pulse energy contained in the leading part of the pulse up to time t. This has the affect of confining the leading edge of the pulse through absorption and the trailing edge of the pulse through gain saturation, resulting in short, high peak-power pulses. It is evident that in order to maintain a steady-state mode-locked pulse stream, the gain medium (SOA) must have a larger saturation energy than the absorber (SA).

This interplay of gain saturation and saturable absorption in the PML laser is the predominant factor in the robust clocking dynamics of the system. The presence of additional optical flux, through pulse injection of a data signal, alters the dynamics of the saturation processes, causing the clock oscillator to synchronize to the injected data stream. It should be noted that the additional optical flux alters the mode-locking process more easily if the gain/absorption is unsaturated. This implies that more injected power is required to achieve synchronization when the injected data signal arrives at the saturating media immediately after the inherent cavity pulse has saturated the media. Less injected power is required when the media has had sufficient time to recover.

When an injected data pulse passes through the SOA before the inherent cavity pulse, it starts to saturate the gain as it is amplified. Then, when the inherent cavity pulse passes through the SOA, the gain saturates sooner, reducing the trailing edge of the inherent pulse more quickly. Likewise, as the injected data pulse passes through the saturable absorber, it starts to bleach the absorber, reducing the absorption of the leading edge of the inherent cavity pulse. The net result of the altered pulse shaping is to shift the inherent clock pulse toward the injected data signal. The experimental results presented in this paper show that only a very small data signal is required to achieve clock synchronization.

IV. Experimental Results

A. Error-Free Clock Recovery

Regenerated clock signals from the injection-locked PML mode-locked laser are illustrated in Fig. 2. Fig. 2(a) shows the synchronized clock signal when the PML laser was fundamentally mode-locked. Harmonic passive mode-locking, and subsequently, harmonic clock recovery, were demonstrated by modifying the gain and absorption saturation energies of the SOA and the SA respectively. The gain saturation energy was changed by

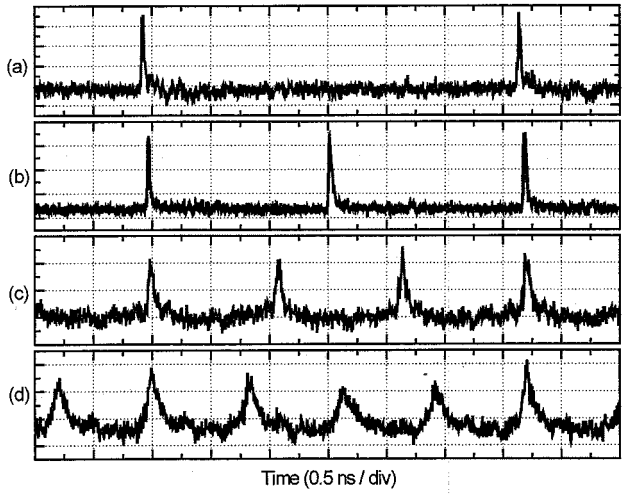


Fig. 2. Regenerated clock signal from a PML laser at the fundamental (a) 311 MHz and at harmonics: (b) 622 MHz, (c) 933 MHz, and (d) 1.244 GHz.

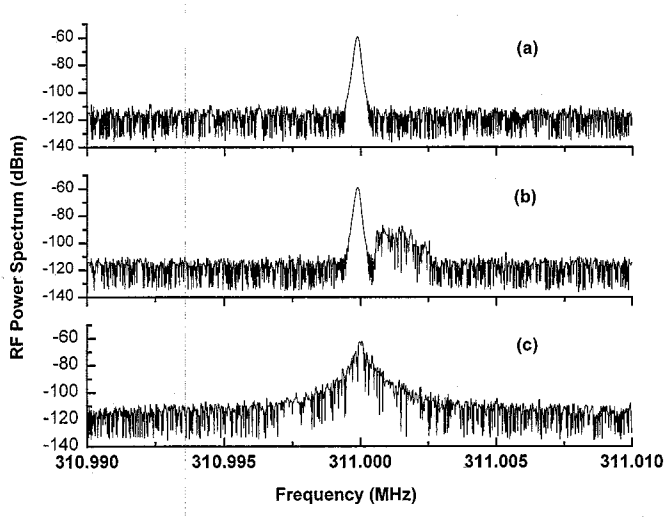


Fig. 3. RF power spectrum of clock signal when injected power is (a) above threshold, (b) at threshold, and (c) below threshold.

adjusting the dc current bias of the SOA, which alters the carrier injection rate and, subsequently, the carrier concentration. The absorption saturation energy was changed by adjusting the location of the focal spot on the SA, due to nonuniformities in the absorber caused by the liftoff process, proton implantation, and the fabricating growth process. Fig. 2(b)–(d) show clock signals at 622 MHz, 933 MHz and 1.244 GHz, respectively, when a 311 MHz *all-1's* data stream was used for clock synchronization. Harmonic clock recovery from the same PML laser, as demonstrated in Fig. 2, shows the potential capability of a reconfigurable clocking rate from a single clock oscillator.

The experimental results show that the clock pulses were degraded with higher harmonic operation as a result of cross gain modulation between the multiple intracavity pulses due to the long recovery time ($\sim$1.1 ns) of the SOA. While the recovery time of the SOA is shown to degrade the harmonically generated clock signal, it should be noted that it does not have as strong of an effect on fundamental clock recovery. In general, it should be noted that the pulse repetition period is determined by the relative recovery times of the gain and saturating mechanisms. To scale the results to higher data rates the relative recovery times must also be scaled. In many situations, the absorption recovery time is faster than the gain, and as a result, the gain recovery time must be reduced to increase the operating rate. This can be achieved by optical pumping methods. Fundamental clock recovery has been demonstrated at 10 Gb/s and higher, typically using monolithic devices [6], [7].

A BER measurement was performed to verify error-free operation of the clock oscillator. To perform a BER measurement for the clock signal, which contains no data (consists of all "1's"), it was necessary to use an additional frequency generator operating at a multiple of the clocking frequency. A 622-MHz signal from a synthesized signal generator, synchronized to the injected data signal, was used as the clock input to the BER instrument. The optical clock signal is received by the high-speed photodetector and connected to the data input of the BER measurement instrument. The BER measurement was performed using a bit-test pattern of [10101010]. With 140 μW of average injected data power, the clock oscillator remained synchronized to the data signal, with no missed clock bits, for over 10 min (error rate $< 5 \times 10^{-12}$). Injecting data with average power as low as 50 μW resulted in at least one minute of error free operation.

In general, short bursts of errors occurred with increasing frequency as the amount of injected power was decreased, as the clock slipped momentarily out of synchronization. This continued until the injected power was reduced below a minimum, at which point the clock completely lost synchronization with the incoming data stream. Fig. 3 illustrates the synchronization characteristics of the clock oscillator in the RF power spectrum of the clock signal as the injected data power was decreased. When the injected data power is high, the RF power spectrum, shown in Fig. 3(a), showed little phase noise, indicating that the clock is completely locked to the incoming data stream. The radio frequency (RF) power spectrum retained this characteristic until the injected data power approached the locking threshold. At threshold, the system slipped in and out of synchronization and the RF power spectrum, as shown in Fig. 3(b), alternated between locked and unlocked noise power as the spectrum analyzer swept through the frequency span. Below the threshold, the RF power spectrum, shown in Fig. 3(c), had additional sideband noise power indicating that it was no longer synchronized, and was free-running in a PML mode. The injection threshold for this system was measured to be 3–6 μW average power (10–20 fJ pulse energy), which is less than 1% of the clock intracavity power.

B. Phase Noise (Timing Jitter) and Amplitude Noise

Phase noise and amplitude noise are important parameters to characterize for clocking systems, since they adversely effect the clocking performance. High timing stability is a fundamental requirement for clocking systems, which implies that the phase noise should be as small as possible. Amplitude noise is especially significant when a clock signal is to be used for data regeneration or optical logic that relies on the clock intensity

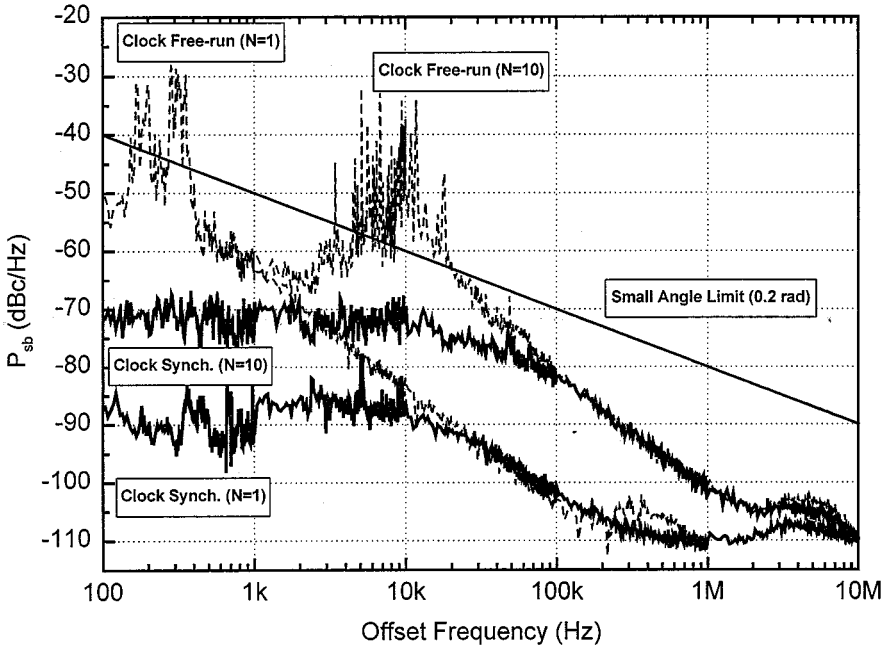


Fig. 4. Noise power spectrum at the fundamental and tenth harmonic of the clock oscillator when synchronized to data (solid) and free-running (dashed), measured from 100 Hz to 10 MHz offset frequencies.

(e.g., nonlinear and interferometric switching systems) where it will be directly mapped onto the processed data signal.

Phase noise arises from a variety of sources, including gain fluctuations, effective cavity length fluctuations, and spontaneous emission fluctuations. Amplitude noise also arises from a variety of sources, including gain fluctuations, spontaneous emission fluctuations, and relaxation oscillations. Additional phase and amplitude noise is also contributed by the SA during PML.

Standard RF power spectrum techniques were used to measure the phase noise and amplitude noise of the clock oscillator [24], [25]. It should be noted that by performing AM & PM noise measurements in the frequency domain, additional information regarding the physical mechanism of these noise sources can be identified, e.g., the rolloff of the noise band, the frequency band of the noise, etc. The mode-locked signal from the clock oscillator, with amplitude and phase noise, can be expressed as

$$I(t) = I_0(t)[1 + A(t)] + \dot{I}_0(t)TJ(t) \tag{2}$$

where $I_0(t)$ is the ideal, noiseless, clock signal, $A(t)$ represents the relative deviation from the average pulse amplitude, and $J(t)$ represents the relative deviation from the average pulse repetition period T. The last term in the equation is the first order term of a Taylor series expansion with respect to time. It is assumed that $A(t)$ and $J(t)$ are ergodic and stationary random processes.

The power spectral density, $S_p(f)$ is given by the Fourier transform of the time-averaged intensity autocorrelation function

$$S_p(F) = \Im\{\langle I(t)I(t+\tau)\rangle. \tag{3}$$

The resulting power spectral density for the clock oscillator is

$$S_{Clock}(f) = \left(\frac{2\pi}{T^2}\right)|\tilde{f}(f)|^2 \sum_{n=-\infty}^{+\infty} \cdot [\delta(f_n) + S_A(f_n) + (2\pi n)^2 S_J(f_n)] \tag{4}$$

where $f_n = (f - n/T)$ and $|\tilde{f}(f)|^2$ is the spectral envelope of the ideal mode-locked pulses. The term n is the harmonic number, and S_A, S_J are the amplitude and phase noise power densities. It can be assumed, for short pulsewidths, that the slowly varying envelope can be removed from the sum, which contains rapidly varying terms. Thus, for a periodic clocking signal, the amplitude and phase noise appear as sideband power on each harmonic of the fundamental clocking rate.

Since the jitter term is derived from a first order approximation for phase noise, (4) is only accurate when phase fluctuations are relatively small compared to the pulse period. The commonly accepted small angle criterion is that the integrated phase deviation over a frequency decade must be less than 0.2 radians [26]. It is also assumed that the pulsewidth remains constant over time.

It is evident, in (4), that the phase noise increases with the square of the harmonic number (n^2), whereas amplitude noise remains constant. Thus, to accurately measure phase noise, measurements should be made on two different harmonics such that the amplitude noise contribution can be subtracted out. Fig. 4 shows the noise power spectra of the clock recovery oscillator on the fundamental and tenth harmonic over a frequency offset range from 100 Hz to 10 MHz. The solid curves show the noise power when the clock was synchronized to the data signal. For frequency offsets between 100 Hz and ~100 kHz, the 20 dB increase in noise power for the tenth harmonic is an indication that phase noise dominates the noise spectrum. For frequencies

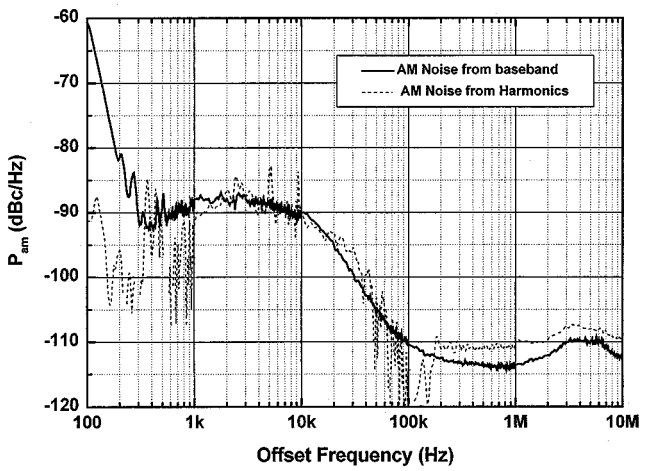


Fig. 5. Amplitude noise power spectrum for the clock oscillator.

above ~100 kHz, where there is less than a 20 dB difference between the noise powers, amplitude noise becomes more prominent. The dashed curves show the noise power when the laser was free-running PML. The differences in the noise spectra between the free-running and synchronized clock signal are most evident in the lower offset frequencies, indicating that injection of a data signal reduced low frequency drifting of the clock oscillator. The 20-dB/decade decay in the phase noise, observed in all the spectra after 10 kHz, is typical for a conventional oscillator [27]. The free-running PML noise power spectra violate the small-angle criterion at low frequency offsets, meaning that the phase noise was too large to accurately measure timing jitter with RF power spectral techniques. In addition, the free-running PML laser also violates the requirement of stationarity, because the fundamental repetition rate experienced small fluctuations over time due to effective cavity length fluctuations.

The fractional pulse-to-pulse root-mean-square (rms) timing jitter is calculated using

$$\frac{\Delta t}{T} = \frac{1}{2\pi}\sqrt{\frac{P_2 - P_1}{P_c(n_2^2 - n_1^2)}} \tag{5}$$

where n_2 and n_1 are the harmonic numbers, P_1 and P_2 are the total integrated powers contained in the noise sidebands at the harmonics, and P_c is the carrier power. Using (5) for the power spectra in Fig. 4, the clock oscillator's fractional timing jitter is measured to be $2 \cdot 10^{-3}$.

The amplitude noise can also be determined from the noise power spectra. Fig. 5 shows the amplitude noise power spectrum. The dashed curve shows the amplitude noise as calculated from the fundamental and tenth harmonic noise spectra in Fig. 4. For comparison, the amplitude noise was also measured at baseband with an HP 11 792C Carrier Noise Test Set (CNTS), and is shown as the solid trace. It can be seen in Fig. 5 that the two measurement techniques provide good agreement. The noise power spectrum measured in the first decade of the baseband measurement is inaccurate due to leakage of the dc component into the resolution bandwidth of the spectrum analyzer.

The relative pulse energy fluctuation is calculated using

$$\frac{\Delta E}{E} = \sqrt{\frac{n_2^2 P_2 - n_1^2 P_1}{P_c(n_2^2 - n_1^2)}}. \tag{6}$$

Using (6) for the power spectra in Fig. 4, the clock oscillator's relative pulse energy fluctuation is measured to be 0.05.

C. Phase Tracking

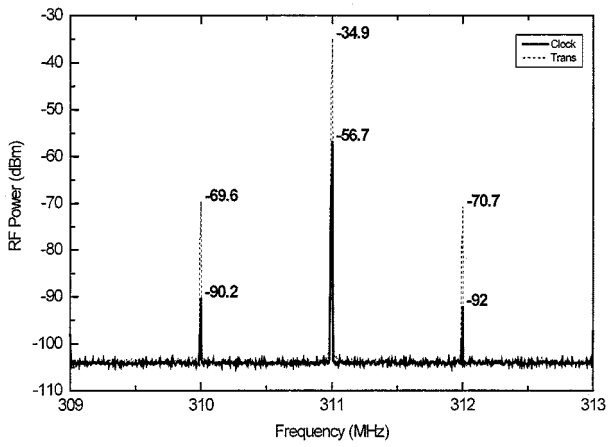
The phase tracking capability of the clock oscillator plays an important role in its suitability for certain clocking applications. For data regeneration or timing references, it is desirable to have a clock with little to no phase tracking, so that phase noise is reduced for the regenerated data signal. For optical signal processing (demultiplexing, switching, etc.) of short optical pulses, it is more suitable to use a clock with phase tracking capability in order to assure proper timing for the optical logical operations.

To demonstrate the phase tracking capability of the clock oscillator, the data signal was phase modulated before injection into the clock oscillator. An external voltage-controlled phase shifter was used to phase modulate the RF signal from the signal synthesizer before biasing the SOA in the transmitter laser. The phase shifter was driven at 10 kHz to 3 MHz with 0.2–2 V amplitude and a 3.5-V DC offset. Fig. 6(a) shows the phase noise sidebands of the clock oscillator and transmitter when the data signal was phase modulated at 1 MHz. The dashed trace shows the RF power spectrum of the transmitter, which was set to about -35 dBc by adjusting the applied modulation voltage on the phase shifter. The solid trace shows the RF power spectrum of the clock oscillator when it was locked to the data signal. The phase noise sidebands on the clock oscillator are also about -35 dBc indicating full phase tracking of the data signal. The clock carrier is weaker than the data carrier because the data signal was optically amplified (see Fig. 1).

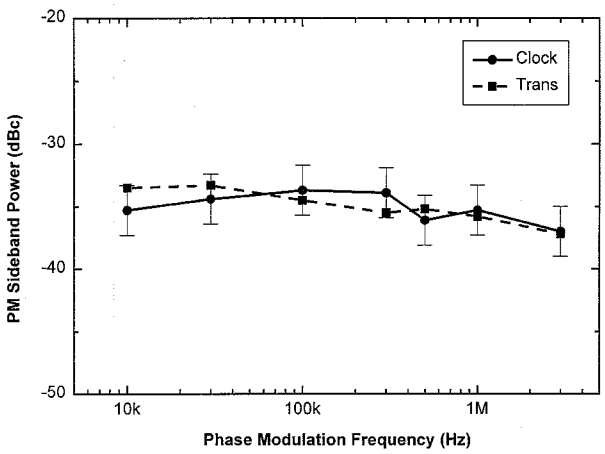
To see the phase tracking bandwidth of the clock oscillator, the PM modulation frequency on the data signal was varied while observing the clock's RF power spectrum. Fig. 6(b) shows the relative modulation power on the clock and transmitter versus the modulation frequency. The measurements showed that the clock oscillator tracks the phase noise of the data signal from low modulation frequencies to high modulation frequencies. The measurements were limited to 3 MHz by the bandwidth of the phase shifter. These results suggest that the PML clock oscillator may be best suited for clock regeneration for optical signal processing applications, where it is desirable for the clock oscillator to track the data signal's phase.

D. Lockup Time

It is important to measure the time required to achieve synchronization of the clock oscillator to an injected data stream since clock lockup time will affect system latency. To measure the lockup time of the clock recovery oscillator, the injected data signal was gated using an SOA modulator or a Mach–Zehnder lithium niobate intensity modulator. The data signal was terminated for a long temporal period to assure the loss of clock synchronization. When the data signal was reestablished, time was required for the clock laser to resynchronize to the data signal.



(a)

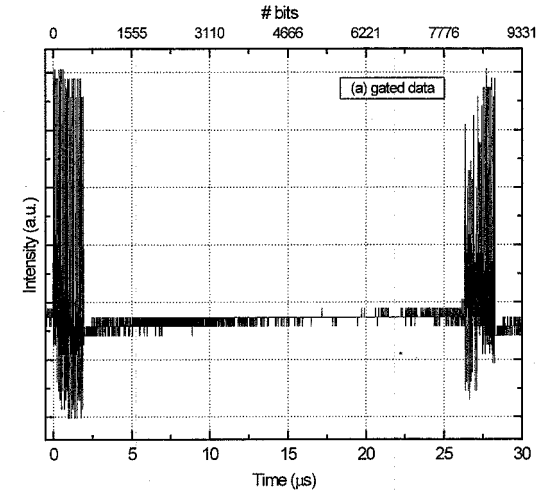


(b)

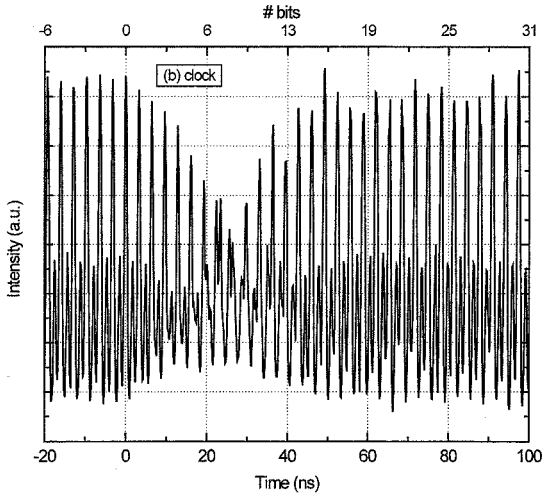
Fig. 6. (a) Phase noise sidebands of the clock oscillator and transmitter when the data signal is phase modulated at 1 MHz. (b) Relative phase modulation sideband power versus modulation frequency.

The clock output trace was detected with the high-speed photodetector, amplified by the low bandwidth (500 MHz) amplifier to reduce aliasing, and measured by the DSO. The DSO was triggered by the same pattern generator that gated the injected data signal. Thus, when the measured signal was averaged on the DSO, only clock pulses that were synchronized to the data signal were observed, and clock lockup time could be measured.

Fig. 7(a) shows the gated data signal over the entire gating period. The data signal was switched on for 608 bits (1.95 μs) and switched off for 7584 bits (24.3 μs). The average injected data power was 7 μW, corresponding to 303 fJ pulses. The resulting averaged clock signal, at the start of data injection, is shown in Fig. 7(b). The dip in pulse amplitude was the result of injecting the data signal. The inherent cavity pulse power decreased as a new synchronized pulse built up from the injected data signal. Analysis of the data in Fig. 7(b) shows that the unsynchronized clock was $\sim$180° out of phase with the data signal at the start of injection. Even with this large phase mismatch, it is shown that the clock synchronizes to the data signal in less than 16 bits (50 ns). This is significantly less than the number of bits required for clock synchronization observed in fiber lasers [28], [29] or self-pulsing diodes [30].



(a)



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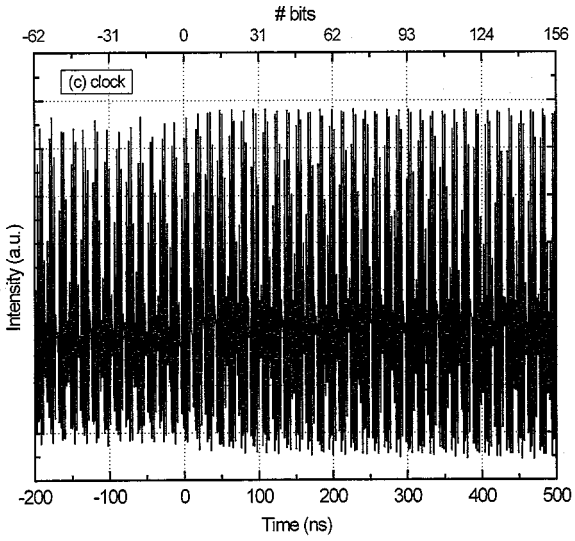

(b)

Fig. 7. (a) Gated data signal and clock signal at the start of data injection, (b) with slight frequency offset, and (c) without.

It was expected that the clock signal before pulse injection would be dephased (unsynchronized) and thus not appear in

the averaged oscilloscope trace. The fact that the pulses were observed in Fig. 7(b), before data injection, suggests that the accumulated clock dephasing arising from timing jitter was quite small. Loss of synchronization was, rather, a result of a slight mismatch between the free-running clocking rate and the data rate, and is deterministic in nature. It should be noted that in this case, the clock and data signal will dephase at the beat frequency. By carefully adjusting the clock's natural repetition rate, it was possible to accurately match the data rate, in which case no dephasing occurred and the clock remained synchronized, even with no data signal present, for all 7584 bits (24.3 μs). This is illustrated in Fig. 7(c). To the best of the authors' knowledge, this is the longest experimentally measured time that an optical clock recovery system remained synchronized to a data signal, when the data signal was no longer present. It should also be noted that the clock signal did not actually dephase in 24.3 μs, but rather, the experimental measurement was limited by the experimental techniques, which required that the high-speed DSO be triggered slowly to be able to average over the entire gated bit pattern. It is likely that the clock dephasing time is even longer than what was demonstrated.

Simulation of injecting a data signal into the clock oscillator was performed to support the experimental measurements. A simple unidirectional ring laser model, shown in Fig. 8(a), was chosen to model the clock oscillator, following [31]. The theoretical models for the gain/absorption saturation and the bandwidth limiter follow [19]–[31]. There are two mechanisms that are responsible for locking to the data signal: a pulling of the clock's phase to match the data signal and/or an overpowering of the unsynchronized clock signal by the injected data signal. Intensity plots [Fig. 8(b), (c)], with reversed contrast for clarity, show the evolution of the clock signal under certain data injection conditions. In Fig. 8(b), the data signal has 1% of the energy of the intracavity clock signal and is injected 100 ps ($\Delta\phi = 0.2$ rad) before the unsynchronized clock. In this figure, the clock signal is slowly pulled toward the data signal and becomes synchronized in about $\sim$1000 round-trips. Increasing the data signal energy to 10% yields the results in Fig. 8(c). The data signal rapidly overpowers the unsynchronized clock in 10–50 round-trips. Thus, to achieve the quickest lockup time the data injection energy should be sufficiently large to ensure rapid lockup. Fig. 8(d) shows the peak intensity in the clock cavity, for the 10% data signal energy case, as the unsynchronized clock pulse decays and the synchronized pulse builds up. The peak intensity dip is the same feature seen in the experimental measurement [see Fig. 7(b)], since the experimental measurement does not resolve the individual synchronized and unsynchronized pulses. Fig. 8(e) shows the pulse evolution for the first 100 round-trips in Fig. 8(c), illustrating the quick build-up of the synchronized clock pulse and the simultaneous decay of the unsynchronized pulse.

E. Frequency Locking Bandwidth

The nominal frequency of the clock oscillator is controlled by its cavity length. This frequency will vary slightly as environmental parameters (temperature, dc bias, etc.) slightly alter the effective cavity length. Deviations in the data signal frequency can also exist, especially if the clocking system is used in an optical network, where data streams may come from a multiple of independent sources. Thus, to ensure proper clock operation, the clocking system should have a large frequency locking bandwidth.

To demonstrate the frequency locking bandwidth of the clock recovery oscillator, the clock's performance was observed while varying the input data signal's carrier frequency. The data rate was varied by adjusting the frequency of the signal generator that provided the RF bias modulation for the actively mode-locked data laser. Fig. 9 shows the maximum upper and lower frequency offsets achieved for a given average injected data power. The inset graph shows the total frequency locking bandwidth of the clock oscillator as a function of injected data power. At the clock recovery threshold power, there was almost no locking bandwidth. The clocking rate must match the data repetition rate exactly in order to achieve clock synchronization. As the injected data power was increased, the locking bandwidth increased until very large powers, where the increase rolled-off. The maximum locking bandwidth observed was 833 kHz, which corresponds to a fractional bandwidth of $2.9 \cdot 10^{-3}$. Larger locking bandwidths may be possible with increased injected data power. It should be noted that these results of locking bandwidth are in good agreement with the locking bandwidth in clock recovery experiments at 10 GHz [8], showing that significant insight to the clock recovery process can be obtained at lower data rates, and extrapolating the results to higher data rates.

Fig. 10 shows the RF power spectrum of the clock oscillator at the limits of the locking bandwidth for large injected data power. The clocking frequency tracked the data signal's frequency as it was detuned, rather than remaining at its base frequency determined by the cavity length. An interesting feature seen in Fig. 10 is that the locking bandwidth is asymmetrical around the free-running clock repetition rate. The data rate can be detuned to much higher repetition rates, but not to much lower ones. This asymmetry is caused by the causality of the gain and absorption saturation mechanisms, as mentioned in Section III. Less injected data energy will be required to dominate the mode-locking process of the clock oscillator if the data enters the clock prior to or overlapping the naturally resonant optical pulse inside the clock oscillator cavity. This occurs when the data signal is at a higher frequency than the nominal clock frequency.

At first, one might suspect that the shift in clock frequency is caused by a change in the index of refraction in the SOA due to data injection. However, the magnitude and sign of the resulting change in index of refraction do not support this conclusion. Injecting the data signal reduces the carrier concentration through gain depletion, which increases the index of refraction and increases the effective cavity length. This implies that injecting a data signal decreases the clock frequency, whereas the experimental results show that the clock frequency is more easily increased. Ignoring the sign and only considering the magnitude of the frequency shift, to achieve the positive frequency shift observed in Fig. 10 (752 kHz), the index of refraction of the SOA would need to change by 2.83, which is physically unrealistic.

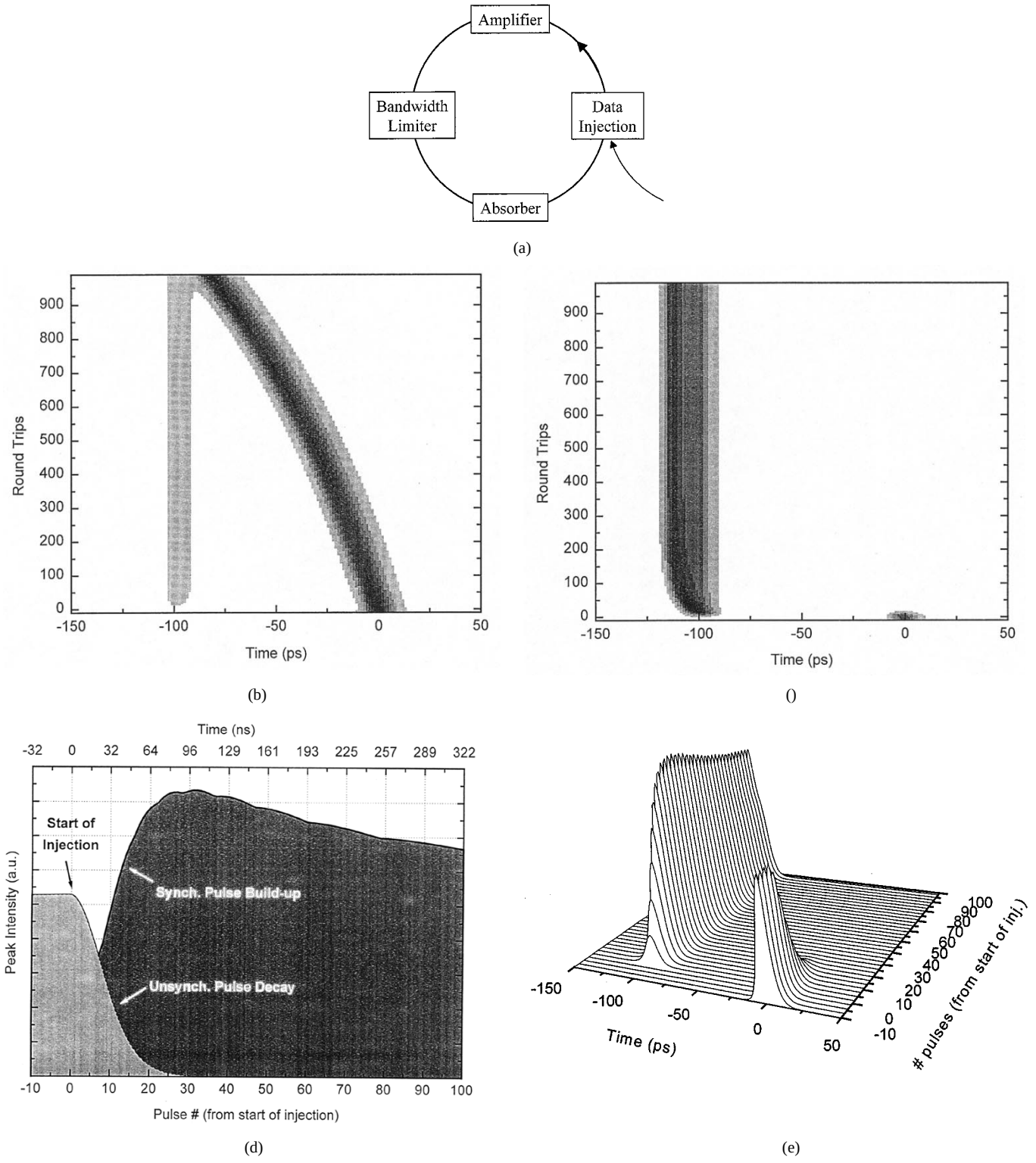

Fig. 8. Clock lockup simulation (a) model and results, showing (b) 1% data signal injection and (c) 10% data signal injection and, for the 10% data signal injection, (d) peak intensity characteristics, and (e) synchronized clock pulse evolution for the first 100 round-trips.

It should be noted that by performing this experiment at a low data rate, we can conclusive determine that the frequency shift is not owing to changes in the refractive index, which would not be clearly evident if the clock were operating at 10 GHz, where small changes in the index could make a significant impact.

In these experiments, there was no observable wavelength shift (spectral resolution 0.4 nm), or pulse broadening effects associated with frequency shifts in the clock rate. However, slight dynamic wavelength shifts and pulse-shaping effects can occur owing to the injection of the optical data signal. However, these

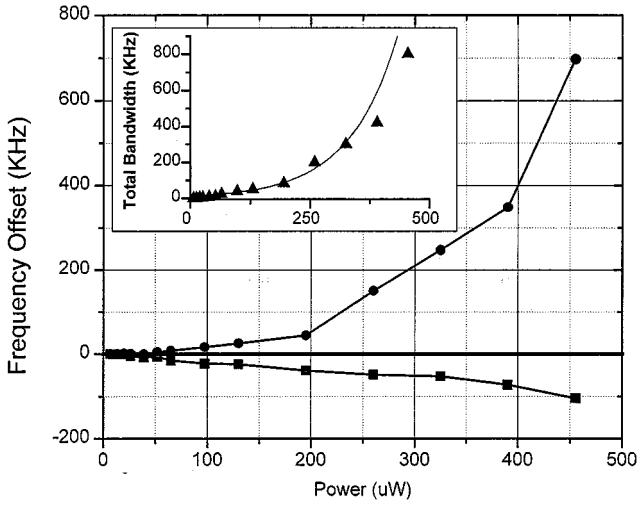

Fig. 9. Repetition rate detuning bandwidth vs. injected power.

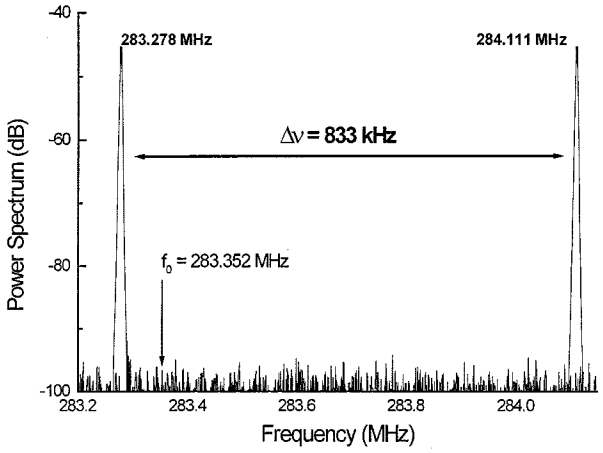

Fig. 10. RF power spectrum of clock signal as injected data rate is detuned.

effects are not directly related to the clock frequency shift observed during frequency locking.

F. Immunity to Bit-Pattern-Effects

The clock oscillator should operate properly independent of the bit pattern that is encoded onto the data signal. To show immunity to bit pattern effects, two bit patterning experiments were performed: one to observe the clocking behavior for a data signal with few "1's" (since "1's" are the data pulses that cause the synchronization effects in the clock) and one to observe the clocking behavior for a data signal with a long series of "0's."

First, a subharmonic data signal was used to show locking to a sparse signal with few "1's." Stable clock regeneration was achieved using a data signal at 1/50th of the clock repetition rate. Fig. 11 shows the output pulse stream from the clocking system, operating at 283 MHz, when a 5.66-MHz data signal was injected. The bold trace indicates the injected data signal. It should be noted that the sinusoidal modulation on the recovered optical clock is due to the alaising incurred by displaying the entire clock stream and two consecutive logical "1's" within the

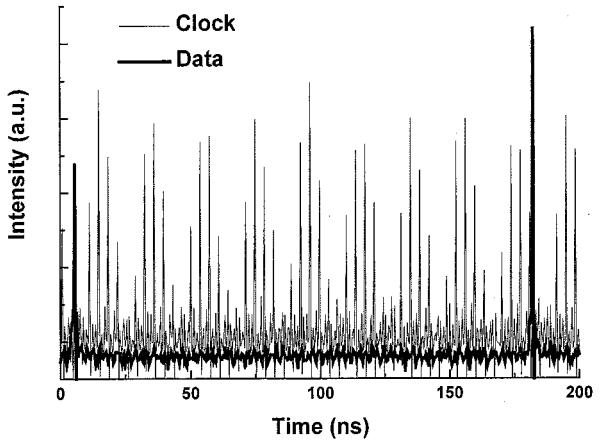

Fig. 11. Clock recovery for subharmonic data input (1/50th).

data packet on the DSO. This modulation is not actually present on the clock signal.

This experiment also demonstrates the capability of sub-harmonic injection locking of a clock oscillator. This becomes especially important when the clock oscillator operates at ultra-fast speeds, where it may be necessary to achieve synchronization or phase stabilization with a slower optical signal. Synchronization of an ultra-fast clock has been demonstrated in this way, through sub-harmonic pulse injection, at up to 40 GHz [32].

The second experiment, previously discussed in Section IV-D, concerns locking the clock oscillator to a data signal that contains a long string of "0's." The data signal consisted of 76 words of data "1's" (608 bits) followed by 948 words of all "0's" (7584 bits). Fig. 7(c) showed the clock signal at the end of the long string of zeros, showing that the clock remained synchronized. This shows that the clock remains synchronized for over 24.3 μs in the absence of a data signal.

The bit pattern immunity is a result of two conditions. First, that the pulse-to-pulse timing jitter, which is the predominant mechanism that limits locking stability, is very small. Second, that the pulse energy required to achieve clock synchronization is small, due to the high gain and low saturation energy of the SOA.

V. Conclusion

These experiments demonstrate the robust clocking dynamics of injection-locked, PML semiconductor laser systems. The experimental characterization of the clock recovery dynamics provides insight into the characteristic parameters that drive clocking performance for many all-optical clock recovery techniques.

Clock synchronization is experimentally demonstrated for fundamentally and harmonically mode-locked PML laser systems. Experimental results show that a data signal with less than 10 fJ pulse energy is necessary to achieve stable, error-free clock recovery, with small amplitude fluctuations $(\Delta E/E = 0.05)$ and timing jitter $(\Delta t/T = 2 \cdot 10^{-3})$. Phase tracking of the data signal was experimentally demonstrated from 10 kHz to 3 MHz. The clock lockup time was shown

to be less than 16 bits (1.95 μs) when injecting a data signal with less than 10% of the clock energy (300 fJ/bit), even when the phase mismatch was $\sim$180°. This is the shortest locking time measured for an all-optical clock recovery system, to our knowledge. The clock remained locked for over 7584 bits (24.3 μs) without a data signal, which is, to our knowledge, the longest holdover time observed. At larger injected powers, the PML laser system is capable of locking to a data signal with a wide frequency locking bandwidth of 833 kHz, or $2.9 \cdot 10^{-3}$ fractional bandwidth. The system also shows stable clocking for nonoptimal data signals with few 1's or many 0's, suggesting that the system is not adversely affected by the data pattern. These clock recovery characteristics show that injection-locked, PML external-cavity semiconductor lasers are well suited for all-optical clock recovery.

ACKNOWLEDGMENT

The authors would like to acknowledge J. C. Connolly and G. A. Alphonse of Sarnoff Corporation for providing the semiconductor optical amplifiers.

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