98-GHz InP/InGaAs HBT Amplifier with 26-dB Gain

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***Abstract*—In this letter the design and characterization of an InP/InGaAs single heterojunction bipolar transistor (HBT) W-Band amplifier is described. The amplifier achieves 26-dB gain at 98 GHz with a bandwidth of 3.1 GHz. On-wafer S-parameter and gain compression measurements are presented. The goal was to explore high gain HBT-amplifiers around 100 GHz. No comparable HBT amplifier at these frequencies could be found in literature.**

***Index Terms*— Heterojunction bipolar transistor (HBT), InP/InGaAs, millimeter-wave amplifier.**

I. INTRODUCTION

THE mm-wave spectrum has become the focus of attention in recent years because the lower frequency bands are filling up quickly. The 95–100-GHz band has been allocated for mobile and mobile-satellite communication, radio navigation, and radio astronomy. New wide-band applications, e.g., wireless LAN, or mm-wave radar require large bandwidths which are readily available at mm-wave frequencies.

In this letter a key component for such applications, a mm-wave amplifier, is presented. The circuit is implemented using InP HBT's (heterojunction bipolar transistors). Similar performance of an HBT-amplifier was reported only at significantly lower frequencies (30 GHz) [1], 50–70 GHz [2].

II. InP/InGaAs HBT PROCESSING

The InP/InGaAs single HBT (SHBT) used for the design has an MOVPE-grown layer structure as described in [2]–[4]. Base and collector thicknesses are 50 and 400 nm, respectively. Wet etching is used to define the mesa isolated transistors. A slight under-etch of the emitter of about 0.1 μm enables self-aligned emitter and base contacts which minimize the external base resistance. Device isolation is achieved by etching down to the semi-insulating InP substrate. Planarization and passivation is performed with polyimide. All devices in the circuit have the same emitter area of 1.0 $\times$ 8 μm^2 achieved with conventional optical lithography. HEMT devices with comparable high-frequency performance would require E-beam lithography for the gate exposure.

On-wafer small signal measurements of the transistors were performed from 45 MHz to 120 GHz. A de-embedding procedure eliminates the effects of the pad frame. The HBT's have a measured dc current gain of 25 and an extrapolated f_T and $f_{\max}$ of 140 GHz and 170 GHz, respectively ($f_{\max}$ was extrapolated from Mason's unilateral gain, all at $V_{CE} = 2$ V, $I_C = 6$ mA).

III. CIRCUIT DESIGN

The design of the amplifier is based on measured S-parameters of the HBT described above. The devices operate at a V_{CE} of 2 V and a collector current density of 7.4$\cdot$10^4 A/cm^2 resulting in $I_C = 5.9$ mA per device. Initial simulation showed that common emitter stages including matching losses (about 2 dB/stage) would not result in sufficient gain at 100 GHz. On the other hand, a single cascode stage shows a maximum available gain (MAG) of 16 dB at 100 GHz compared to 4 dB of a common emitter stage. However, cascode amplifier stages tend to be unstable up to mm-wave frequencies. As a result, stability requires special attention. The four-stage amplifier consists of four cascode stages coupled by coplanar waveguide matching networks. A simplified schematic diagram of a single cascode stage including matching and device stabilization is shown in Fig. 1. The common emitter stage of the cascode is stabilized by a lossy high impedance line (CPW2) at the base and a quarter wave length transmission line terminated with a capacitor at the collector (CPW4, C2). Both lines serve simultaneously as biasing networks. Bias is applied through resistors (R1, R2). These resistors with the capacitors also form a low-pass filter preventing signal feedback via the power supply network. The common base stage is stabilized by a resistor (R4) at the collector. Bias voltage is applied to the base through the resistor R3. CPW5, CPW6 and C3 act as biasing network and also form a matching network between the two transistors to maximize gain [5]. Input and output matching to 50 Ω is achieved by CPW1 and CPW11 with CPW12 respectively.

Small-signal simulations were performed using HP-ADS [6]. All transmission lines are implemented as coplanar waveguides. The capacitors are MIM structures with Tantalpentoxide (Ta_2O_5) as dielectric. These capacitors are modeled by an equivalent circuit with lumped elements and transmission lines. The individual cascode stages are cascaded with coupling capacitors to two, three, and four stage amplifiers. In Fig. 2 a chip photograph of the four-stage amplifier is shown. This chip measures 2.41 $\times$ 0.92 mm^2. The circuit requires two bias voltages $V_C = 6$ V and $V_b = 1.2$ V. V_b could be derived from V_C by a voltage divider to achieve a single supply voltage. The dc power dissipation is 285 mW.

IV. MEASURED RESULTS

The fabricated one-, two-, three-, and four-stage amplifiers were measured on-wafer from 45 MHz to 120 GHz. In

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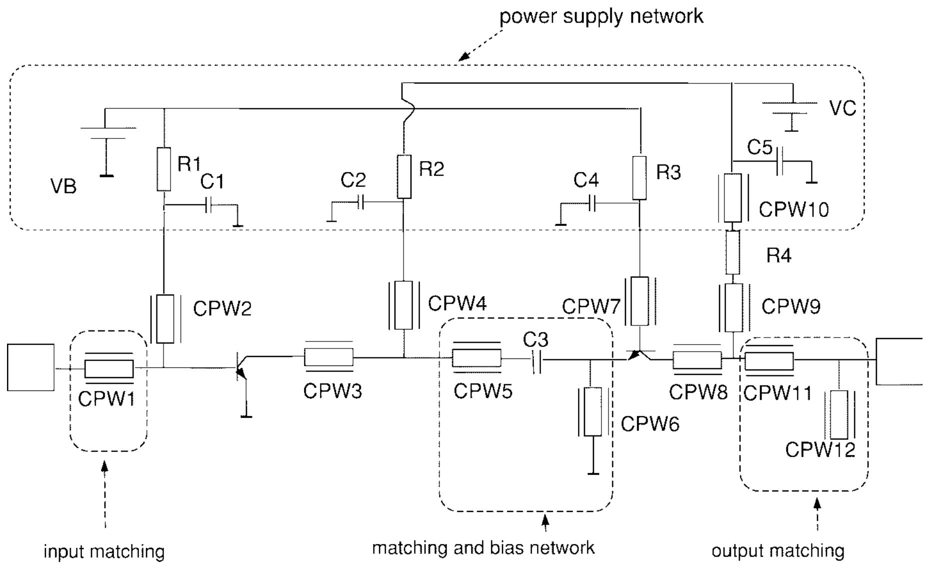

Fig. 1. Simplified schematic of the W-band InP-HBT amplifier implemented with a cascode stage. The four-stage amplifier consists of four capacitively coupled cascode stages.

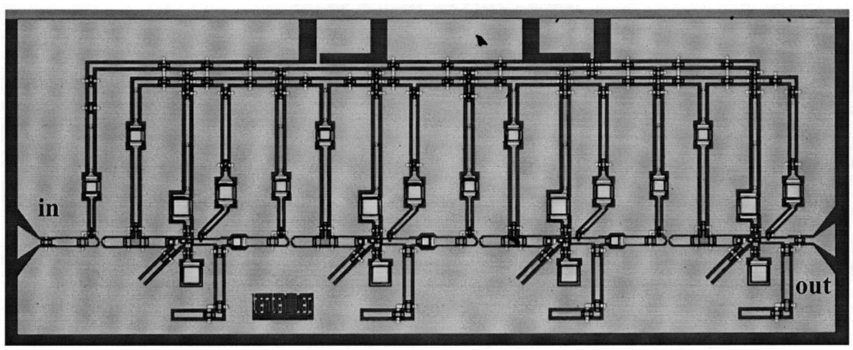

Fig. 2. Photograph of the fabricated four-stage W-band InP-HBT amplifier. Input left, output right. Remaining pads are used for power supplies.

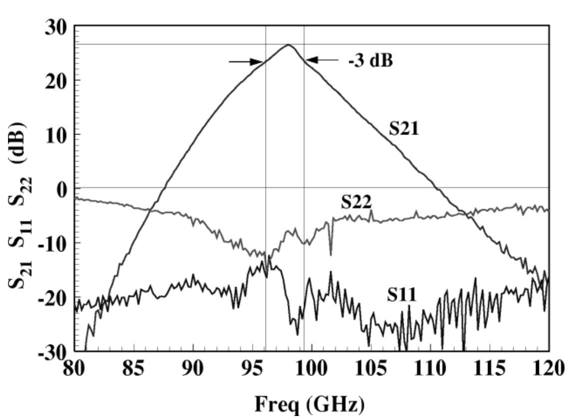

Fig. 3. Measured gain (S21), input reflection coefficient (S11), and output reflection coefficient (S22) of the four-stage W-band HBT amplifier, 26.4 dB gain at 98 GHz, −3 dB Freq. 96.2 GHz, and 99.3 GHz.

Fig. 3 the measured gain (S21) of the four-stage amplifier is presented. A gain of more than 26 dB was achieved with −3-dB frequencies of 96.2 and 99.3 GHz. The amplifier is unconditionally stable for all terminations including short and open circuits. Also shown in Fig. 3 are the input and output reflection coefficients (S11 and S22). In the passband the input reflection is below −12 dB and the output reflection below −6 dB. The one stage to three stage amplifiers show the following measured gain: one stage: 6.2 dB (bandwidth 11 GHz), two stages: 12.2 dB (BW 9 GHz), three stages: 20 dB (BW 5 GHz) all at a center frequency of about 98 GHz.

In Fig. 4 the measured output power versus input power of the four stage amplifier at 98 GHz is presented. The amplifier exhibits a −1-dB gain compression point of −10 dBm which corresponds to an output voltage swing of 200 mV_{PP} at 50 Ω. Saturated output power was measured to be about −4 dBm corresponding to (400 μW) or 400 mVpp into 50 Ω. Noise performance could not be measured due to lack of noise measurement equipment at 98 GHz. Based on previous work at 60 GHz [2] a higher noise figure compared to HEMT's is expected.

V. Conclusion

In this letter the design and characterization of a W-band InP HBT amplifier is presented. The amplifier achieves more than 26 dB gain at 98 GHz. Envisioned applications are in wireless communication or radar. No comparable HBT amplifiers at these frequencies could be found in literature. We

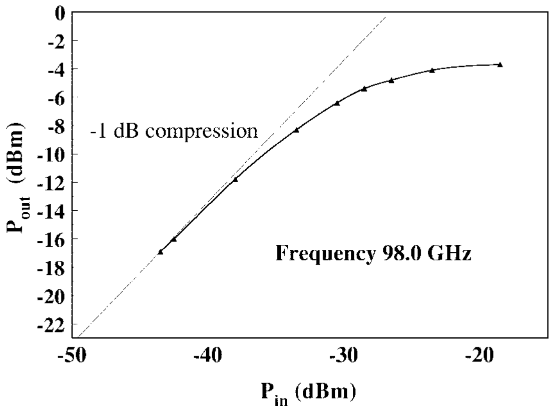

Fig. 4. Output power versus input power of the four-stage amplifier at 98 GHz.

previously reported similar performance of an HBT-amplifier however, at significantly lower frequencies (50–70 GHz) [2].

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