Low-Loss Distributed MEMS Phase Shifter

Andrea Borgioli, Yu Liu, Amit S. Nagra, and Robert A. York

***Abstract*—This letter presents a one-bit low-loss K/K_a-band phase shifter circuit that employs microelectromechanical systems (MEMS) capacitors. The measured results demonstrate a delay line with a 180° phase shift/1.17 dB loss phase shift at 25 GHz, 270° phase shift/1.69 dB loss at 35 GHz, and a return loss better than 11 dB over a 0–35-GHz band. The state-of-the-art insertion loss performance, 154°/dB at 25 GHz and 160°/dB at 35 GHz, demonstrates the potential for the implementation of a very low-loss multibit digital MEMS phase shifter.**

***Index Terms*—Distributed circuit, low-loss, MEMS, micromachining, microwave, millimeter-wave, phase shifters, switches.**

I. Introduction

THERE is a great demand for low-loss low-cost true-time delay phase shifters in modern radar and communications systems. Phased array antennas are indispensable components of such systems, and since a typical phased array employs thousands of independent phase controllers, it is easy to understand why a low-loss low-cost phase shifter technology is crucial in the development of such applications. Microelectromechanical systems (MEMS) concepts have been successfully applied in the past few years to the development of low-loss radio frequency (RF) switching devices and variable capacitors [1]–[10]. Low-loss MEMS switching devices have been used to realize conventional switched-line phase shifter circuits with significantly lower loss than can be realized using conventional technology [1]. Recently, in [11] and [12] a true-time delay phase shifter has been developed using distributed MEMS capacitors by using a single analog control voltage to vary the height of the MEMS bridge, without inducing the snap down, resulting in a limited capacitive ratio $C_{\max}/C_{\min}$ (<1.5).

The circuit design here proposed is based on the idea of a syntethic transmission line [13] whose phase velocity can be varied by snapping down the membrane of MEMS loading capacitors (DOWN state). Since a proper design requires a relatively small value of loading capacitance per unit length [14], [15], the fabrication of physically small MEMS switches can be a challenge, often resulting in the drawback of very high actuation voltages. The topology of the MEMS switches here presented helps to cope with this problem since it does not require a very small capacitive contact of the switch, resulting in a better reliability of the fabrication, a reduced pull-down voltage, and a higher capacitive ratio (~7.5).

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Although the results presented are for 1-bit phase shifter, it is simple to extend the fabrication and design technique to a multibit digital distributed MEMS phase shifter by means of a simple length scaling of the circuit design. The current design is capable of producing 360° phase shift with 2.34–dB loss at 25 GHz and with 2.25-dB loss at 35 GHz, which is state-of-the-art performance for K/K_a band phase shifters.

II. Circuit Design and Fabrication

The phase shifter consists of a CPW transmission line 8.58 mm long, loaded periodically with 11 shunt MEMS capacitors, as shown in Fig. 1(a) and (b). The spacing between the MEMS capacitors is 780 μm. By applying a dc voltage it is possible to actuate the MEMS switches from the UP state (membrane up) to the DOWN state (membrane snapped down), inducing an increase in the value of the loading capacitance: for frequencies below the Bragg frequency (in our design, 40 GHz), the effect is an increase in the total capacitance per unit length of the transmission line structure, and hence a change in the phase velocity and characteristic impedance [12]–[15]. The change in the phase velocity produces a phase shift that is determined by the capacitive ratio $(C_{\rm ON}/C_{\rm OFF})$ of the MEMS elements and by the original (intrinsic) capacitance of the line. A high-impedance line is used to start with $(Z_0 = 69\ \Omega)$, so that the loaded line has a characteristic impedance close to 50 Ω. The designed $Z_{\rm UP}$ and $Z_{\rm DOWN}$ (the characteristic impedances in the UP and DOWN state) are 66.4 and 37.6 Ω, respectively, and they agree fairly well with measure values.

As mentioned above, in order to maintain an acceptable matching over a wide band, it is recommendable not to overload the transmission line with an excessively large MEMS switch capacitance in the DOWN state. To reduce the DOWN state capacitance value of the single MEMS switch, it is possible to increase the thickness of the dielectric layer coating the central conductor or shrink the size of the upper membrane. Unfortunately, both these measures can be exploited only to a certain point, since they result in difficult fabrication or more critical reliability. By adopting a "series" configuration, as illustrated in Fig. 2(a) and (b), it is possible to achieve relatively low value of capacitances (<0.1 pF) in the DOWN state with a larger, more reliable, upper membrane. Also, this design offers other advantages. The quality of the contact of the membrane over the coated central conductor is often an issue since the inevitable irregularities in the profile of the SiN film and of the metal bridge make an accurate control of the value of the final DOWN state capacitances difficult. With a "series" configuration, this problem is reduced since the value of the capacitance in the DOWN state is less sensitive to small aberrations of the contact membrane-dielectric film.

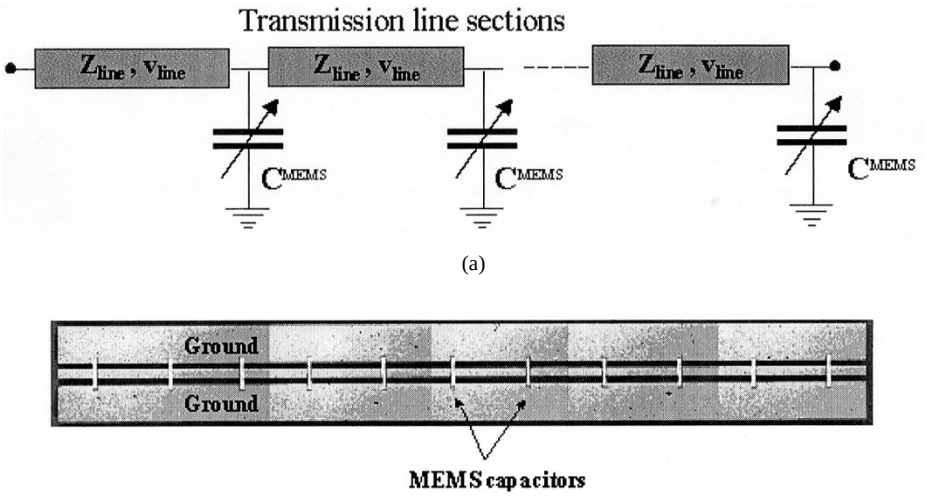


Fig. 1. (a) Circuit schematic of the phase shifter. (b) Actual photograph of the phase shifter circuit fabricated at UCSB. The total length of the phase shifter is 8.58 mm.

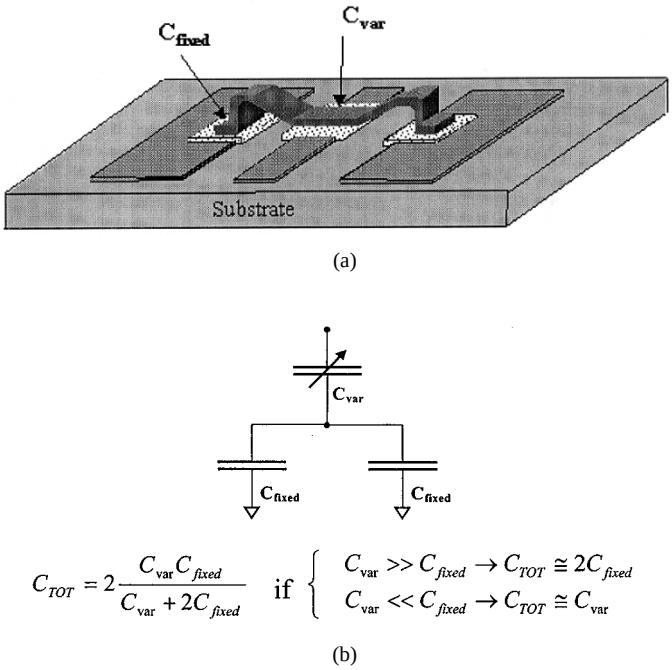


Fig. 2. (a) "Series" configuration topology for the MEMS capacitive switch. (b) Circuit representation for the total capacitance of the MEMS capacitor. In our design C_{fixed} was chosen to be 0.045 pF. The resulting designed total capacitance C_{TOT} is 0.01 pF in the UP state and 0.075 pF in the DOWN state.

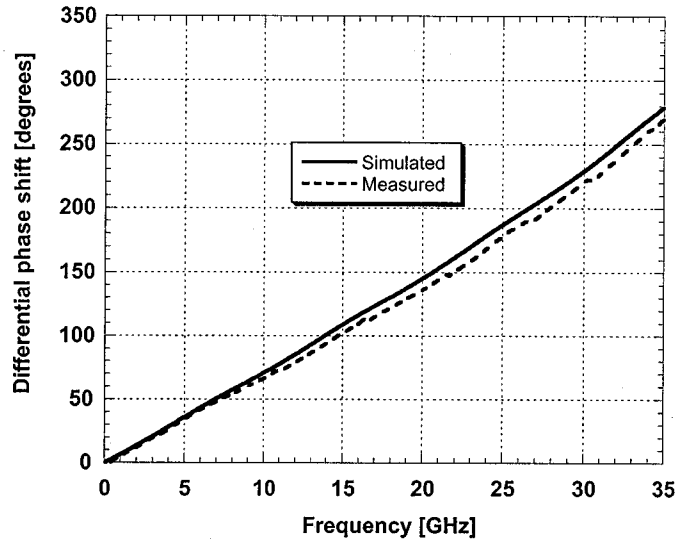


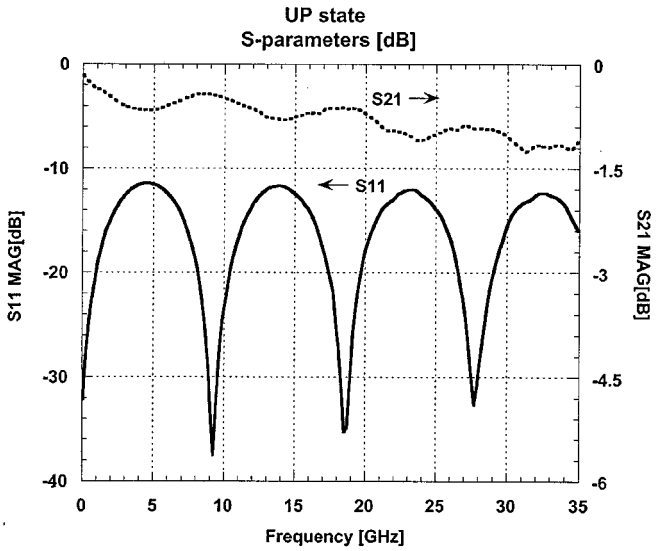
Fig. 3. Simulated and measured differential phase shift versus frequency when the circuit is biased (DOWN state). The phase shift is with respect to the transmitted phase when the circuit is unbiased (UP state).

Also, if the dc bias is applied directly between the membrane and the center conductor with a dedicated control circuitry, the pull-down actuation voltage can be significantly reduced.

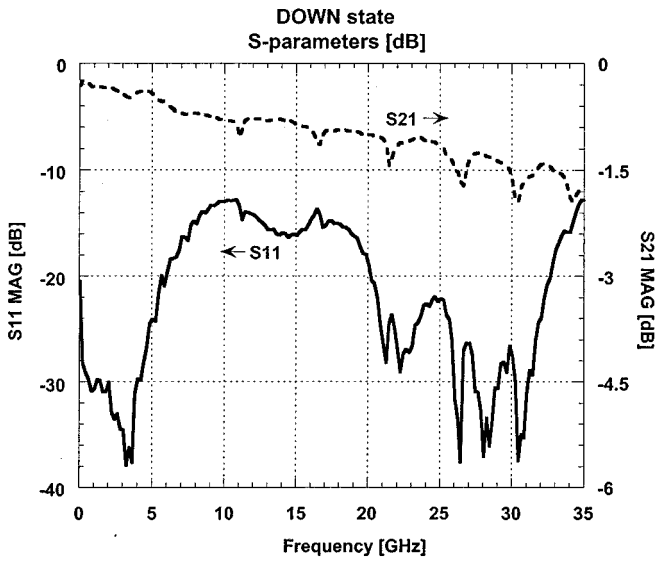
The MEMS one-bit phase shifter is fabricated using CPW transmission lines defined by evaporating 200/7000/200 Å layer of Ti/Au/Ti on a glass substrate ($\varepsilon_r = 5.7$, $\tan(\delta) = 0.001$). The widths of the center conductor and of the gap are chosen to be 100 and 60 μm, respectively. A 5000-Å plasma-enhanced chemical vapor deposition (PECVD) SiN layer is grown and patterned on top. Next, a sacrificial photoresist layer, which determines the height of the MEMS bridge, is patterned. The height of the bridge above the central conductor is chosen to be 3 μm. A 200/10000-Å Ti–Au layer is then evaporated and patterned to define the geometry of the MEMS bridges. The width and the span of the membranes are 40 and 300 μm, respectively. The sacrificial photoresist is then removed and a critical point drying system is used to release the MEMS bridges. The yield of the process and the reliability of the switches vary greatly and depend upon critical parameters such as thickness of the metal membrane, height of the bridge, and residual stress of the metal.

III. Measurement Results

RF measurements were made on a HP 8722D network analyzer, calibrated using on-wafer standards. The two-port s-parameters of the circuit were recorded up to 35 GHz. Fig. 3 illustrates the differential phase shift as a function of frequency. The phase shift is with respect to the transmitted phase at the UP state of the MEMS capacitors. By applying a dc bias (~75 V) a



(a)



(b)

Fig. 4. (a) Measured insertion loss and return loss versus frequency in the UP state. (b) Measured insertion loss and return loss versus frequency in the DOWN state.

change in the phase velocity and hence a phase shift is induced. As expected, the circuit is capable of producing a phase shift that varies linearly with frequency. The phase shift at 25 GHz is 180° and at 35 GHz is 270°. Fig. 4(a) and (b) shows the insertion loss and the return loss for the UP state and the DOWN state. The UP state insertion loss is 0.98 dB at 25 GHz and 1.07 dB at 35 GHz. The DOWN state insertion loss is only 1.17 dB at 25 GHz and 1.69 dB at 35 GHz. It is worth noticing that the ripple in the insertion loss in the DOWN state can be explained by the inevitable nonuniformities of the DOWN capacitance values. This generates a small mismatch among the sections of the line and therefore it sets up standing waves. The return loss is better than 11 dB for both the DOWN and UP state of the MEMS capacitors, over the entire frequency range of 0–35 GHz. These are the best performances for a K/K_a-band phase shifter reported to date.

IV. Conclusion

In summary, we have designed, fabricated, and tested a distributed one-bit phase shifter based on MEMS capacitors. The phase shifter demonstrated a phase shift of 180° with an insertion loss of 1.17 dB at 25 GHz, a phase shift of 270° with an insertion loss of 1.69 dB at 35 GHz, and a return loss better than 11 dB over a 0–35-GHz band. To the best of our knowledge, this is the lowest reported insertion loss for a phase shifter at K/K_a band reported to date.

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