Impact of Test-Fixture Forward Coupling on On-Wafer Silicon Device Measurements

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***Abstract*—Often, the test-fixture forward coupling is ignored during on-wafer device measurements, although existing de-embedding techniques provide means for addressing its effect. In this letter it is demonstrated that large errors may occur if forward coupling is not determined and accounted for. An investigation based on basic scaling properties of MOSFET's is proposed as a benchmark test to partially verify de-embedding methods.**

***Index Terms*—Calibration, integrated circuits, microwave measurements.**

I. Introduction

ACCURATE on-wafer measuring techniques are required to characterize integrated devices so that full microwave performance of current silicon technologies can be unleashed. Standard practice is to combine high-accuracy *impedance standard substrate* (ISS) calibration with a de-embedding method for separately addressing losses associated with the silicon substrate and low-performance interconnects [1]. In the literature, the test-fixture forward coupling has become a disputed subject and its effects are often left unaccounted [2], [3]. In this letter, basic properties of scaled MOSFET's are employed to demonstrate that test-fixture forward coupling should indeed be considered for accurate results and that large errors can occur if proper actions are not taken.

II. Test-Fixture Forward Coupling

Forward coupling of an on-wafer test-fixture is caused by several mechanisms including: 1) direct coupling due to proximity of probes; 2) direct fringing between fixture input and output leads; and 3) substrate carried coupling. The two former effects are typically small enough in practice to be ignored for many measurements; say below -50 dB at 12 GHz [4]. However, for standard silicon technologies (Bipolar/CMOS), the substrate-carried coupling is more noticeable due to limited substrate resistivity. Existing de-embedding methods [5], [1] provide the possibility for estimating and correcting forward coupling errors by use of an in-fixture open standard, but this feature is often not used in practice [3], [2]. The reason given in [2] is that the open fixture is not representative for the forward coupling of the actual measuring fixture since the presence of the *device under test* (DUT) leads to a changed doping and electrode profile. Further, it is assumed that intrinsic terminal coupling of the device dominates test-fixture forward coupling. By using BSIM3v3 as a reference it is found that inclusion of the forward coupling leads to an f_T overestimation as large as 50% [2]. However, the fixture used in [2] displays only about 5 fF of input capacitance which is 10–50 times lower than what is typically experienced with silicon technology when high measuring repeatability is facilitated [4]. Hence, a higher degree of substrate-carried coupling usually exists in practice. Admittedly, the placement of the device is usually accompanied by substrate contacts which give a better grounded substrate when the device is present. However, this effect is limited in practice since: 1) the test-fixture is typically many times larger than the actual DUT and 2) the dominating part of the substrate coupling takes place through lower substrate layers which are relatively unaffected by substrate taps placed at the surface [4]. To avoid the numerous concerns and inaccuracies reported with compact models, the above issues are demonstrated in this letter by utilizing basic scaling properties of MOSFET's.

III. Test for Forward-Coupling Compensation

The basis for the test is that MOSFET's display certain characteristics which scale with geometry. For submicron minimum-length devices and operating frequencies in the low-gigahertz range, the quasi-static assumption is largely fulfilled and bulk resistive effects may be ignored. Given these conditions [4]

$$y_{12} = \left.\frac{I_g}{V_d}\right|_{V_g=0} = \frac{-j\omega C_{\mathrm{gd}}}{1+j\omega(C_{\mathrm{gs}}+C_{\mathrm{gb}}+C_{\mathrm{gd}})R_g} \quad [S]. \quad (1)$$

At sufficiently low frequencies, $\omega(C_{\mathrm{gs}}+C_{\mathrm{gb}}+C_{\mathrm{gd}})R_g \ll 1$ so that $\Im\{y_{12}\} \simeq -\omega C_{\mathrm{gd}}$. The input admittance y_{11} can also be considered for this test but is more sensitive to any distortion caused by varying fixture-device interconnects [4]. For a physical transistor C_{gd} is proportional to the total transistor width W, provided that channel length is kept constant and all fingers are identical (so that the ratio of edge effects to distributed effects is kept constant). This is accommodated by cascading a unit transistor as seen in Fig. 1(a) to form larger devices. Hence, measured responses of $\Im\{y_{12}\}$ must be proportional to W provided that test-fixture forward coupling does not offset the results. This basic property provides a convenient benchmark test.

To ensure a high level of consistency between varying-width device measurements, the interconnects to each transistor must be nearly identical and coupling to substrate and other parts of the transistor minimized. By using relatively large devices, say $W > 50$ μm, the test proves to be quite resistant toward small fixture effects caused by the mounting of differently-sized devices. Multifingered layouts should be applied to give low gate resistance so that above specified conditions can be fulfilled.

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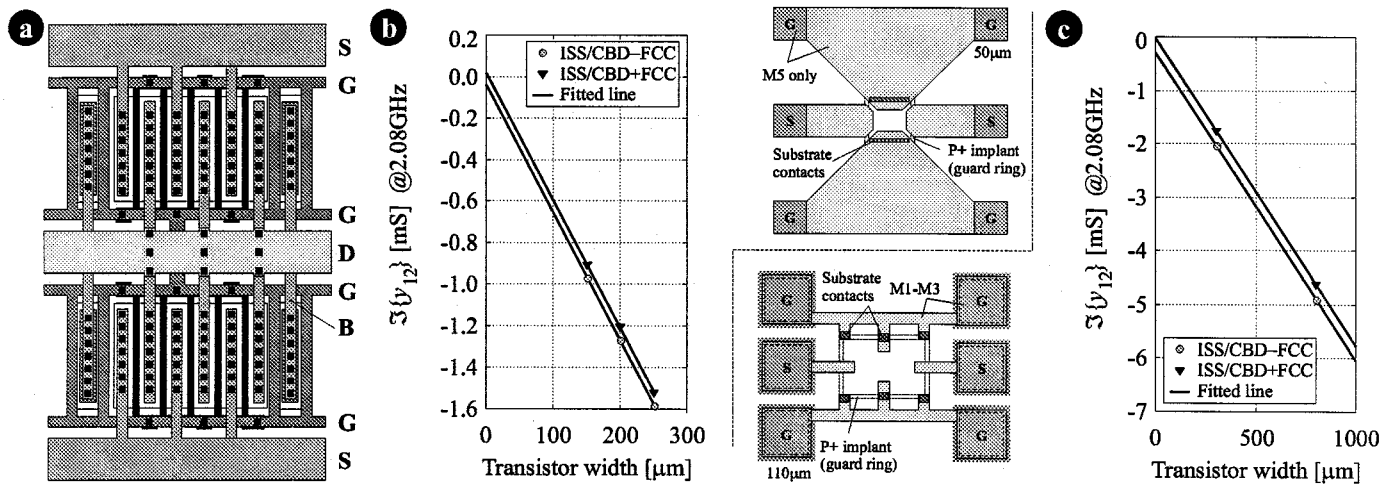

Fig. 1. Illustration of (a) layout of 10-finger μm $\times$ 0.25 μm unit NMOSFET and (b), (c) test-fixtures and results for CMOS25/CMOS50 scaling tests.

Bulk contacts should be placed consistently for every 4–5 fingers. As to reduce the number of effects active at a time it suffices to zero-bias the test transistors. A proper range of test frequencies can be found by sweeping device Y-parameters. The frequency should be high enough that very high impedance characteristics of the MOSFET do not give large measuring inaccuracies. A proper frequency range appears to be 1–3 GHz [4].

IV. Experiments

A 0.25-μm bulk CMOS technology (CMOS25) and a 0.5-μm epitaxial CMOS technology (CMOS50) have been used to fabricate sets of scaled MOSFET's and in-fixture standards. In CMOS25, the set consists of three MOSFET's of dimensions 150 μm $\times$ 0.25 μm (30 fingers), 200 μm $\times$ 0.25μm (40 fingers), and 250 μm $\times$ 0.25 μm (50 fingers). All transistors are mounted in the test-fixture depicted in Fig. 1(b). Although designed for low substrate coupling (small pads in top metal layer only), the fixture displays more than 40 fF of input capacitance. The test frequency is set to 2.08 GHz. Two approaches have been used to de-embed the measurements. One is to combine an ISS LRM calibration with a reduced *Cho/Burk de-embedding* (CBD) method [5], [1] where forward coupling is not considered (denoted "ISS/CBD−FCC"). The other applied method is similar but employs the full-scale CBD method (denoted "ISS/CBD+FCC"). Measuring results are plotted in Fig. 1(b) along with best-fit lines in a least-squares sense. Note that with forward coupling compensation, the extrapolated line of $\Im\{y_{12}\}$ intersects the axis of ordinates close to 0 mS as desired. Without forward coupling compensation, an error corresponding to 0.04-mS or 3-fF results. Similar curves have been drawn for several other frequencies below 3 GHz. In every case, the inclusion of the forward coupling leads to a significant improvement which indicates that tolerance effects are not significant.

In the above experiment, the bulk-type substrate and the specific test-fixture design give a moderate forward coupling. The second experiment uses the CMOS50 process and a test-fixture with pads compliant with given layout rules. For epitaxial processes, the heavily $p+$ doped substrate layer provides a low-impedance path from probe to probe which generally leads to a large degree of test-fixture forward coupling [4]. One 300 μm $\times$ 0.5 μm and one 800 μm $\times$ 0.5 μm NMOSFET have been fabricated and mounted in the test-fixture shown in Fig. 1(d). Again, a large improvement in the response of $\Im\{y_{12}\}$ is achieved when using forward coupling compensation. The error resulting from ISS/CBD−FCC corresponds to 23 fF which may even dominate the gate-drain capacitance of many RF transistors. Again, results are consistent for all tested frequencies.

V. Conclusion

From considerations of silicon substrate properties it has been argued that: 1) forward coupling compensation must be used for accurate results and 2) an open test-fixture may be used to obtain a fair estimate of the effects. A more accurate estimate of the forward coupling can be achieved by placing an unconnected device in the fixture gap (with substrate contacts connected) and use this structure as the in-fixture open standard. These intuitively based arguments have been convincingly supported by two different CMOS measuring situations where basic MOSFET properties are exploited. The proposed test can be used to partly verify de-embedding methods.

References

[1] T. E. Kolding, "On-wafer calibration techniques for giga-hertz CMOS measurements," in *Proc. IEEE Int. Conf. Microelectronic Test Structures (ICMTS)*, Gothenburg, Sweden, Mar. 1999, pp. 105–110.

[2] C.-H. Kim, C. S. Kim, H. K. Yu, and K. S. Nam, "An isolated-open pattern to de-embed pad parasitics," *IEEE Microwave Guided Wave Lett.*, vol. 8, pp. 96–98, Feb. 1998.

[3] C. E. Biber, M. L. Schmatz, T. Morf, U. Lott, and W. Bächtold, "A nonlinear microwave MOSFET model for spice simulators," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 604–610, May 1998.

[4] T. E. Kolding, "On-Wafer Measuring Techniques for Characterizing RF CMOS Devices," Ph.D. Thesis, RF Integrated Systems & Circuits (RISC) Group, Aalborg University, 9220 Aalborg Øst, Denmark, Aug. 1999.

[5] H. Cho and D. E. Burk, "Three-step method for the de-embedding of high-frequency S-parameter measurements," *IEEE Trans. Electron Devices*, vol. 38, pp. 1371–1375, June 1991.