Fully Integrated 94-GHz Subharmonic Injection-Locked PLL Circuit

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***Abstract*—A new integrated *W*-band frequency source MMIC is presented which consists of a 94-GHz voltage-controlled oscillator (VCO) with large tuning range and a phase comparator, forming a subharmonic injection-locked phase-locked loop (ILPLL). The ILPLL combines conventional injection-locking with an additional phase control loop to improve the locking range of the oscillator significantly. The 4th subharmonic frequency is used as the reference signal. The locking range was increased from 80 MHz without ILPLL to 4.5 GHz with ILPLL by closing the loop with an external dc amplifier. A phase noise of −83 dBc/Hz at 100-KHz offset was achieved. Pseudomorphic GaAs HEMT's and a coplanar circuit topology were used to allow integration into complex single-chip subsystems and flip-chip packaging.**

***Index Terms*—Injection-locked phase-locked loop, mixer, phase detector, PLL, subharmonic injection-locked oscillator, voltage-controlled oscillator.**

I. Introduction

MILLIMETER-WAVE systems for automotive control and radar applications raise the demand for low-cost signal sources with high spectral purity. Solid-state oscillators based on high-electron mobility transistors (HEMT's) using coplanar technology [1] ease the fabrication of millimeter-wave modules. They offer the possibility to develop one-chip solutions for complete subsystems [2] and allow the application of state-of-the-art assembly techniques, like flip-chip mounting [3]. The poor phase noise performance of HEMT oscillators, when compared to cavity stabilized Gunn oscillators, necessitates the development of advanced stabilization techniques like synchronization to a high-quality reference at a subharmonic frequency. Injection-locking or conventional phase-locked-loop (PLL) techniques are commonly applied. Injection-locking has been demonstrated up to *V*- and *W*-band frequencies [4], whereas the integrated PLL approach is limited to lower frequencies [5]. The major disadvantages of conventional injection-locked oscillators (ILO's) are the lack of feedback control of the synchronized output signal and the small locking ranges, especially when using higher order subharmonics as the reference signal [6]. Thus, frequency drifts of the oscillator due to temperature effects can result in breaking up the synchronization, when small locking ranges exist.

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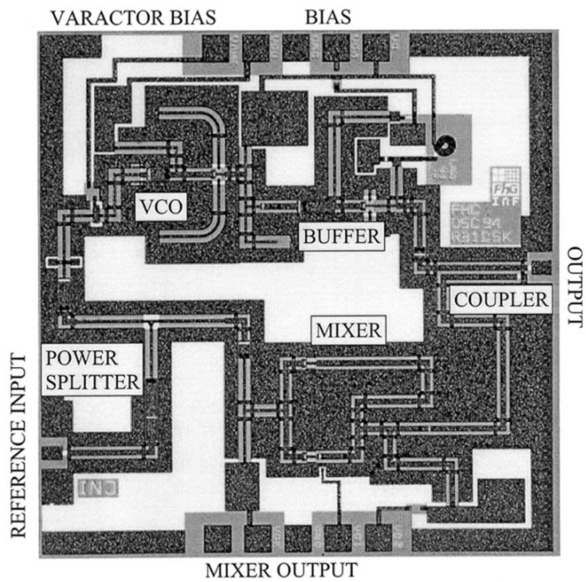

Fig. 1. Chip photograph of the 94-GHz injection-locked PLL MMIC. The chip size is 2×2 mm^2.

II. Principle of Operation

The 94-GHz source module with extended subharmonic injection-locking presented here is based on the injection-locked phase-locked loop principle (ILPLL) [7]–[9]. Within the locking range, a phase difference from $-\pi/2$ to $+\pi/2$ exists between the reference signal and the locked output signal, as described in [10]–[12]. A zero-degree phase shift specifies the center of the locking range. This phase relation is used to control the oscillator output frequency to lie at the center of the locking range, counteracting any frequency drift. The phase noise of the synchronized signal is primarily determined by the injection-locking process. Thus, only a simple PLL is necessary to control the oscillator frequency, but a fast controller can even further improve the phase noise performance [7]. Applying this technique, the locking range depends mainly on the tuning characteristics, and not on the locking behavior of the oscillator. Compared to conventional injection-locking, we achieved an increase of the locking range by a factor of more than 50 using the 4th subharmonic as the reference.

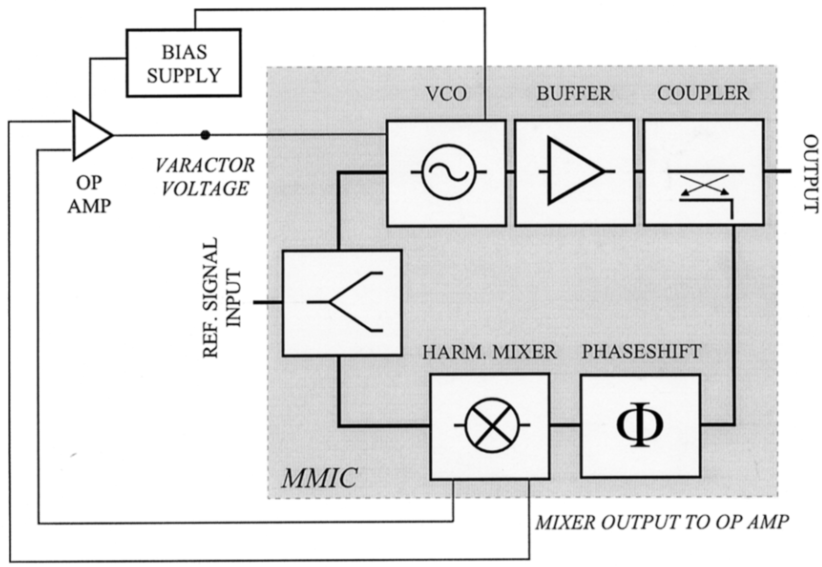

Fig. 2. Block diagram of the ILPLL circuit.

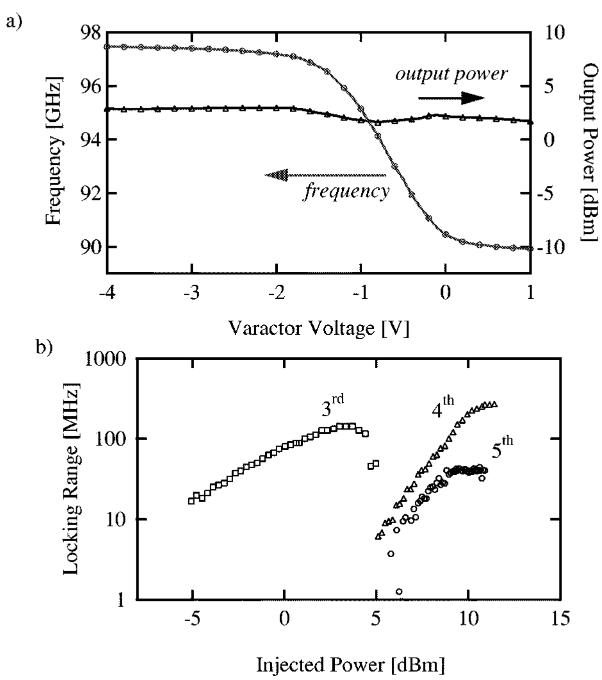

Fig. 3. Measured performance of the integrated oscillator: (a) Tuning range. (b) Locking range.

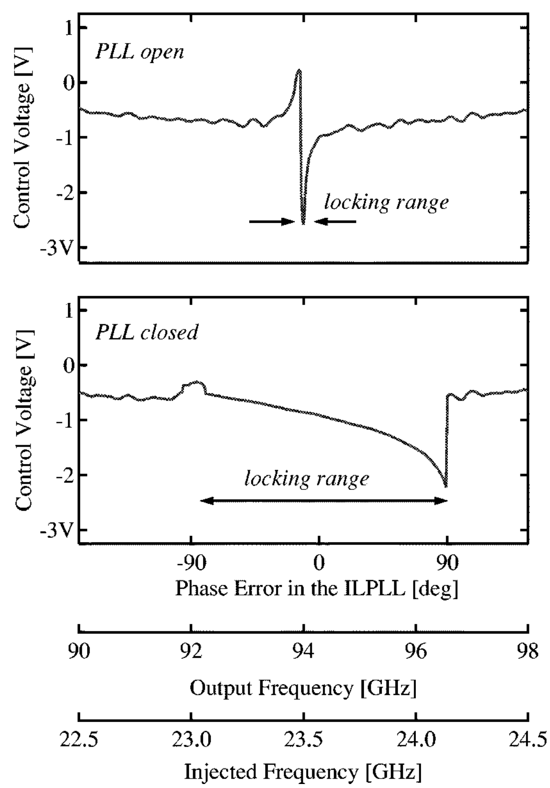

Fig. 4. Differential dc output voltage of the mixer, indicating the locking range with and without the PLL loop.

III. Circuit Description and Measurement Results

A block diagram and a chip photograph of the presented MMIC are shown in Figs. 1 and 2. The circuit consists of a voltage-controlled oscillator (VCO) including an injection port for the 3rd to 5th subharmonic frequency, as described in [1] and [4], and a harmonic resistive mixer used as a phase comparator. As shown in Fig. 2, the reference signal is divided to the injection port of the oscillator and to the phase comparator, realized by a harmonic mixer. Part of the oscillator output signal is fed back by a 10-dB coupler and a transmission line, whose length is optimized to adjust the phase shift to be zero degrees at the center of the locking range. The dc output of the mixer, which is directly related to the phase difference between the two signals, is amplified externally and added to the tuning voltage of the oscillator.

The oscillator achieves a tuning range of more than 7.5 GHz, centered at 94 GHz, as shown in Fig. 3(a). We measured the locking range of the oscillator by sweeping the injected signal frequency at the 3rd, 4th, and the 5th subharmonic. Fig. 3(b) shows a maxmimum locking range of 300 MHz, when using the 4th subharmonic.

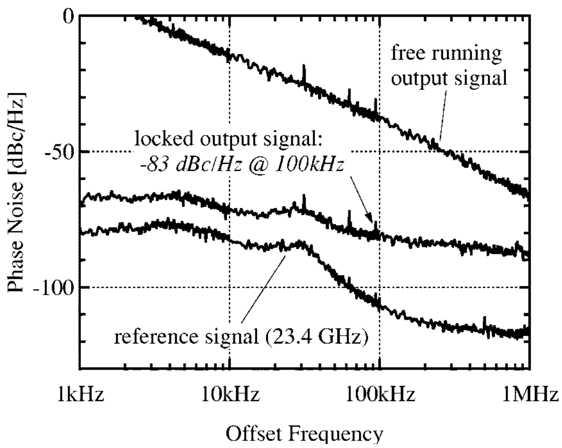

Fig. 5. Phase noise measurements of the 94-GHz ILPLL chip.

For the phase comparator, a mixer was developed for operation at subharmonics of the same order as used for locking the oscillator. A balanced design was chosen to generate a differential dc output signal, compensating unwanted dc components. The locking range of the oscillator can be observed directly on the dc output signals. The difference of the two signals is then used to control the oscillator.

The 4th subharmonic with 8-dBm injection power was used for measuring the performance of the ILPLL. Fig. 4 shows the effect of the phase control. The diagram shows the control voltage for the oscillator with the PLL closed versus the phase difference in the ILPLL, which is equivalent to the axis for input and output frequency, respectively. The locking range of 80 MHz obtained without the PLL was increased to the value of 4.5 GHz by closing the loop. Fig. 5 illustrates the phase noise measurement results of the locked oscillator, compared to the phase noise of the reference source and the free-running oscillator. We measured a phase noise of −83 dBc/Hz at the 100-KHz offset frequency for an injected power level of 6 dBm at 23.4 GHz. According to theory, the frequency multiplication increases the phase noise as $P_{\text{noise out}} = N^2 P_{\text{noise in}}$, where N is the subharmonic factor, predicting 12-dB degradation of the phase noise for $N = 4$. This noise degradation is a function of the frequency offset and injected power. This dependence is more pronounced in the case of subharmonic injection. Thus, for higher offset frequencies, the noise reduction can be improved by higher injected power levels, as shown in [4]. A further improvement of the phase noise performance can be obtained using a reference signal with lower phase noise [13] or by a faster dc controller.

IV. Conclusion

We developed a new single-chip 94-GHz source module with an integrated injection-locked phase-locked loop (ILPLL) using the 4th subharmonic. The locking range could be improved from 80 MHz without the ILPLL to 4.5 GHz by applying this technique. A phase noise of −83 dBc/Hz at 100-KHz offset was achieved.

The result demonstrates the great potential of the ILPLL for solid-state millimeter-wave sources. An additional improvement of the phase noise is possible by using a faster dc controller.

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