A Synthesis-Oriented Approach to Design Microwave Multidevice Amplifiers with a Prefixed Stability Margin

Francesco Centurelli, *Member, IEEE*, Giuseppe Scotti, Pasquale Tommasino, and Alessandro Trifiletti

***Abstract*—A design methodology that allows forcing a prefixed stability margin on microwave and millimeter-wave multidevice amplifiers during the synthesis procedure performed by CAD tools is proposed. To the best of our knowledge, for the first time expressions equivalent to stability margins have been determined to guide CAD optimizers to design circuits stable under parameter variations. Stability margins discussed in this paper allow inclusion of stability requirements among yield specifications in a rigorous way. A case study of a 4-FET distributed amplifier design is presented where stability under parameter variations has been achieved by using the proposed methodology.**

***Index Terms*—CAD tools optimizer, MMIC, stability, yield.**

I. Introduction

IN TODAY'S competitive microwave circuit market it is important to achieve more and more rigorous performance requirements. Circuit responses have to meet specifications in spite of the unavoidable variations in circuit parameters caused by nonidealities of fabrication process, if a robust product design is desired. Typically [1], the designer has to choose a set of design factors (i.e., transmission line lengths, capacitance values, damping resistor values) in order both to meet specifications and to reduce the effect of the so called noise factors (i.e., parameter variations, input and output load variations, temperature, aging) on circuit responses. It is possible to quantify circuit response variability and to estimate circuit yield by means of statistical analyses such as Monte Carlo simulation. Yield specifications which define acceptability region are usually fixed taking into account circuit responses such as gain, noise figure, and voltage standing wave ratios [1], whereas little importance is often given to stability requirements in estimating circuit yield. Circuit stability is one of the troublesome aspects for the designer and it has to be assured in spite of parameter variations: therefore, a design methodology which guarantees stability under parameter variations is required. Microwave designers usually rely on stability factors such as Rollet Factor K [2] or other equivalent ones in ascertaining the stability of their designs; however, this approach fails in many cases, as it has been pointed out by several authors [2]–[6], since it is valid only under the proviso [3] that immittance or S parameters of the two port have no RHP poles. Moreover, the stability check is performed after circuit optimization, leading to a time-consuming trial and error design methodology, and anyway it checks stability only for nominal device parameters and termination values. In a previous work [5], we presented a design methodology, which allowed to perform circuit synthesis by CAD tools including stability among optimizer goals. In the same work, we stated a criterion to guarantee conditional stability in given circular regions of the input and output termination planes Γ_S and Γ_L, by means of stability factors depending on the maximum modula ρ_S and ρ_L allowed for input and output reflection coefficients. This procedure leads to a product design robust with respect to input and output load variations, but does not consider circuit parameters dispersion which could drive a stable circuit to instability. Control engineers usually make their design stable with a certain gain or phase stability margin to take parameter variations into account. A similar approach can be used to guarantee microwave multidevice circuits stability. In this work, we propose a yield oriented design methodology which allows the synthesis of microwave circuits stable under both process parameters dispersion and input and output load variations. The proposed methodology makes use of novel stability conditions, which are able to guarantee stability of multidevice amplifiers with a prefixed gain or phase margin and are suitable to be used by CAD tools optimizers during the synthesis of passive matching networks.

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The authors are with the Dipartimento di Ingegneria Elettronica, Università di Roma "La Sapienza," 00184 Roma, Italy (e-mail: trifiletti@die.ing.uniroma1.it).

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II. Stability Conditions

A rigorous way, based on Nyquist criterion, to check the stability of multidevice microwave circuits was proposed in [4]. To allow circuit analysis from the viewpoint of Nyquist criterion, the circuit is partitioned into an active $2N$-port network S, comprising all the N active devices, and a passive $2N$-port network S'. The overall circuit is considered as a multiloop system and is described by $2N$ open-loop transfer functions $G_i(j\omega)$ defined starting from the signal flow graph and its $(2N-1)$ subgraphs of the incident and reflected waves at the interface ports. Lack of encirclements of the point $(1,0)$ in the Nyquist plot of each open-loop transfer function $G_i(j\omega)$ ensures stability for a given couple of terminations (Γ_S, Γ_L). In order to allow CAD-based stability check during the optimization procedure, all the $G_i(j\omega)$ have to be calculated simultaneously [5] and stability goals have to be evaluated in each of optimizer iterations. It is not possible to inspect Nyquist plots within the optimization routine, so an equivalent formulation is required

for stability criteria. Here we propose new conditions, suitable to be evaluated during the optimization step, which guarantee circuit stability according to the procedure in [4], with prefixed stability margins.

A circuit is stable with a gain margin m_g if the following condition is fulfilled:

$$|G_i(j\omega)| \cdot \Phi(\arg(G_i(j\omega))) < 1 - m_g, \quad i = 1, 2, \ldots 2N \quad (1)$$

where the function Φ is defined as

$$\Phi\left(\arg\left(G_i(j\omega)\right)\right) = \begin{cases} 1, & \text{if } \arg\left(G_i(j\omega)\right) = 0 \\ 0, & \text{if } \arg\left(G_i(j\omega)\right) \neq 0. \end{cases} \quad (2)$$

Similarly, the circuit is stable with a phase margin m_φ if

$$\arg(G_i(j\omega)) \cdot \Psi(|G_i(j\omega)|) > m_\varphi, \quad i = 1, 2, \ldots 2N \quad (3)$$

where the function Ψ is

$$\Psi(|G_i(j\omega)|) = \begin{cases} 1, & \text{if } |(G_i(j\omega)| \geq 1 \\ 0, & \text{if } |(G_i(j\omega)| < 1. \end{cases} \quad (4)$$

Functions Φ and Ψ cannot directly be used in a CAD during the synthesis procedure. In order to force a gain or a phase margin on the circuit during the optimization step we have derived approximating analytical expressions for functions Φ and Ψ suitable to be evaluated by CAD tools.

We have chosen, as approximating functions of $\Phi(\arg(G_i(j\omega)))$ and $\Psi(|G_i(j\omega)|)$

$$\Phi'(\arg(G_i(j\omega))) = \left[\cos\left(\frac{1}{2} \cdot \arg(G_i(j\omega))\right)\right]^n \quad (2')$$

and

$$\Psi'(|G_i(j\omega)|) = \frac{2}{\pi} \cdot \operatorname{arctg}(|G_i(j\omega)|^m) \quad (4')$$

respectively, for large values of the integer parameters n and m.

Function Φ' in (2′) is equal to one for $\arg(G_i(j\omega)) = 0$ and vanishes when $\arg(G_i(j\omega))$ is different from zero. Equation (1), where Φ' is used in place of Φ, can be used as an optimization goal to force $|G_i(j\omega)|$ to be less than $1 - m_g$ when $\arg(G_i(j\omega)) = 0$, so preventing functions $G_i(j\omega)$ to cross the real axis between $1 - m_g$ and infinity; thus, lack of encirclements of the point $(1, 0)$ with a margin m_g, as required by definitions (1) and (2), is guaranteed. A dual consideration can be done for conditions (3) and (4).

Conditions (1) and (2′) or (3) and (4′) ensure stability for a given couple of terminations and therefore, as stated in [3], allow achieving Proviso fulfilment if real positive terminations are considered; these conditions can be used together with the following ones related to termination variations [5]:

$$K_S(S, \rho_S, \rho_L) = \frac{1 - |S_{11}|^2\rho_S^2 - |S_{22}|^2\rho_L^2 + |\Delta|^2\rho_S^2\rho_L^2}{2\rho_S\rho_L|S_{12}S_{21}|} > 1 \quad (5)$$

$$B_S(S, \rho_S, \rho_L) = 1 - |S_{11}|^2\rho_L^2 - |S_{12}S_{21}|\rho_S\rho_L > 0 \quad (6)$$

to ensure conditional stability in given circular regions of the input and output termination planes Γ_S and Γ_L, or unconditional stability if ρ_S and ρ_L are chosen equal to one.

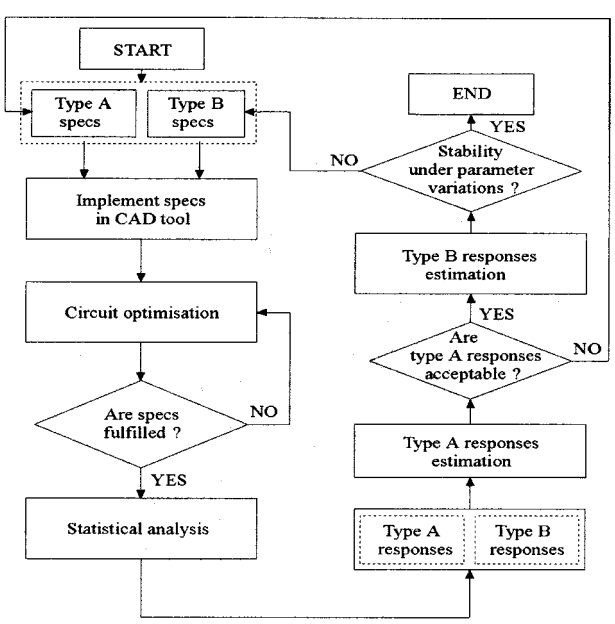

Fig. 1. Flowchart of the proposed design methodology.

III. Design Methodology

The design method is explained by the flowchart in Fig. 1: as a first step, the designer has to fix a set of specifications for gain, noise figure, input and output return losses (type A specs) which define the acceptability region. A preliminary study of package, interconnections and process parameters dispersion allows to choose both termination regions radii ρ_S and ρ_L stability margins m_φ or m_φ (type B specs), in order to guarantee circuit stability in spite of process parameter and termination variations.

Type A specs can be simply implemented in CAD tools, while in order to guide CAD optimizers to fulfill type B specs, conditions proposed in Section II can be used. In the next step the CAD tool optimizer automatically finds a set of optimal design factors. Then, a Monte Carlo analysis is performed in order to estimate both type A and type B circuit responses variability under parameter variations. If the yield found for type A responses is not satisfactory (i.e., it is lower than the prefixed value) type A specs have to be changed in order to reperform optimization. Otherwise, we can proceed to evaluate type B responses: if all the $G_i(j\omega)$ functions do not encircle the point $(1, 0)$ in the Nyquist plot for each of the Monte Carlo iterations (i.e., the circuit is stable under parameter variations), total yield is satisfactory and the design procedure ends. Otherwise, it is necessary to modify type B specs and reperform optimization.

The new method is oriented to design for manufacturing, and allows the synthesis step to be performed automatically by means of a CAD tool optimizer. At the end of the procedure the circuit fulfills given specifications with the prefixed yield and is stable in spite of parameter and termination variations considered in the statistical analysis.

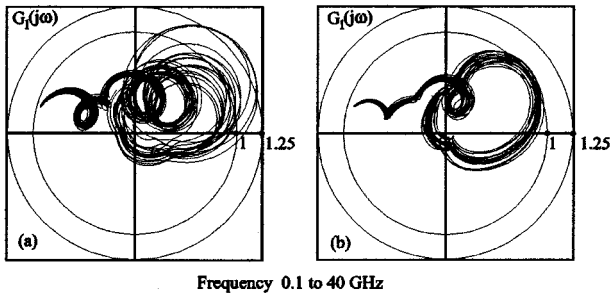

Fig. 2. Polar plot of the open-loop transfer function $G_1(j\omega)$: (a) denoting instability in some iterations of the Monte Carlo analysis and (b) showing stability for all the iterations of the Monte Carlo analysis.

IV. Case Study

The design methodology has been checked on a 4-FET distributed amplifier, a critical topology from the viewpoint of stability because of the large number of internal loops. The amplifier was designed to operate in 2–20-GHz frequency band with a minimal 11-dB 50-Ohm transducer gain and input and output reflection coefficients lower than -8 dB. NEC 32 400 GaAs FET's were employed in circuit design and HP-MDS CAD software was used to carry out circuit optimization. A stability check was performed on the optimized circuit by using the methodology proposed in [4] and stability was ascertained for the nominal case [none of the eight open-loop transfer functions $G_i(j\omega)$ encircled the critical point]. Anyway, a Monte Carlo analysis implemented on the circuit varying the noise factors in their tolerance regions (i.e., $\pm 10\%$ for microstrip lines and capacitance values, $\pm 15\%$ for resistance values and $\pm 25\ \Omega$ for both the resistance and reactance of input and output terminations) showed that the circuit was driven to instability by parameter variations [Fig. 2(a)]. The amplifier was then redesigned according to the flowchart in Fig. 1, setting the design goals reported in Table I. A Monte Carlo analysis performed on the obtained circuit showed that the circuit was stable under parameter variations [Fig. 2(b)]. Simulated performance reported in the Table I highlights a good agreement with the fixed design goals, thanks to conditions discussed in Section II which allow an easy tradeoff between performance and stability.

TABLE I
Design Goals and Optimized Performance

Design Goals	Optimized Performance
S21>11 dB	S21=11.7 dB
BW =2-20 GHz	BW = 2-20.5 GHz
S11 < -8 dB	S11< -9.2;
S22 < -8 dB	S22 < -8.3 dB
Gain Margin > 0.2	$m_g = 0.22$
Phase Margin> 45°	$m_\phi = 48°$
$K_S(\underline{S}, \rho_S=0.5, \rho_L=0.5)>1$	$K_S(\underline{S}, \rho_S=0.5, \rho_L=0.5)>1.95$

V. Conclusion

A new design methodology has been developed, which allows synthesizing circuits with a prefixed yield estimated taking into account also stability requirements under termination and process parameter variations. Unlike previous design methodologies, where stability check was performed after circuit optimization leading often to a time-consuming trial and error process, the proposed method allows to include stability margins among the goals of a circuit synthesis by CAD tools optimizer by means of a new set of stability conditions. A case study of a 4-FET distributed amplifier design has been presented in which desired performance and stability under parameter variations have been achieved by using the proposed methodology.

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