Computer Modeling of Bistability Effect in P-I-N Diode Limiter Characteristic

Nikolai Drozdovski and Tadashi Takano

***Abstract*—The bistability effect noted in p-i-n diode limiters has been studied using a computer simulation based on the one-dimensional drift-diffusion model (DDM). Computed results for silicon p-i-n diodes with different base width are shown. Frequency properties of the bistability effect were studied. Also the comparison between theoretical and experimental results is shown.**

***Index Terms*—Bistability, limiter, p-i-n diode.**

I. Introduction

NONLINEAR properties of p-i-n diodes have been studied extensively [1]–[]. The bistability phenomenon in the p-i-n diode limiters is an interesting nonlinear effect, illustrated in Fig. 1. When the input power $P_{\rm in}$ increases from zero, the output power $P_{\rm out}$ increases nearly linearly with the input power. There is a jump of the output power at an input power P_1; the output power increases slightly with the input power increase above this power P_1. When the input power decreases from its maximum value, the reverse jump of the output power takes place at another power $P_2 < P_1$.

An improved method to compute this limiter characteristic with bistability using the computer program ISTOC [], based on the one-dimensional drift-diffusion model (DDM), is under consideration in this letter.

II. Simulation Technique

There are several programs based on DDM that have been used for p-i-n diode simulation in limiting applications, but they do not show the bistability effect [2], [6], [7] because conventional modeling techniques do not provide detection and computation of the bistability area. Two ways to overcome this problem were reported in [4], [5], but both of these modifications have limitations based on the need to look over a considerable number of manual iterations in many points of the limiter characteristic.

The circuit configuration used for our computations is presented in Fig. 2. The load resistance Z_2 and the series resistance Z_1 are equal to the transmission line characteristic impedance of 50 Ω. Input data to the program are the geometry of the semiconductor and contact regions, the doping profile of the p-i-n diode and the values of lumped-elements forming the circuit.

The waveforms of diode voltage $V_d(t)$ and current $I_d(t)$ are computed with an input signal $V(t)$ at fixed frequency and

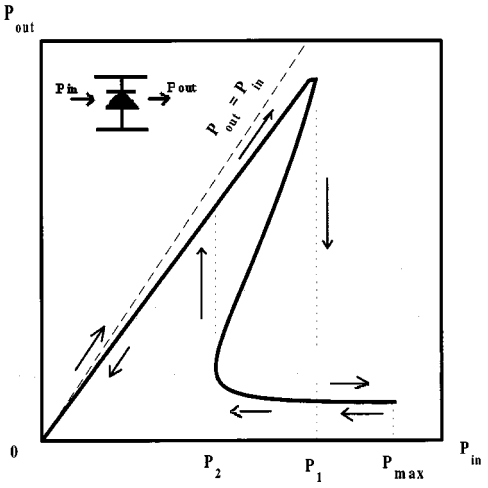

Fig. 1. Limiter characteristic of p-i-n diode with bistability area.

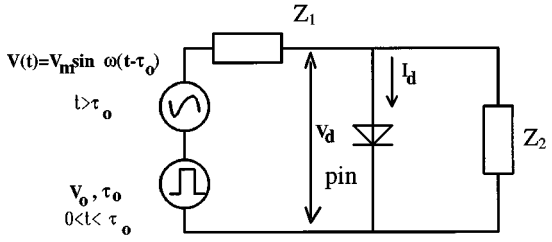

Fig. 2. Circuit used in simulations.

amplitude. The program solves the continuity equations for electrons and holes, the Poisson equation and the total current equation. To approximate the stationary state of the diode a big number of the input signal cycles were used. The input and output power calculations for the limiter curves were carried out using an additional Fourier analysis program [6].

A novel method for the bistability area detection is based on this program. There are two stable states in the bistability area, so it is necessary to have at least two different initial conditions for the calculation: the first condition is the so-called "high-impedance diode" and the second one is the "low-impedance diode."

The first initial condition corresponds to an unbiased p-i-n diode and which was used to compute direct motion of the limiting characteristic (input RF power increases from 0 to P_1 and from P_1 to $P_{\rm max}$, see Fig. 1).

The second initial condition is realized using forward-biased rectangle pulse before starting the RF cycles. Parameters of this pulse (amplitude V_o and duration τ_o) are defined once for each

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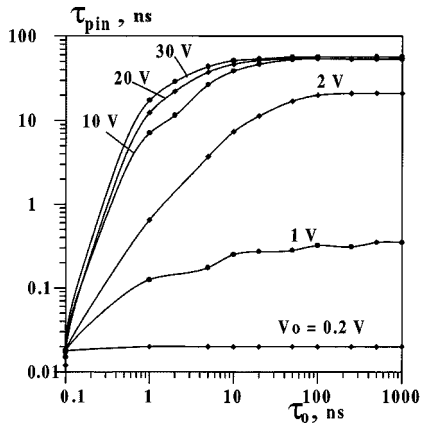


Fig. 3. Transition off time versus pulse duration and amplitude.

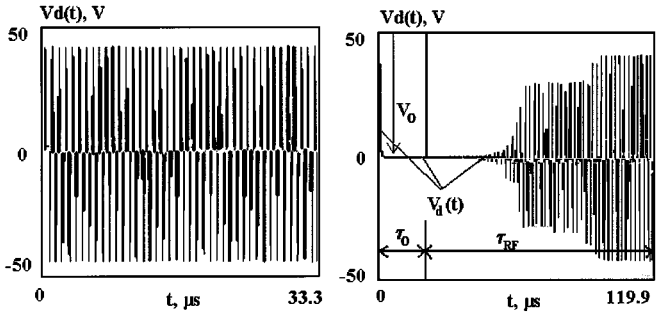
diode. This procedure for a 5-μm p-i-n diode is shown in Fig. 3. This figure shows the computed transition off time t_{pin} versus the pulse duration t_o with different pulse amplitudes V_o. From Fig. 3, starting from the point about 100 ns and amplitude 10 V (5 V applied across the diode), further increases of pulse duration and amplitude do not cause an increase in p-i-n diode transition off time. The pulse with the above-mentioned parameters is sufficient to transition the p-i-n diode to the low impedance (the "low impedance diode" initial condition). The second condition was used to compute the reverse motion of the limiting characteristic (input RF power decreases from $P_{\max}$ to P_2 and from P_2 to 0, see Fig. 1). Note, that for $t > \tau_0$ there is no dc pulse and the RF signal is applied to the initially low impedance p-i-n diode. The superposition of these two computed curves for two different initial condition gives us the total limiting curve. If there is no bistability area, all computed points from the two curves must coincide.

III. Calculation Examples

The computer simulation of bistability in p-i-n diodes was made over a wide frequency range for silicon p-i-n diodes with a p^+-n-n^+ structure. The 150 μm p-i-n diode used in simulation had a I-layer doping level of 5×10^{12} cm^{-3}, a cross section of 3.14×10^{-2} cm^2, and electron and hole lifetimes of 10 μs. The diode doping profile was assumed to be an error function with acceptor p^+ and donor n^- concentrations of 5×10^{19} cm^{-3} and 10^{20} cm^{-3}, respectively. Figs. 4–6 show the computed diode voltage $V_d(t)$ for a p-i-n diode with an I-layer thickness of 150 μm at the frequency 30 MHz.

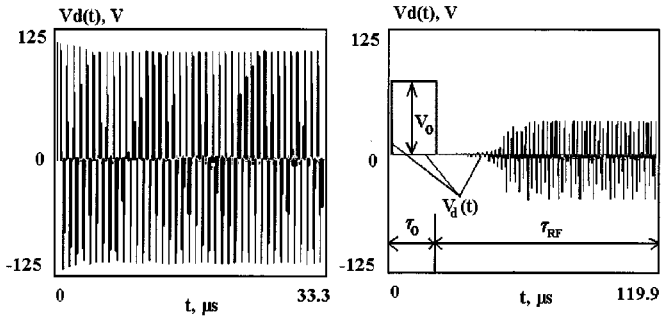
Fig. 4 shows $V_d(t)$ simulation with the amplitude of the input signal V_m corresponding to the input power between 0 and P_2 of the limiting characteristic (see Fig. 1). Fig. 5 shows similar simulations but with the V_m for the input power between P_2 and P_1, and Fig. 6—with the amplitude of the input signal V_m corresponding to the input power between P_1 and $P_{\max}$.

Results computed for the first initial condition (high-impedance diode) are shown in Figs. 4(a), 5(a), and 6(a). It corresponds to a direct motion of limiting characteristic (input RF power increases from 0 to $P_{\max}$). There are one thousand RF cycles in Fig. 4(a), Fig. 5(a) and 200 RF cycles in Fig. 6(a).



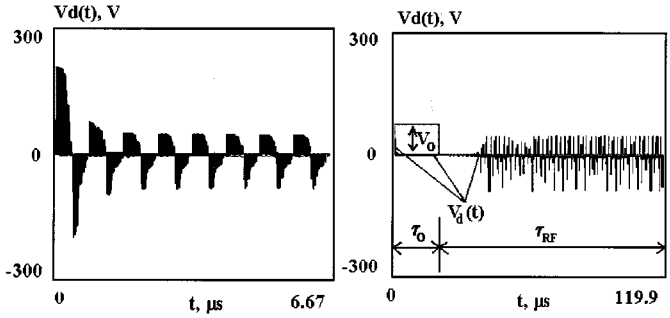
(a) (b)

Fig. 4. RF voltage across 150 μm silicon p-i-n diode versus time, $f = 30$ MHz, $V_m = 100$ V: (a) first initial condition ("high impedance diode") and (b) second initial condition ("low impedance diode").



(a) (b)

Fig. 5. RF voltage across 150 μm silicon p-i-n diode ersus time, $f = 30$ MHz, $V_m = 250$ V: (a) first initial condition ("high impedance diode") and (b) second initial condition ("low impedance diode").



(a) (b)

Fig. 6. RF voltage across 150 μm silicon p-i-n diode versus time, $f = 30$ MHz, $V_m = 600$ V: (a) first initial condition ("high impedance diode") and (b) second initial condition ("low impedance diode").

Results obtained for the second initial condition (low-impedance diode) are shown in Figs. 4(b), 5(b), and 6(b). It corresponds to a reverse motion of limiting characteristic (input RF power decreases from $P_{\max}$ to 0). In these cases, the rectangle pulse with amplitude of $V_o = 80$ V and duration of $t_o = 20$ μs was used to realize the low-impedance state of the diode. Three thousands of RF cycles corresponding to the RF signal duration of $t_{\rm RF} = 99.9$ μs were used.

One can see that the computed ac voltage stationary values across p-i-n diode for an input power $P_{\rm in} < P_2$ [Fig. 4(a) and (b)] and $P_{\rm in} > P_1$ [Fig. 6(a) and (b)] coincided for different initial conditions. When diode initially is in high-impedance

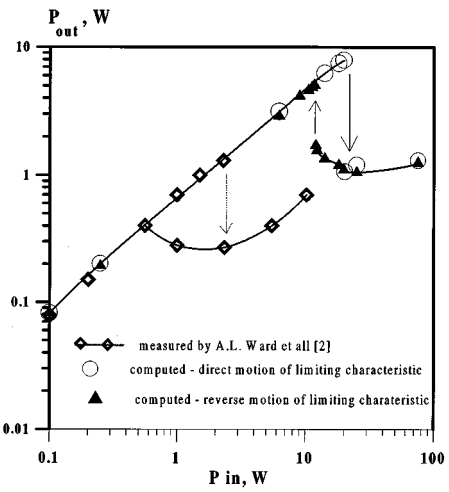


Fig. 7. Comparison of computed and measured [2] results for 10-μm silicon p-i-n diode.

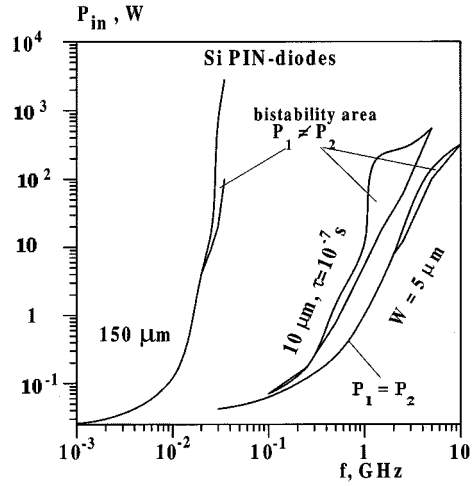


Fig. 8. The bistability area as a function of operating frequency for 5-, 10-, and 150-μm silicon p-i-n diodes.

state the input power over the range 0 and P_2 is insufficient to change the PIN diode to conducting low-impedance state [Fig. 4(a)]. On the other hand the same input power also is insufficient to keep diode in conducting state under the second (low-impedance) initial condition [Fig. 4(b)]. For $P_{\rm in} > P_1$ an input power is sufficient to transfer p-i-n diode from the high-impedance state to the low-impedance state [Fig. 6(a)] and to remain the low-impedance diode in its conducting state as seen in Fig. 6(b).

For an input power $P_2 < P_{\rm in} < P_1$ the stationary values of ac voltage are different [Fig. 5(a) and (b)]. An input power is still not enough to transfer high-impedance p-i-n diode to the low-power state [Fig. 5(a)], but it is sufficient to keep low-impedance diode in its conducting state [Fig. 5(b)] It indicates operation in the bistability area.

Silicon p-i-n diodes with 5- and 10–μm base width were also studied. Other parameters includes a cross section of 3×10^{-4} cm^2, an I-layer doping level of 4×10^{13} cm^{-3} and electron and hole lifetimes of 10 μs. Simulations show a highly pronounced bistability region for both diodes. This fact is in agreement with the computed results obtained for thinner diodes [5] and with experimental results obtained for a 10 μm silicon p-i-n diode [2], but it is contradictory with the statement about the bistability region absence for the 10-μm p-i-n diode in studied in [6].

The computed limiting characteristic for the 10-μm p-i-n diode at a frequency of 1.5 GHz is shown in Fig. 7 with experimental data points [2] for the same frequency. The general agreement between the computed and experimental results is quite good. The calculated limiter curve shows a highly pronounced bistability area. Some qualitative difference between the theoretical and measured curves is observed, which may be explained by incomplete knowledge of the p-i-n diode used [2] and the p-i-n diode model parameters used in these simulations.

Fig. 8 summarizes the computed limiting characteristics of p-i-n diodes with 5, 10, and 150 μm, showing the bistability areas ($P_1 \neq P_2$) versus RF input signal frequency. Note the bistability area is moved to lower frequencies with an increase in I-layer thickness. This is in agreement with all previous theoretical and experimental results [1]–[5]. In addition, frequency range of the bistability effect for the 150-μm diode is very close to the observed experimental frequency range [1], [4]. The bistability effect is detected over a specific frequency range determined by diode geometry, semiconductor material properties, and even external circuit parameters. Its appearance is the result of the field redistribution inside the I-layer between the depleted and nondepleted regions [1], [5] (the same bistability effect recently was observed in two-diode chains series p-i-n and Schottky diodes [3]) with RF input power increase and decrease.

IV. Conclusion

An improved method of simulating p-i-n diode limiting characteristic with bistability was shown. This model provides more accurate results and requires less computational time.

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