Substrate Crosstalk Suppression Capability of Silicon-on-Insulator Substrates with Buried Ground Planes (GPSOI)

J. S. Hamel, *Member, IEEE*, S. Stefanou, M. Bain, B. M. Armstrong, and H. S. Gamble

***Abstract*—Experimental s_{21} transmission crosstalk studies have been conducted on silicon-on-insulator substrates with buried ground planes (GPSOI's) where a 2 Ω per square metal-silicide buried ground plane existed between a 15 Ω-cm p-type silicon substrate and a 1 μm thick buried CVD oxide layer. Locally grounded transmission test structures fabricated on GPSOI were found to exhibit 20 dB increased crosstalk suppression compared to published data for high resistivity (200 Ω-cm) SOI substrates incorporating capacitive guard rings over a frequency range from 500 MHz to 50 GHz. This represents an order of magnitude improvement in crosstalk power suppression capability compared to existing state-of-the-art suppression techniques in silicon substrates.**

I. Introduction

INSUFFICIENT crosstalk isolation between devices and circuits at rf/microwave frequencies in standard silicon bulk and silicon-on-insulator (SOI) substrates presents significant limitations to the practical realization of highly integrated rf/microwave communication systems. SOI substrates with standard substrate resistivities (i.e., 15–20 Ω-cm), while offering superior isolation at lower frequencies compared to bulk substrates, offer no significant advantages at rf/microwave frequencies above a few hundred megahertz, and SOI substrates with high resistivities (i.e., 200–5000 Ω-cm) fail to provide improved isolation over standard low resistivity bulk silicon above 10 GHz [1].

In this paper, the crosstalk suppression capability of a new silicon substrate technology is presented and shown to be superior to existing advanced technologies. The approach taken involves the use of a buried metal ground plane which is placed below the oxide layer in what would otherwise be a standard silicon-on-insulator substrate. The resulting substrate structure will be referred to as a Ground Plane Silicon-On-Insulator (GPSOI). This SOI substrate is manufacturable by bonded silicon technology in a similar manner to that for silicon on metal-silicide on insulator (SMI or SSOI) substrates [2]. In this case, the difference in the process is that the WSi_2 layer is at the interface between the handle wafer (substrate) and the buried oxide rather than between the active layer and the buried oxide. For SOI substrates manufactured by bonded silicon technology the buried ground plane requires three additional process steps: 1) CVD of W Six, 2) contact via etch, and 3) refill. This is very similar to the addition of an extra layer of metallization and will incur a similar cost penalty.

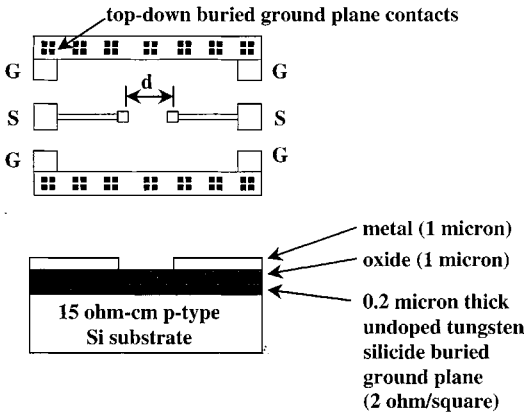

Fig. 1. GPSOI experimental crosstalk transmission structure with locally grounded buried ground plane.

At this time it is foreseen that this technology will enable higher levels of integration of mixed rf analog/digital telecommunication circuits, where the passive components of the analog circuits are lumped as opposed to distributed components. Under these circumstances, the inductor component quality factor would be most affected by the presence of a continuous buried ground plane unless the ground plane is appropriately patterned. The incorporation of patterned ground planes is actively being researched.

II. Experimental Results

Using an identical approach to [1] for high resistivity SOI, crosstalk suppression of the GPSOI was assessed by use of s_{21} transmission structures, as shown in Fig. 1, where square ($50\ \mu$m $\times 50\ \mu$m) Al metal pads with center separation d were fabricated in a ground-signal-ground (*GSG*) coplanar configuration on top of the oxide layer directly above the buried ground plane. Three substrate configurations were considered. As depicted in Fig. 1, the first structure was fabricated on a GPSOI substrate which consisted of a 15 Ω-cm p-type silicon substrate, a 0.2 μm thick 2 Ω per square buried WSi_2 silicide layer, and a 1.0 μm CVD oxide deposited from a TEOS precursor. In this case, the buried ground plane was electrically grounded locally by use of metallized vias such that the coplanar rf probe grounds were shorted directly to the buried silicide ground plane. The backside of the

Manuscript received November 29, 1999; revised February 4, 2000.

J. S. Hamel and S. Stefanou are with the Department of Electronics and Computer Science, University of Southampton, Southampton, U.K.

M. Bain, B. M. Armstrong, and H. S. Gamble are with the School of Electrical and Electronic Engineering, The Queen's University of Belfast, Belfast, U.K.

Publisher Item Identifier S 1051-8207(00)04026-5.

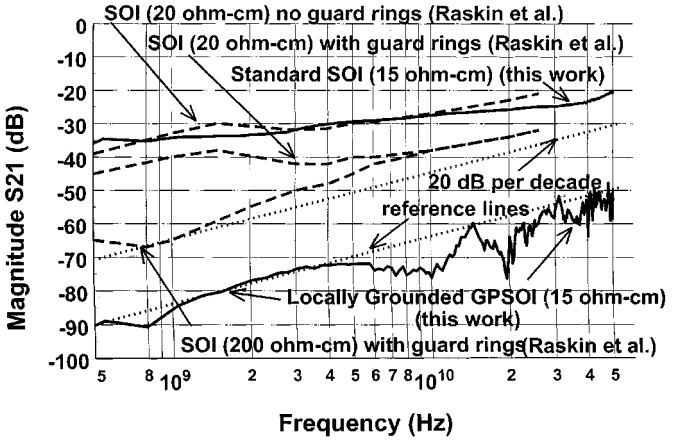

Fig. 2. Measurements of the magnitude of the s_{21} transmission parameter for the locally grounded crosstalk structure on GPSOI and the standard SOI. Results from previous work on low and high resistivity substrate SOI with and without guard rings [1] are shown for comparison. Pad separation was $d = 100\,\mu$m and pad areas were 50 μm$\times$50 μm for all cases.

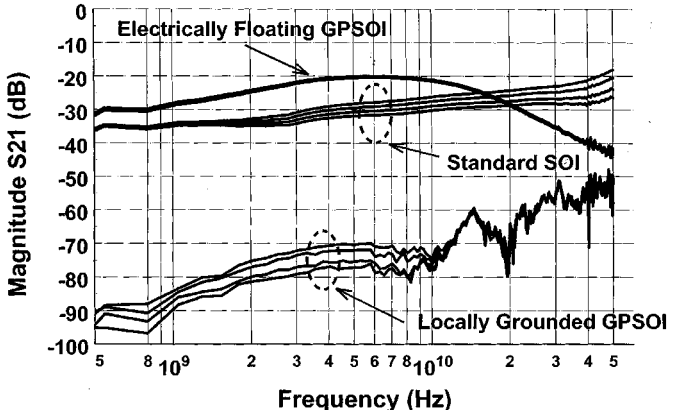

Fig. 3. Measurements of the magnitude of the s_{21} transmission parameter for the locally grounded and electrically floating crosstalk structures on GPSOI for distances d of 75, 100, 150, and 200 μm between metal pad transmission and receiver elements. Data is also shown for the standard SOI control.

wafer was left floating. The second structure was identical to the first but where the grounding vias were absent such that the buried ground plane was left to float electrically. The third structure was the control to represent conventional SOI technology and was identical to the second structure but with no buried ground plane and a CVD oxide layer thickness of 1.2 μm. The separation d between the centers of the rf signal pads was varied from 75 to 200 μm. Measurements were accomplished using an HP 85109C on-wafer s-parameter characterization system in the frequency range of 500 MHz–50 GHz in conjunction with tungsten-tip 150 μm pitch Cascade air-coplanar probes.

Fig. 2 shows s_{21} magnitude transmission plots versus frequency from 500 MHz to 50 GHz for two of the crosstalk structures, namely, the locally grounded GPSOI and the control SOI substrates. Metal pad separation d was 100 μm. The locally grounded crosstalk structure on GPSOI exhibited a high degree of crosstalk isolation ranging from 90 dB at 500 MHz rising to 50 dB at 50 GHz. The control, which is similar to widely available standard SOI substrates, exhibited crosstalk isolation of approximately 40 dB at 500 MHz rising to a little above 30 dB at 50 GHz. Published data from [1] for low and high resistivity SOI substrates with no buried ground planes with and without capacitive guard rings have been plotted in Fig. 2 for comparison, where identical transmission structures, pad separations, and pad dimensions were reported to have been used directly on the buried oxide layer. The grounded GPSOI structure is seen to provide 20 dB greater crosstalk isolation than the best of these structures from [1].

Fig. 3 shows magnitude of s_{21} transmission data for the three structures including locally grounded GPSOI, electrically floating GPSOI, and the control with no buried ground planes. Data is shown for all three structures for pad separations d of 75, 100, 150, and 200 μm. Crosstalk isolation was observed to increase by approximately 2 dB per 50 μm of pad separation in the grounded GPSOI structures below 10 GHz which is similar to what was reported for high resistivity SOI substrates with no buried ground planes [1]. Both the floating and standard SOI structures exhibited little variation of crosstalk with pad separation over most of the frequency range, with the floating GPSOI displaying significant increased crosstalk compared to the standard SOI. These results indicate that it would be essential to provide ground plane grounding for devices and circuits fabricated on GPSOI, or to pattern the buried ground plane. The data in Fig. 3 indicates that the locally grounded GPSOI provides the same advantage as high resistivity SOI without buried ground planes by accommodating increased crosstalk isolation with increased spacing between components, while at the same time providing greatly increased crosstalk isolation for a given component separation.

REFERENCES

[1] J. Raskin, A. Viviani, D. Flandre, and J. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Trans. Electron Devices*, vol. 44, pp. 2252–2261, Dec. 1997.

[2] W. Goh, D. Campbell, B. Armstrong, and H. Gamble, "Buried metallic layers with silicon direct bonding," *Spring Meeting of the Electrochem. Soc.*, vol. 95–97, pp. 553–560, May 1995.