Low-Loss Cascadable MEMS Distributed X-Band Phase Shifters

Joseph S. Hayden and Gabriel M. Rebeiz

***Abstract*—A wideband distributed coplanar-waveguide (CPW) phase shifter has been developed for X-band operation. The design is based on the distributed MEMS transmission line (DMTL) loaded with high capacitance-ratio varactors. The varactors are fabricated using a series combination of MEMS bridges and fixed-value MIM capacitors. A high-capacitance ratio varactor (1.5–2.5) results in a large loading on the CPW line and therefore a large phase shift. A distributed phase shifter was fabricated on a 500 μm quartz substrate, and achieved a true-time delay operation from 1 to 10 GHz with a reflection coefficient less than −15 dB, and 180°/dB of insertion loss at 8–10 GHz. It is possible with this design to cascade the DMTL to result in 2- and 3-bit phase shifters with excellent wideband performance at X-band frequencies.**

***Index Terms*—Distributed circuit, MEMS, phase shifter.**

I. Introduction

THE distributed phase shifter consists of a high impedance line (>50 Ω) capacitively loaded by the periodic placement of discrete varactors [1]. By applying a single bias voltage on the line, the distributed capacitance can be changed, which in turn changes the phase velocity of the line and creates a true-time delay phase shift. The phase shift can be varied from 0 to 360° depending on the bias voltage and the length of the distributed line. This technique has been recently optimized by Nagra *et al.*with Schottky diode varactors [2], [3], and have shown good performance with 86°/dB insertion loss at 20 GHz. However, the millimeter wave performance of these devices is limited by the series resistance of the diodes which is typically 2–5 Ω. This problem was solved by Barker *et al.* [4], [5] with the use of suspended MEMS varactors over a coplanar-waveguide (CPW) line. The MEMS varactors have a series resistance of 0.15 Ω and result in excellent performance at mm-wave frequencies with 90°/dB and 72°/dB insertion loss at 60 GHz and 100 GHz, respectively.

The performance of the DMTL was limited by the MEMS capacitance ratio of 1.2. Mechanical instability of the MEMS bridge under a constant dc bias voltage resulted in a theoretical usable capacitance ratio of 1.5 and a practical limit of 1.2–1.3 [4]. Furthermore, the designs of Nagra and Barker are based on an analog bias voltage and therefore any electrical noise on the bias line will transfer into phase noise at the output of the device.

The purpose of this work is twofold: first, to turn the distributed MEMS phase shifter into a "digital" design which is not sensitive to electrical noise; and second, to develop a distributed MEMS phase shifter which has a large capacitance ratio (1.5–2.5) resulting in a large phase shift with minimal insertion loss.

The mechanical integrity of MEMS switches is of current research [6]. MEMS switches have been cycled up to several million times in clean room environments with very low humidity. If MEMS switches are to be used in standard applications, then the MEMS switch or phase shifter needs to be packaged to shield it from dust, humidity, and oil vapor. In this phase shifter design, all the MEMS switches activate at the same time since the charging time constant of the CPW line is much smaller than 1 μs.

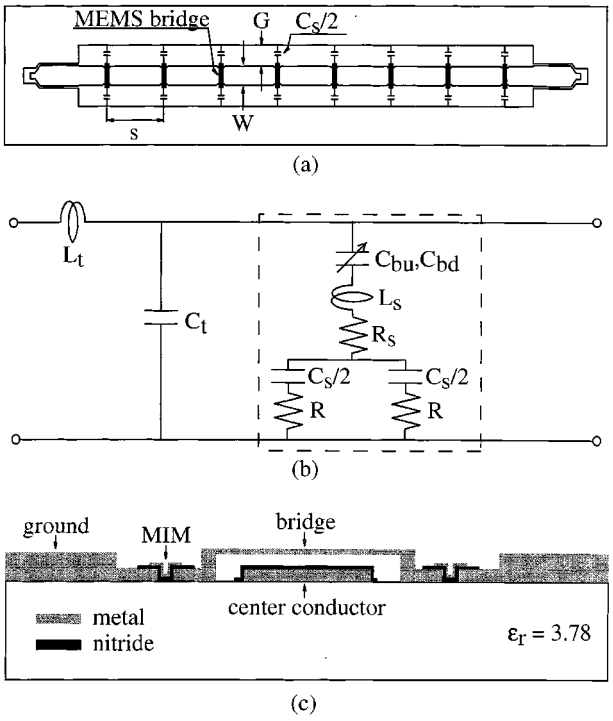

Fig. 1. (a) CPW phase shifter with MEMS bridges and MIM capacitors. (b) Distributed lumped model. (c) Cross-sectional sketch of the MEMS bridge.

II. Design of the Distributed MEMS Phase Shifter

The "digital" distributed MEMS phase shifter is shown in Fig. 1 together with the equivalent circuit model of a single period, s. The design is composed of a periodically loaded line with MEMS bridges in series with lumped element capacitors. The load capacitance seen by the line is the series combination

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of the bridge capacitance (C_b) and the total lumped capacitance (C_s) and is

$$C_l = C_s C_b/(C_b + C_s). \tag{1}$$

When the MEMS bridge is in the up-state position, the bridge capacitance (C_{bu}) is, in the limit, much smaller than C_s and the effective capacitance seen by the line, is $C_{lu} \approx C_{bu}$. When a bias is applied on the line and the MEMS bridge is in the down-state position, the bridge capacitance (C_{bd}) increases by a factor of 40–80 and becomes much larger than C_s, thereby resulting in a load capacitance of $C_{ld} = C_s$. The distributed capacitance can therefore be "discretely" controlled by the independent choice of C_{bu} and C_s. In most designs, $C_{bu} \approx C_s/4$ to C_s, and the capacitance ratio can be varied from 5 to 2.

If the down-state MEMS capacitance, C_{bd}, is much larger than C_s, then the exact value of C_{bd} is not important. This provides a relief in the fabrication process since the MEMS bridge capacitance ratio actually changes from 20 to 80 depending on the roughness of the metal and the dielectric layer underneath the MEMS bridge. Therefore, the performance of the distributed phase shifter is relatively independent of the MEMS bridge capacitance ratio (and the fabrication procedure) as long as the phase shifter is designed to have $C_{bd} \gg C_s$ and the MEMS capacitance ratio is larger than 10–20.

The phase shift of the DMTL can be calculated to be:

$$\begin{aligned}\Delta\phi &= \omega\sqrt{L_t C_t}\left(\sqrt{1+\frac{C_{lu}}{sC_t}} - \sqrt{1+\frac{C_{ld}}{sC_t}}\right) \\ &= \frac{\omega Z_o\sqrt{\epsilon_{r,eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \quad \text{rad/m}\end{aligned} \tag{2}$$

where Z_{lu} and Z_{ld} are the DMTL characteristic impedances for the low and high bridge capacitance states, and L_t and C_t are the unloaded CPW line inductance and capacitance, respectively. Z_o is the characteristic impedance of the unloaded CPW line, $c/\sqrt{\epsilon_{r,eff}}$ is the guided velocity of the unloaded CPW line.

The phase shift is determined by the impedance change of the DMTL, which also determines the reflection coefficient of the phase shifter. For this design, a maximum reflection coefficient of -15 dB is required since the DMTL is to be cascaded in 90° and 180° sections to result in a two-bit phase shifter. Therefore, the impedance of the distributed line in the up-state position cannot be higher than 60 Ω. Fig. 2 shows the calculated phase shift vs. frequency for an unloaded CPW line impedance of 102 Ω on a quartz substrate (ϵ_r = 3.8) with Z_{lu}/Z_{ld} = 60/44 Ω ($S_{11} < -15$ dB) and $Z_{lu}/Z_{ld} = 70/38$ Ω ($S_{11} < -10$ dB). It is shown that a much larger phase shift can be obtained with the 70/38 Ω design, albeit with the use of a larger capacitance ratio. The price paid is an increase in the reflection coefficient of the device, which results in poor performance for cascadable phase shifters.

III. Fabrication and Measurements

The DMTL is designed for 10 GHz operation and is composed of a 900 μm wide (W + 2G) CPW line with 284 μm center (G) conductor. The CPW line is wide for reduced ohmic loss. The DMTL is composed of 18 MEMS bridges at a spacing of

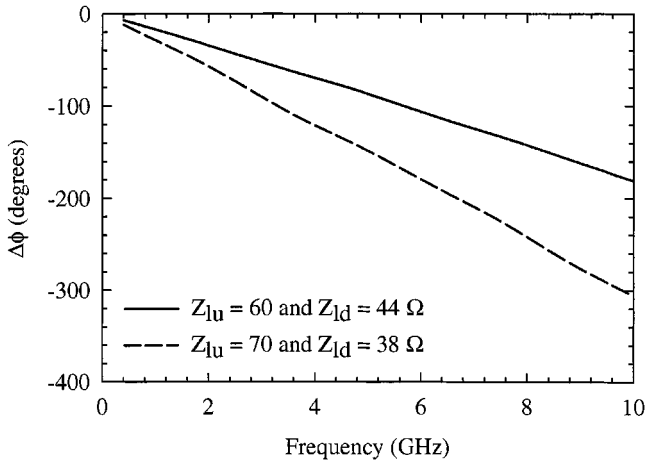

Fig. 2. Simulated results from a 18 bridge MEMS phase shifter. s = 884 and 767 μm for the 60/44 and 70/38 Ω cases, respectively. s is changed to maintain the same Bragg frequency of 30 GHz. Z_o is 102 Ω.

884 μm. The bridges are 350 μm long, 60 μm wide and suspended at a height of 1.5 μm above the substrate. A 2000 A nitride layer is used as the insulating dielectric between the CPW center conductor and the MEMS bridge. The conductor under the MEMS bridge is 5000 A thick. The fabrication procedure of the MEMS bridges follows [4]. The CPW center conductor and ground plane are electroplated to 3 μm high except underneath the MEMS bridge.

The pull down voltage of the MEMS bridges was 40 V. This is larger than usual (15–20 V) due to the series division of the applied voltage between the MEMS bridge and C_s. The bridges are connected to two MIM capacitors with a Q of 50–100 at 8–10 GHz. The MIM capacitors are fabricated in the CPW gap using the nitride layer of the MEMS bridge.

The simulated and measured performance of the DMTL phase shifter is shown in Fig. 3. The expected up-state capacitance of the MEMS bridge is 134 fF, calculated using a three-dimensional electrostatic simulator [7], with a series resistance of 0.1 Ω and a series inductance of 20 pH (which does not have an effect at X-band). The actual bridge capacitance is 200 fF due to the residual stress in the bridges which reduced the bridge height. In this design, C_s = 190 fF, resulting in a capacitance change (C_{td}/C_{tu}) of 1.76 and an impedance shift from 57 to 46 Ω in the up and down-states, respectively. The simulations are done on Libra, and include the CLR model of the MEMS bridge, the CR model of the finite Q MIM capacitor, and the loss of the unloaded CPW line. The down-state Bragg frequency is 30 GHz, making this phase shifter cascadable up to 12 GHz with a reflection coefficient of -14 dB.

The DMTL results in excellent return loss from 4 to 10 GHz (< -15 dB) in both the up-state and down-state positions. It is seen that the measured data agrees quite well with the simulations. The measured phase shift (Fig. 4) at 8–10 GHz is 95–123° with an insertion loss of 0.6–0.7 dB. This results in a 180°/dB of insertion loss at 8–10 GHz, and is excellent for wideband cascadable phase shifters. As usual of distributed phase shifters, the performance is best in the upper frequency range since the loss increases as $\sqrt{f}$ while the phase shift increases as f. The

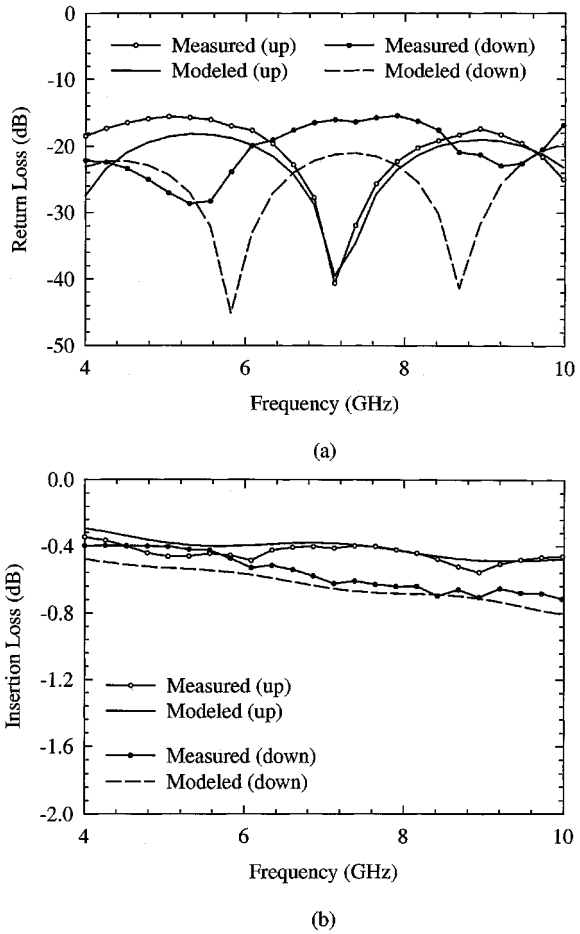

Fig. 3. Measured and modeled (a) return and (b) insertion loss of the MEMS phase shifter.

measured performance is comparable to state-of-the-art X-band MEMS phase shifters based on Lange couplers and resulting in a loss of 1.5 dB/360° [8].

IV. Conclusion

A novel topology for a "digital" distributed MEMS phase shifters has been proposed and implemented at 10 GHz. The novel topology is relatively insensitive to the MEMS capacitance ratio and the fabrication procedure. The DMTL performance can be further improved with the use of $C_s = 230$ fF and

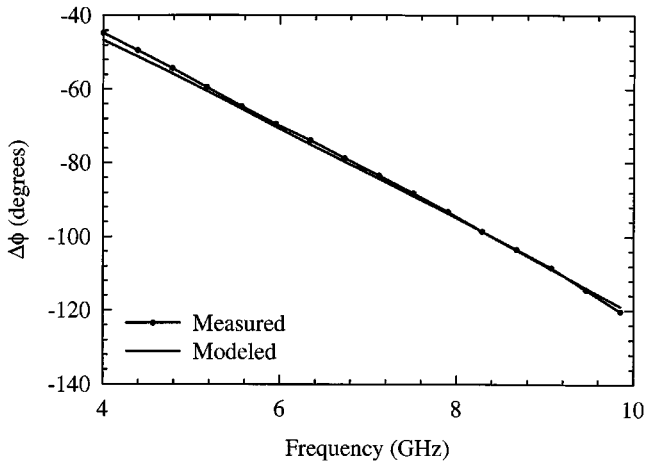

Fig. 4. Measured and modeled phase response of the MEMS phase shifter.

tuning the bridge capacitance to 134 fF while still maintaining a low reflection coefficient ($S_{11} < -15$ dB). The DMTL is designed to yield a low reflection loss so as to be cascadable in 90 and 180° sections. This results in a 2-bit phase shifter with a maximum S_{11} of -11 dB and an insertion loss of 1.0 ± 0.3 dB at 10 GHz.

References

[1] M. J. W. Rodwell, S. T. Allen, R. Y. Yu, M. G. Case, U. Bhattacharya, M. Reddy, E. Carman, M. Kamegawa, Y. Konishi, J. Pusl, and R. Pullela, "Active and nonlinear wave propagation devices in ultrafast electronics and optoelectronics," *Proc. IEEE*, vol. 82, pp. 1037–1059, July 1994.

[2] A. S. Nagra, J. E. Xu, and R. A. York, "Monolithic GaAs phase shifter circuit with low insertion loss and continuous 0–360 degree phase shift at 20 GHz," *IEEE Microwave Guided Wave Lett.*, vol. 9, pp. 31–33, Jan. 1999.

[3] A. S. Nagra and R. A. York, "Distributed analog phase shifters with low insertion loss," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 1705–1711, Sept. 1999.

[4] N. S. Barker and G. M. Rebeiz, "Distributed MEMS true-time delay phase shifters and wideband switches," *IEEE Trans. Microwave Theory Tech.*, pt. 2, vol. 46, pp. 1881–1890, Nov. 1998.

[5] ——, "Optimization of distributed MEMS phase shifters," *IEEE MTT-S Int. Symp. Dig.*, 1999.

[6] E. A. Sovero, R. Mihailovich, D. S. Deakin, J. A. Higgins, J. J. Yao, J. F. DeNatale, and J. H. Hong, "Monolithic GaAs PHEMT MMIC's integrated with high performance MEMS microrelays," in *Int. Microwave and Optoelectronics Conf.*, Rio de Janeiro, Brazil, Aug. 1999.

[7] Maxwell, Ansoft Corporation, , Pittsburgh, PA.

[8] A. Malczewski, S. Eshelman, B. Pillans, J. Ehmke, and C. L. Goldsmith, "X-band RF MEMS phase shifters for phased array applications," *IEEE Microwave Guided Wave Lett.*, vol. 9, pp. 517–519, Dec. 1999.