

A High-Power W-Band Monolithic FGC Doubler

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Abstract—This paper describes the realization of a high-output power W-band planar monolithic doubler using finite ground coplanar lines. The design of this doubler is based on two parallel pairs of varactor Schottky diodes fabricated on GaAs substrate. Measured results indicate a 12.5% efficiency at 74 GHz, a minimum 3-dB bandwidth of 12.5%, a return loss of -15 dB and a maximum output power of 115 mW. To the authors' knowledge, this is the highest output power level reported for a planar/monolithic W-band doubler.

I. INTRODUCTION

LOCAL oscillator sources are an important part of all high-frequency transmitters and receivers. Most millimeter-wave multipliers are based on waveguide circuits that have the low loss and high quality factor needed for efficient multiplier operation and can also include tuners and backshorts to optimize for peak performance. Several waveguide-based multipliers have achieved very high efficiencies and output power levels [1], [2]. However, waveguide mounts are complex to design and become more difficult and expensive to machine with increasing frequency and smaller size. An alternative approach is to use many diodes and quasi-optical techniques to greatly increase the power output [3]. This approach allows the power generation and tuning to function on a spatial grid with each grid element's having printed tuning elements. The result is usually increased power and reduced efficiency when compared to waveguide multipliers.

Another multiplier approach is monolithic microwave integrated circuit (MMIC) multipliers. Many similar MMIC multipliers can be fabricated at the same time using standard integrated circuit fabrication techniques, resulting in robust, small-size, and low-cost circuits. Planar circuits, however, tend to have higher loss and lower quality factor when compared to waveguide ones, and it is also more difficult to include tuning elements. Even with these limitations, some very useful MMIC multipliers have been reported: microstrip doublers with 25% efficiency at 94 GHz [4] and 2.8% efficiency at 320 GHz [5], as well as finite ground coplanar (FGC) broad-band doublers with efficiencies of 16.3% and 22% in W-band [6]. The effort of this paper is to demonstrate higher output power from a W-band planar doubler by using four Schottky diodes operating as varactors.

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TABLE I
MEASURED DC CHARACTERISTICS PER DIODE

R_S (Ω)	C_{jo} (fF)	C_p (fF)	η	V_{BR} (V)	f_C (GHz)
2.5	90	21.5	1.18	-11.5	571

II. DESIGN OF FGC DOUBLER

The planar doubler design is based on using two parallel pairs of Schottky diodes with matching and isolation networks at the input and output ports. These networks provide the appropriate conditions to match the diode impedances and block the fundamental and second harmonic from the output and input, respectively. All passive circuits are realized with FGC lines that provide transverse electromagnetic mode (TEM) characteristics and can be easily modeled [7]. A nonlinear multiple reflection software tool that takes into account the velocity saturation effects in the undepleted portion of the epitaxial layer during the radio-frequency (RF) cycle by including a velocity versus electric field expression for the drift current [8] has been used to design the varactor diodes. Input parameters are the epilayer thickness and doping concentration, the input Q of the diode (ratio of imaginary to real part of diode impedance), the fundamental frequency, and the input power. Output parameters include the input and output diode impedances at the fundamental and second harmonic, respectively, the anode area and efficiency, and the bias voltage. For an epilayer doping of $10^{17}/\text{cm}^3$ and a thickness of 4000 Å, the theoretically yielded anode area is $75 \mu\text{m}^2$, the input impedance around 40 GHz is $52-j106 \Omega$, the output impedance is $41.2-j56 \Omega$ at the second harmonic, the bias voltage is -3 V, and the efficiency is 32% (passive circuit losses not included).

In order to find the actual dc characteristics of the diodes needed for simulating more accurately the doubler performance (diodes and passive circuitry), some test diodes with the parameters calculated from the nonlinear multiple reflection program were fabricated on GaAs. The various diode parameters measured from the current–voltage (I – V) and capacitance–voltage (C – V) characteristics are summarized in Table I, where it is seen that the parasitic capacitance per diode is 21.5 fF. The zero bias capacitance C_{jo} is 90 fF, which is close to the theoretical value of 75 fF (the difference is due to fabrication tolerances in the anode area).

The matching and isolation networks at the input and output side were first designed in *Libra*, where the diodes were modeled as a series combination of a resistor and a capacitor (just for an initial estimate in the design). Quarter-wavelength open-end stubs were placed at the input and output that block second harmonic and fundamental, respectively. The diodes were connected to the 50Ω line with high-impedance (71Ω) inductive lines. In order to achieve a good matching at the input, a low

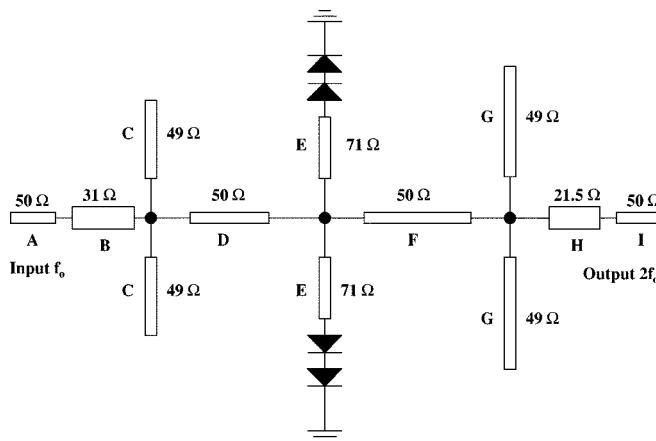


Fig. 1. Multiplier configuration with passive circuits and four diodes.

impedance section had to be inserted before the open-end stubs that trap the second harmonic (see Fig. 1). The dimensions and lengths of the various line segments were determined by the simulations and the mathematical relations linking the characteristic impedance and geometrical characteristics of an FGC line [9]. In the *Libra* simulation, each FGC line segment was modeled as an ideal transmission line with known effective dielectric constant and attenuation. This is correct since FGC lines support a TEM mode of propagation. Measured values of the attenuation and effective dielectric constant were used in these simulations [6].

With the lengths of the different line sections specified, the performance of the doubler was simulated in the harmonic balance test bench of *Libra*. Each diode was simulated with a pn junction model of known dc parameters (from measurements). Results can be seen in Fig. 2, where for a bias voltage of -3.5 V an efficiency of 13% and a bandwidth of 17% were achieved at an input frequency of 39 GHz. If the parasitic capacitance of 21.5 fF is not included (ideal case), then the efficiency increases to 18%. This shows the effect that diode parasitics have in the performance of the doubler. The discrepancy between the efficiency estimated by *Libra* and the one estimated by the nonlinear multiple reflection program is due to the passive circuit line loss that is accounted for in *Libra*.

III. RESULTS AND DISCUSSIONS

The four-diode doubler was fabricated on a GaAs wafer ($N_d = 1 \times 10^{17} \text{ cm}^{-3}$, thickness = 4000 Å) and a photograph of the actual circuit can be seen in Fig. 3, with the low-impedance sections at the input and output shown. A closeup of the diodes is shown in Fig. 4.

The measurement system for the performance evaluation of the doubler consisted of a Ka-band subsystem at the input that included a planar probe, a 3.5-mm male-to-male adaptor, a coax-to-waveguide transition, several WR-28 waveguide components, and a traveling wave tube source connected to an HP8510 network analyzer. At the output, the measurement system consisted of a subsystem that included a planar probe, a WR-10 waveguide, a WR-10 E-H tuner, and a power sensor and meter. Losses at the different components between the probe tips and the power meters were measured first in order

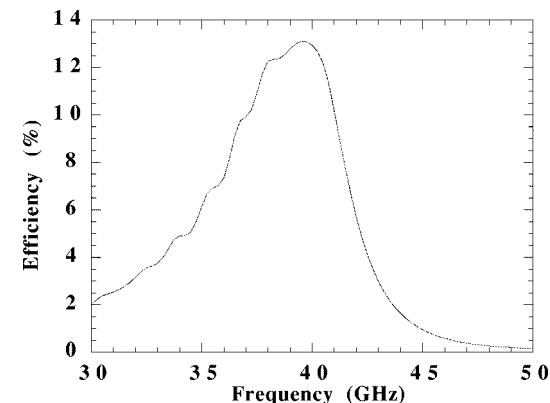


Fig. 2. Simulated efficiency versus input frequency for an input power of 20 dBm.

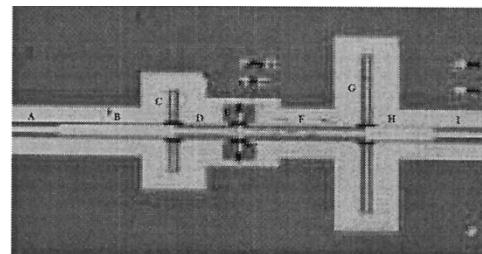


Fig. 3. Photograph of the fabricated four-diode doubler.

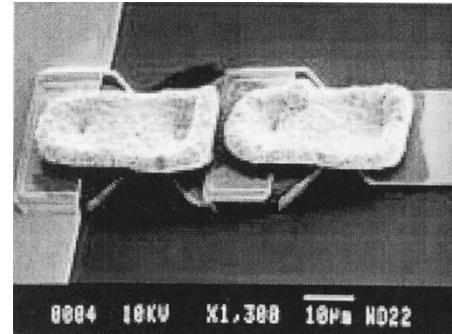


Fig. 4. Scanning electron microscope photo of two diodes in series.

to deembed them from the measured data. The total loss of the input subsystem was measured to be 3.5 ± 0.3 dB, while the loss of the output subsystem was found to be 3 ± 0.3 dB over the measurement band. The loss of each subsystem was evaluated by measuring the return loss of three planar standards (open, short, load) and solving for the S-parameters of the subsystem [10]. The WR-10 E-H tuner was placed at the output side after the probe to minimize any mismatches between the output part of the doubler and the diode impedances. As was observed in the measurements, the E-H tuner increased the measured efficiency by a small percentage only, due to the good matching achieved with the output circuitry of the doubler.

Efficiency measurements for an input power of 20 dBm can be seen in Fig. 5, where it is observed that an efficiency of 12.5% has been achieved at approximately 74 GHz with a return loss of -15 dB and a bandwidth of 12.5% for a bias voltage of -3.5 V. The actual bandwidth is larger but cannot be measured due to upper frequency limitations of the system setup. For 23 dBm of input power and the same bias voltage, the efficiency did

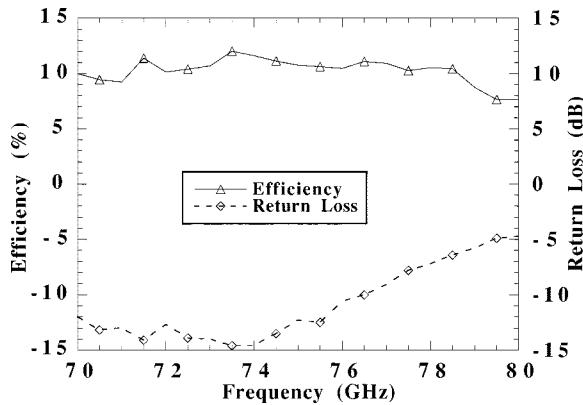


Fig. 5. Measured efficiency and return loss versus output frequency of the four-diode doubler for an input power of 20 dBm.

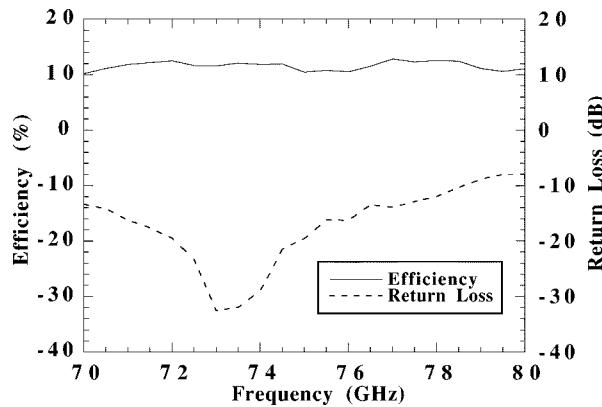


Fig. 6. Measured efficiency and return loss versus output frequency of the four-diode doubler for an input power of 23 dBm.

not change significantly, as can be seen in Fig. 6, but the return loss became better, especially for output frequencies above 76 GHz. This means that pumping the four-diode combination harder changes the impedances in a way that the input matching is improved, under the condition that the bias voltage does not change substantially. It should also be noted here that the E-H tuner at the output improved the output power of the doubler by 5 to 10%, when compared to the measurement with no tuner.

The measured output power versus input power at 74 GHz is shown in Fig. 7, where an output power of 115 mW was achieved for an RF input power of 1130 mW at 37 GHz and a -12 V bias voltage. Without the E-H tuner, the output power for the same input drive was measured to be 105 mW. Both of these measured power levels are the highest reported for a totally monolithic W-band doubler, to the best of the authors' knowledge. The combination of the high output power and the broad efficiency bandwidth (greater than 12.5%) makes this doubler design unique. The return loss of the doubler for 1130-mW of input was approximately -10 dB, which is higher than the -30 dB value for 200 mW of input. This is due to the higher bias voltage (-12 V instead of -3.5 V) that degrades the matching at the input side. The measured results for an input power of 20 dBm are in good agreement with the simulated results of Fig. 2.

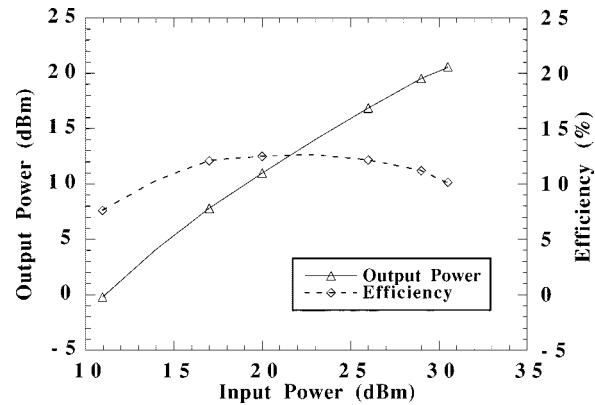


Fig. 7. Measured output power and efficiency versus input power at 74 GHz.

IV. CONCLUSIONS

We have designed, fabricated, and tested a monolithic FGC GaAs doubler based on four varactor Schottky diodes. The doubler demonstrated an efficiency of 12.5%, a minimum 3 dB bandwidth of 12.5%, and a return loss of -15 dB for an input power of 20 dBm, which is in good agreement with simulated results. In addition, an output power of 115 mW was achieved at 74 GHz for an input power of 1130 mW. To the best of our knowledge, this is the highest level of output power and broadest bandwidth achieved at the same time, reported for a monolithic/planar W-band doubler. Further improvement of the efficiency is possible by reducing the parasitics of the diode. The monolithic fabrication technique adopted here is compatible with commercial GaAs MMIC foundry processes, leading to ease of manufacture, low cost, reliability, and integration with existing GaAs products.

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