An Optimized 25.5–76.5 GHz PHEMT-Based Coplanar Frequency Tripler

Y. Campos-Roca, L. Verweyen, M. Fernández-Barciela, E. Sánchez, M. C. Currás-Francos, W. Bronner, A. Hülsmann, and M. Schlechtweg

***Abstract*—This letter presents an optimized single-stage MMIC tripler with W-band output frequency (76.5 GHz). The circuit is based on an 0.15 μm gate-length AlGaAs/InGaAs/GaAs PHEMT. By using a class AB transistor bias point and carefully selecting its input and output terminations, a high conversion gain of −4.3 dB for an 8.5 dBm input signal and a saturated output power of 7 dBm have been obtained. To our knowledge, these results represent the best performance reported up to date for an active frequency tripler with W-band output frequency.**

***Index Terms*—Millimeter wave generation, millimeter wave integrated circuits, MMIC's, MODFET's.**

I. Introduction

THERE is an increasing need of signal sources operating at W-band frequencies (for instance, for 77 GHz automotive radar systems). Signal generation can be achieved by using either directly a W-band oscillator or a lower frequency source followed by a multiplier. The second approach has the advantage of allowing the use of a superior technology for the oscillator in terms of stability and phase noise, so that W-band transmitters with improved overall performance can be realized.

When using that approach, different possibilities are feasible, both in respect of the active device acting as a multiplier and the multiplication order. W-band monolithic doublers based on varactors have been presented in [1]. In general, transistors are preferred to diodes because of their better conversion gain. Even-order PHEMT-based multipliers with W-band output frequencies have already been demonstrated, like, for instance, the ones described in [2].

Another possibility is to use a tripler with W-band output frequency. In general, this type of circuits is based on varactors [3]. To our knowledge, only one transistor-based W-band tripler has been reported up to date [4].

In this letter, we present a 25.5–76.5 GHz PHEMT-based tripler demonstrating the best conversion gain reported up to date at W-band. This superior performance has been achieved by 1) optimizing the active device bias point, and 2) using optimum terminations for all relevant harmonics.

In Section II, we present the theoretical justification of the chosen bias point. Section III describes the tripler design. Performance measurements are presented in Section IV. Finally, the main conclusions of this work are summarized in Section V.

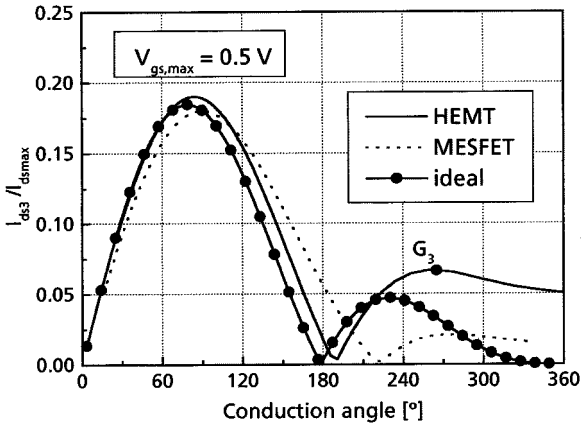

Fig. 1. Normalized Fourier coefficients of the output current waveform as a function of the conduction angle.

II. Theoretical Analysis

The classical theory about transistor frequency multiplication is based on an ideal device, assuming that this is represented by a linear transfer characteristic in its operational active region. By using this simplified model, the Fourier coefficients of the output current waveform, clipped in the pinchoff region, are computed as a function of the conduction angle and normalized with respect to the peak current [5].

A more realistic approach should take into account the active device transfer characteristic nonlinearities. We have selected two well-known large signal models for representing that characteristic: the Statz-Pucel one [6] for MESFET's, and the IAFHEMT one [7] for HEMT's. Fig. 1 shows the calculated normalized output current corresponding to the third harmonic $(I_{ds3}/I_{ds\,\max})$ in three cases: HEMT device, MESFET device, and ideal (linear) device. A peak gate-source voltage $(V_{gs,\max})$ of 0.5 V, in the proximity of the onset of gate current conduction, has been considered for the calculation.

As can be seen in the figure, the three considered devices show a similar performance around the current value absolute maximum. However, this situation is not useful for practical purposes, since the corresponding conduction angle $(80°)$ requires

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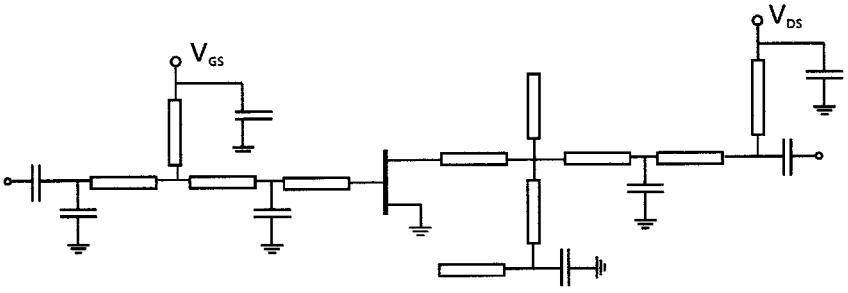

Fig. 2. Schematic circuit diagram of the 25.5–76.5 GHz single-ended frequency tripler.

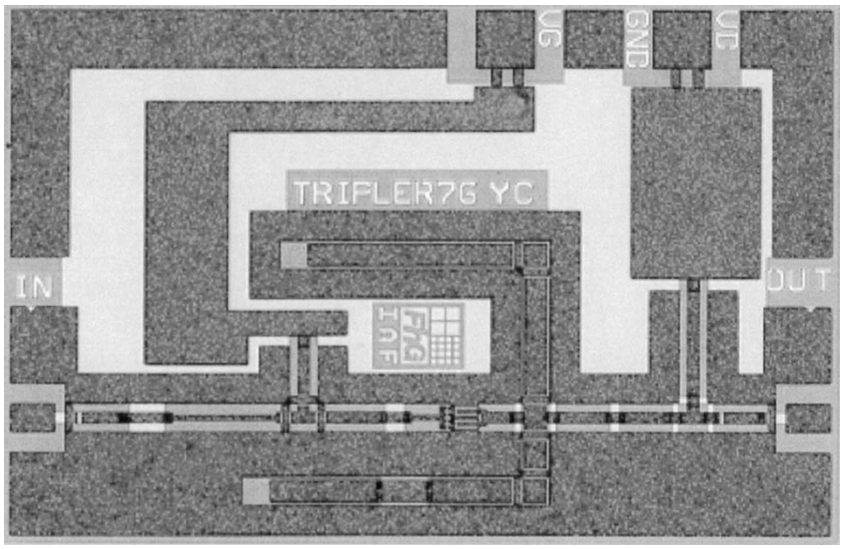

Fig. 3. Chip photograph of the 25.5–76.5 GHz tripler. The chip size is 1×1.5 mm^2.

a high negative gate voltage bias point, which can be problematic in terms of device reliability. Furthermore, it leads to a poor conversion gain.

However, it is interesting to consider the situation around the second local maximum (point G_3 in Fig. 1). Two conclusions can be drawn: a) the ideal theory is no longer valid to predict the performance of real FET's at this bias condition, and b) the HEMT exhibits a clear superiority with respect to the MESFET in class AB. Whereas the latter (due to a transfer characteristic close to a square-law in a wide gate voltage range) generates very low third harmonic power at this bias condition, the HEMT provides relatively high third harmonic output power. Additionally, it can be demonstrated that, for the HEMT, this situation allows to achieve optimum conversion gain. We have verified that these conclusions are general by considering different parameter sets corresponding to different PHEMT processes.

In the literature, different operating classes have been reported for MESFET-based triplers, like bias points close to pinchoff condition [8] (also used for HEMT-based triplers in [9]), overdriven class A condition [10] (also used with HEMT's in [4]), or symmetrical voltage clipping [10].

The key point of this analysis is that it demonstrates a different and efficient way to generate third harmonic power by using a HEMT. To our knowledge, a respective analysis has not been published before.

III. MMIC Design

Following the previous analysis, a 25.5–76.5 GHz MMIC tripler was designed and manufactured at Fraunhofer IAF. The active device is a double δ-doped AlGaAs/InGaAs/GaAs PHEMT, with 0.15 μm gate length and 4×45 μm gate width. A table-based large-signal FET model [11] was used for circuit performance simulation.

The design was focused on selecting the optimum input and output terminations to be presented to the device at all relevant harmonic frequencies. The output third harmonic load and the input fundamental termination should provide conjugate matching under large-signal operational conditions. The other main terminating impedances (for the second and third harmonics at the input, and for the fundamental and second harmonic at the output) should be purely reactive to avoid losses, with an specific phase value in order to enhance the power at the desired harmonic; furthermore, the use of reactive terminations for the undesired harmonics also guarantees the spectral purity of the output signal. Due to the complexity of synthesizing so many terminations, an optimum compromise solution has been used.

Because of the specific requirements of the application the tripler has been designed for, this circuit will be followed by a 76 GHz amplifier. Taking this into account, and in order

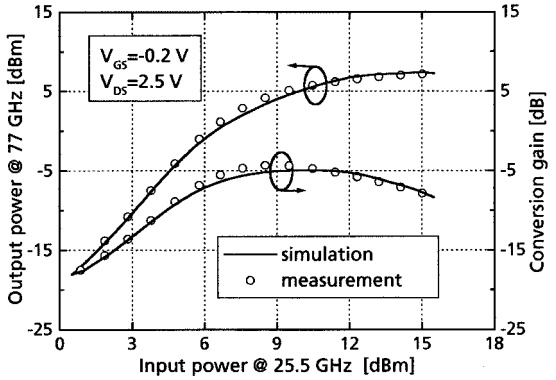

Fig. 4. Output power and conversion gain of the 25.5–76.5 GHz single-stage tripler as a function of the input power.

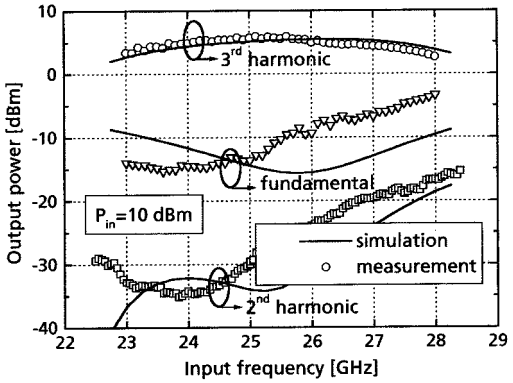

Fig. 5. Output power of the 25.5–76.5 GHz single-stage tripler as a function of the input frequency for an input power of 10 dBm.

to avoid unnecessary filtering elements, the tripler has been designed considering the matching characteristics of the available Fraunhofer IAF 76 GHz cascode amplifiers. These act as bandpass filters, providing high suppression at the fundamental (25.5 GHz) and the fourth harmonic (102 GHz) frequencies, although still providing some gain at the second harmonic (51 GHz) frequency.

The tripler schematic diagram is shown in Fig. 2. In the design of odd-order multipliers, it is not possible to impose a short-circuit for the fundamental at the output by means of a quarter-wave open-circuited stub (which is a common approach in the design of doublers), since this stub would also eliminate the desired harmonic. Therefore, a shorter stub with a shunt capacitor has been used, thus eliminating the fundamental while the second minimum of its transmission coefficient lies far away from the third harmonic frequency.

A photograph of the fabricated MMIC is shown in Fig. 3. The use of a single-ended topology and coplanar waveguide technology results in a small chip size of 1×1.5 mm^2.

IV. Measured MMIC Performance

The circuit has been tested on-wafer using a measurement set-up consisting on a synthesizer, a power amplifier, a directional coupler and a scalar power sensor on the input side, and harmonic mixers (not necessary in the case of the fundamental) and a spectrum analyzer, at the output. Fig. 4 shows the simulated and measured output power, and the conversion gain as a function of the input power. The tripler achieves a high conversion gain of -4.3 dB for an input signal of 8.5 dBm at 25.5 GHz and a saturated output power of 7 dBm. As can be seen, a very good agreement between predicted and measured results is obtained. Fig. 5 shows the measured and simulated output power as a function of the input frequency. The third harmonic output power varies less than 3 dB for an input frequency between 23 and 28 GHz; that is, a 3 dB bandwidth of 20% is achieved. The measured spurious suppressions are 16, 32, and 13 dBc for the fundamental, and the second and fourth harmonics, respectively.

V. Conclusion

A novel analysis has shown that class AB operated HEMT's are suitable for tripler implementation. Following this conclusion and using optimum harmonic terminations, a 25.5–76.5 GHz tripler has been designed and fabricated. The circuit demonstrated a high conversion gain of -4.3 dB for an input power of 8.5 dBm, and a saturated output power of 7 dBm. To our knowledge, these results represent the best performance reported up to date for a W-band active frequency tripler.

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