Fully Monolithically Integrated Feedback Voltage Controlled Oscillator

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***Abstract*—A fully monolithically integrated voltage controlled oscillator (VCO) using feedback technique is presented here. The circuit provides oscillation within the frequency range of 6.3–7.0 GHz. The corresponding tunable relative bandwidth is 10%. The feedback topology proves to provide a good linearity of the oscillation frequency dependence versus tuning voltage. The maximal deviation of the frequency behavior from its linear fit is $\Delta f = 39$ MHz. It is shown in following that the feedback technique can be used for broadband VCO design.**

***Index Terms*—Broadband VCO, Clapp-VCO, full monolithic integration, MMIC-VCO, voltage controlled oscillator (VCO).**

I. Introduction

MICROWAVE monolithic integrated circuits (MMIC's) recently find use in a variety of sensor, automotive, and other applications and systems. One-chip systems make essential the design of compact, high-performance, wide-band fully integrated voltage controlled oscillators (VCO's) based on (P)HEMT (pseudomorphic high electron-mobility transistor) epitaxial structure.

Two basic topologies can be used for oscillator design using a transistor as active element: Negative differential resistance technique (reflection type oscillators) and the feedback arrangement [1], [2]. The reflection type oscillator circuit topology realising negative differential resistance at one of the ports of the active element has often been used for RF-VCO circuit design (e.g,. [3], [4]). It is different for tunable oscillators based on the feedback topology. Whereas this arrangement has often been employed for designs with oscillation frequency below 1 GHz, there is only one recently reported realization for microwave frequencies [5].

This letter describes the design and measured performance of a VCO realization that is based on the modified Clapp-oscillator topology. The circuit is fully monolithically integrated and was fabricated using the commercially available PHEMT-process PH25 of UMS. The PHEMT gate-length featured by this process is 0.25 μm.

The circuit provides oscillations within the frequency range $f_{\rm osc} = 6.3$–7.0 GHz, which leads to a relative bandwidth of $\Delta f/f_0 = 10\%$. This is a good value for a fully monolithically integrated VCO realization. Furthermore, the VCO realizations based on the feedback technique prove to provide a very good linearity of the oscillation frequency tuning.

Manuscript received March 7, 2000; revised April 24, 2000. This work was supported by the Adam Opel AG, Rüsselsheim.

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Publisher Item Identifier S 1051-8207(00)05945-6.

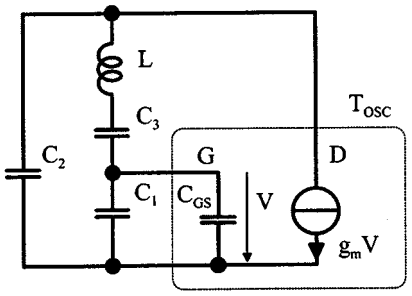

Fig. 1. Principal schematic of considered Clapp-oscillator with transistor presented by its equivalent circuit.

II. Circuit Design

A. Clapp Voltage-Controlled Oscillator

The basic schematic chosen for the oscillator design is a derivation of the Clapp-oscillator [6], [7]. The simplified schematic of this oscillator configuration is shown in Fig. 1. The active transistor $T_{\rm OSC}$ is represented here by its most simple equivalent circuit consisting of the gate-source capacitance $C_{\rm gs}$ and the transconductance g_m.

Analysing this circuit by simple means of small-signal technique, the frequency of oscillation can be calculated to

$$f_{\rm osc} = \frac{1}{2\pi}\sqrt{\frac{1}{LC_3}\left[1 + C_3\left(\frac{1}{C_2} + \frac{1}{C_1 + C_{\rm gs}}\right)\right]}. \quad (1)$$

Choosing $C_1 \gg C_{\rm gs}$ leads to the advantage that technological variations of $C_{\rm gs}$ do not cause change of the oscillation frequency. Further, (1) simplifies to

$$f_{\rm osc} = \frac{1}{2\pi}\sqrt{\frac{1}{L}\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right)}. \quad (2)$$

In order to apply this circuit configuration to a VCO design the capacitance elements have to be made variable. It can be shown using (2) that by altering the values of all the three capacitors **simultaneously** the maximal frequency tuning range can be achieve.

Based on these considerations, a fully monolithically integrated MMIC-VCO was designed. This circuit was developed with the aim to achieve the maximal available bandwidth of oscillation.

B. MMIC VCO Design

The principial schematic of the oscillator designed is shown in Fig. 2. The DC-network is also included into this figure.

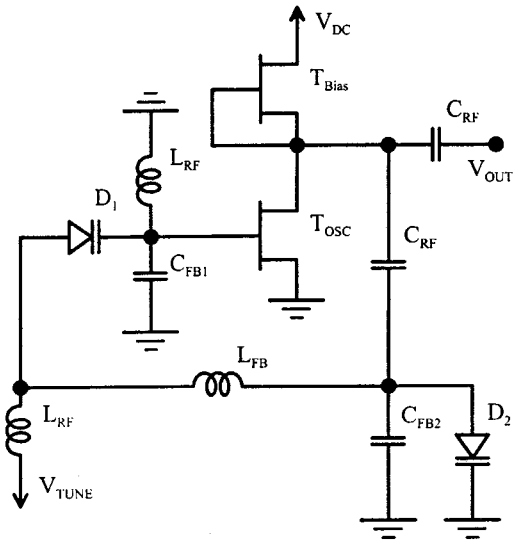

Fig. 2. Principial schematic of the feedback VCO including the biasing network.

An 8×75 μm PHEMT in common-source configuration acts as the amplifying element within the circuit. In order to reduce the required chip-area the active biasing concept was chosen to provide drain-source voltage to the active transistor. For this reason another 8×75 μm PHEMT is used, whose gate and source are connected to each other. Capacitors $C_{\rm RF}$ and spiral inductors $L_{\rm RF}$ separate further RF- and DC-paths within the circuitry.

The output power of the amplifier is fed back to its input via a passive network that fulfil the conditions for steady-state oscillations. The Π-network consists of integrated capacitors, and a transmission line as feedback inductance ($L_{\rm FB}$ in Fig. 2).

The frequency tuning is achieved by employing the integrated planar 10×75 μm diodes. These diodes are not optimized for maximal capacitance change and, thus, their junction capacitance varies with the applied tuning voltage within the range of $C \approx 0.5$–1.6 pF. The low capacitance change ratio of $C_{\rm max}/C_{\rm min} \approx 3$ is a common value for such MMIC diodes.

It should be mentioned that this is the small-signal value. The higher the RF-voltage at the diodes, the lower the effective capacitance change ratio and, hence, the maximal bandwidth of oscillations. In order to reduce the RF-voltage at a single diode four series-parallel connected devices are used as D_1 and D_2. The calculations using a simulation tool, e.g., MDS of HP-EESOF, confirmed this effect.

Of course, it is possible to achieve frequency tuning using only the diode D_1 as proposed by Clapp [7]. But as described in the previous subsection, the bandwidth of oscillations can significantly be increased by simultaneous altering of all the three capacitive elements. These considerations could be confirmed by the large-signal simulations performed. But due to difficulties in connection with the tuning voltage supply to the gate of the active PHEMT, only the capacitors C_3 and C_2 in Fig. 1 were considered to be variable by employing the diodes D_1 and D_2 (Fig. 2). This made the entire DC-biasing network very simple.

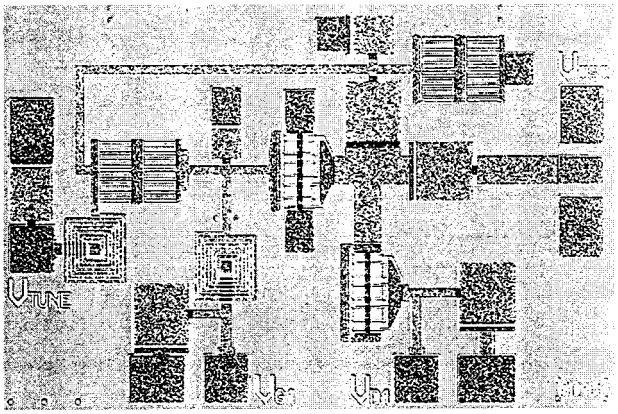

Fig. 3. Microphotograph of the oscillator realized. Dimensions: 1.5×1.0 mm^2.

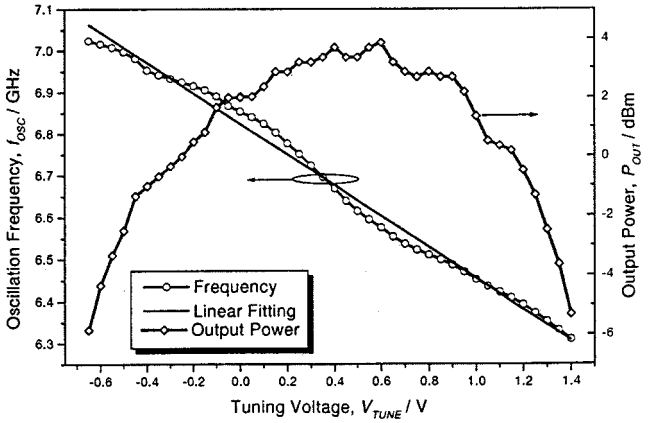

Fig. 4. Oscillation frequency, its linear approximation, and the output power as functions of applied tuning voltage.

The design was implemented utilising the microstrip technology. The circuit is compact and the chip-area used by the VCO amounts to the value of 1.5×1.0 mm^2. Fig. 3 presents a photograph of the oscillator.

III. Measured Performance

On-wafer measurements of the circuit were performed employing the spectrum analyzer HP8565E. Beforehand, the cable losses were determined in order to correct the measured power level. The gate-source bias voltage was set to zero, whereas the value of the drain-source bias supply was $V_{\rm ds} = 3.5$ V at the DC-pads. Approximately half of this is applied to the amplifying PHEMT. The DC current consumed by the circuitry amounts to the value of $I_{\rm dc} = 120$ mA.

Fig. 4 shows the measured curves of the oscillation frequency and the output power of the VCO versus applied tuning voltage. The output power of the circuit varies within the range of $P_{\rm out} = -5.8$–$+3.9$ dBm. The variation of the delivered power versus tuning voltage is rather high. It is mainly due to the mismatch at the oscillator output and can be improved by including a buffer amplifier into the design.

The VCO provides oscillations within the frequency range of $f_{\rm osc} = 6.31$–7.02 GHz. The relative bandwidth of oscillations

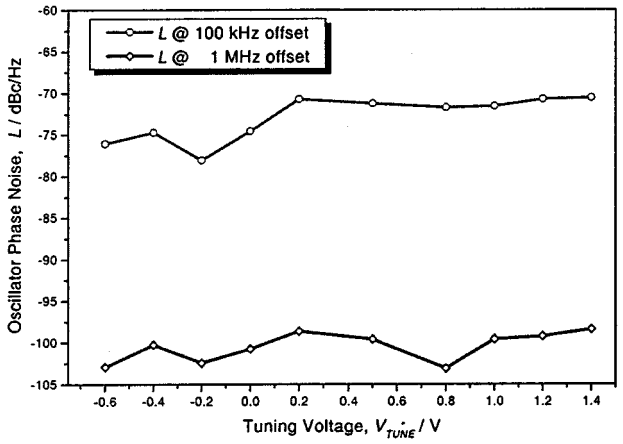

Fig. 5. Oscillator phase noise for different tuning voltages.

exhibits a value of $\Delta f/f_0 = 10.7\%$, which is a good result for a fully monolithically integrated VCO realization with diode frequency tuning.

The frequency dependence on tuning voltage shows a fairly linear behavior. The linearity error is calculated as the difference between the measured frequency tuning and its linear approximation that is also displayed in Fig. 4. This value varies in the range of $\Delta f = \pm 38$ MHz, which leads to a maximal absolute linearity error of $\Delta f/f_{\rm osc} = 0.55\%$. The average frequency tuning sensitivity of the oscillator is $S_{\rm TUNE} = 370$ MHz/V. The good linearity of the circuit is advantageous for many applications such as phase-locked loop systems.

The oscillator phase noise was also measured by using the HP8565E spectrum analyzer with the HP85671A Phase Noise Measurement Utility. The behavior of the phase noise versus tuning voltage is shown in Fig. 5 for offset frequencies of 100 kHz and 1 MHz carrier. The phase noise varies slightly with the tuning voltage and is always below -70 dBc/Hz at 100 kHz offset from carrier.

IV. Conclusions

This letter describes the design and the measured performance of a fully monolithically integrated voltage controlled oscillator with integrated diode frequency tuning. The circuits oscillates in the frequency range of 6.3–7.0 GHz. It bases on feedback topology and is one of the first implementations of this oscillator design techniques for microwave frequencies. This design solution proves to exhibit a good linear behavior of the oscillation frequency variation versus tuning voltage with maximal linearity error of $\Delta f/f_{\rm osc} = 0.55\%$. Further, the designed circuit demonstrates a fairly good value of phase noise (below -70 dBc/Hz @100 kHz offset from carrier). This performance make this kind of VCO's interesting for a variety of applications.

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