Low-Voltage C-Band SiBJT Single-Chip Receiver MMIC Based on Si 3-D MMIC Technology

Kenjiro Nishikawa, *Member, IEEE*, Kenji Kamogawa, *Member, IEEE*, Tadao Nakagawa, and Masayoshi Tanaka, *Member, IEEE*

***Abstract*—This letter demonstrates a C-band Si BJT MMIC single-chip receiver based on the masterslice 3-D MMIC technology. The fabricated receiver MMIC on a chip of 1.8 mm by 1.8 mm integrates a low-noise amplifier, an image-rejection mixer, and an IF hybrid associated with an IF amplifier. The fabricated components on the chip are designed by using reactive matching method due to both broadband and low-voltage operation. The receiver MMIC achieves a conversion gain of 13.5 dB, a noise figure of 5.2 dB, and an image rejection ratio of 30.6 dB at 5.2 GHz. This receiver also has a flat gain characteristic in the C-band. The power consumption of this MMIC is 115 mW with 2 V collector supply voltage.**

***Index Terms*—MMIC low-voltage, Si bipolar, single-chip receiver, three-dimensional.**

I. Introduction

MANY C-band wireless applications have been proposed and developed. Wireless LAN applications operate in the 5.2 GHz- and 5.8 GHz-bands. Intelligent transportation systems (ITS), use the 5.8 GHz-band to offer Electric toll collection system (ETC) and vehicle-to-roadside communication both which are radio frequency identification (RFID) services. Obviously, the commercial market for C-band applications will increase rapidly. These applications require cost-effective and highly integrated MMIC's with low power, as do mobile communication systems in the under 2-GHz band. In addition, broadband MMIC's that covered the C-band are very effective in reducing the equipment cost. These applications are well supported by our Si 3-D MMIC technology [1]–[3] and key components, such as a low-noise amplifier and a mixer have been reported [3]. This technology realizes Si MMIC's that offer high-frequency, broadband, and low-voltage operation using a production-level Si device process. In addition, Si MMIC's that cover these application bands offer lower cost. This letter demonstrates a C-band single-chip receiver MMIC that is designed by utilizing the reactive matching method. The receiver is fabricated on a single 1.8 mm $\times$ 1.8 mm chip. The fabrication process is 0.25-μm Si bipolar technology with low resistive Si wafers (ρ = 20 Ωcm) [4].

Manuscript received March 9, 2000; revised April 27, 2000.

K. Nishikawa, K. Kamogawa, and T. Nakagawa are with the NTT Network Innovation Laboratories, Yokosuka-shi 239-0487, Japan.

M. Tanaka is with the NTT Science and Core Technology Laboratory Group, Yokosuka-shi 239-0487, Japan.

Publisher Item Identifier S 1051-8207(00)06000-1.

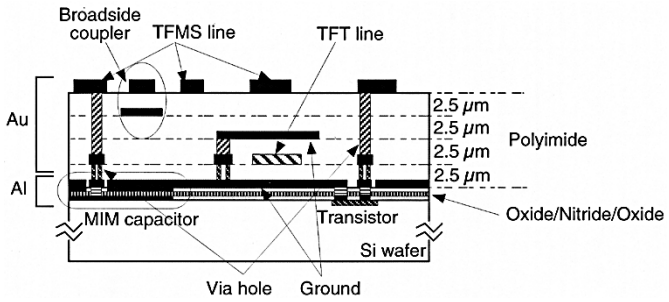

Fig. 1. Basic structure of Si 3-D MMIC.

II. Si 3-D MMIC Technology Using BJT

Fig. 1 shows the basic structure of the Si 3-D MMIC [1]. BJT's, resistors, lower (first-level) aluminum metals of MIM capacitor, passivation layer, and second-level aluminum metals are formed on a Si wafer using a standard Si IC process. The three-dimensional (3-D) passive structure, consisting of four layers of 2.5-μm thick polyimide film and 1-μm-thick gold metal (top-level metal is 2-μm thick), is formed on the top level metal using a Si IC process. This structure isolates the microwave passive circuits from the low resistivity Si wafer, resulting in low-loss passive circuits. The loss of the thin-film microstrip (TFMS) line using 10-μm thick substrate is 75% less than that of the coplanar waveguide with 20-μm width signal line on a Si wafer. The Si bipolar transistor used was fabricated using the 0.25-μm Si bipolar technology [4] of NTT Electronics Corp. and the emitter size of its unit transistor is 0.3 μm $\times$ 8 μm. The measured f_T and $f_{\max}$ are 40 GHz and 62 GHz at 1 V collector bias voltage, respectively. Some of key parameters of the transistor are r_b = 41 Ω, h_{FE} = 44. The MIM capacitor is composed of an 800 Å thick silicon-nitride film to obtain high capacitance (0.74 fF/μm^2), and more efficient space utilization.

III. Circuit Design and Performance

The block diagram of the Si 3-D MMIC single-chip receiver is shown in Fig. 2(a). The receiver incorporates a 2-stage low-noise amplifier (LNA), an image rejection mixer. IF amplifiers and an IF 90° hybrid are followed by the image-rejection mixer. Fig. 2(b) shows a photograph of the fabricated receiver. The chip size is just 1.8 mm $\times$ 1.8 mm and holds eight 0.3 μm $\times$ 8 μm emitter BJT's (amplifiers) and sixteen 0.3 μm $\times$ 8 μm emitter BJT's (mixers). The supply voltages are 2 V for RF amplification, 0.3 V for the mixer, and 1 V for the IF amplifier.

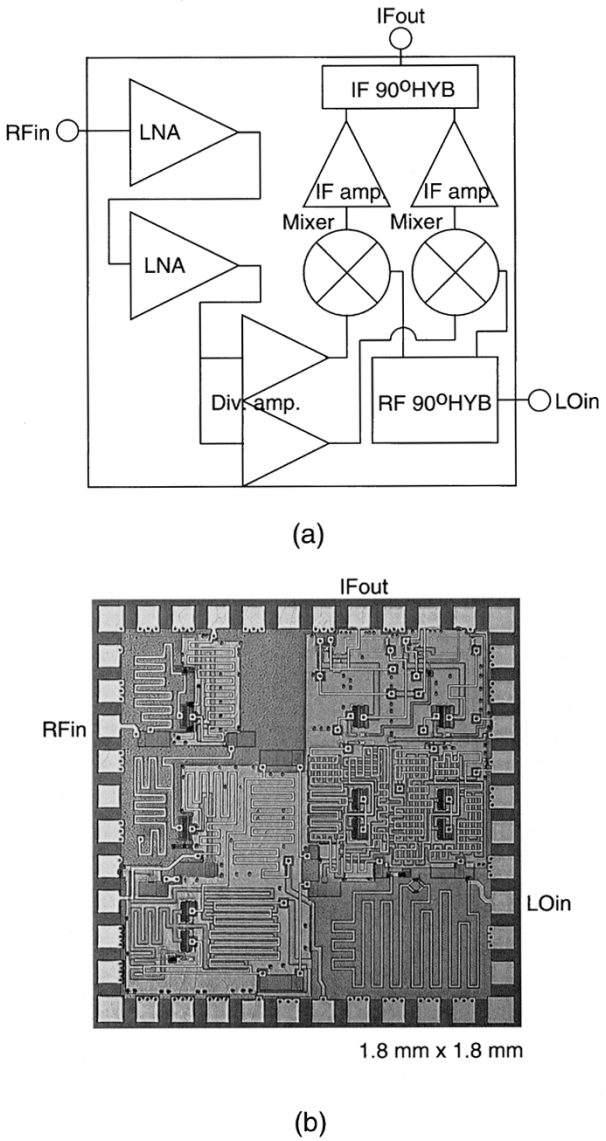

Fig. 2. Fabricated Si 3-D MMIC single-chip receiver. (a) Block diagram of receiver. (b) Photograph.

The LNA is a 2-stage common-emitter BJT configuration amplifier with reactive matching circuits consisting of TFMS lines. The input matching circuit consists of TFMS lines with a 10-μm thick polyimide substrate to obtain a low loss circuit. The inter-stage and output matching circuit consist of a TFMS line and a thin-film triplate (TFT) line that are stacked above and below the middle layer ground plane to achieve compactness. The matching circuits were designed to achieve broadband operation. The LNA achieves 17.5 dB $\pm$1.5 dB gain and less than 4 dB noise figure over the range of 4.5 GHz to 6 GHz. The base bias is supplied through a resistor to obtain the same value as the collector bias. The supplied collector and base biases and the power consumption are 2 V and 64 mW, respectively.

The image rejection mixer consists of an active power divider with common-emitter BJT's, a broadside coupler, collector LO injection mixers, and associated IF amplifiers with IF-band 90 °combiner. The broadside coupler consists of two $\lambda_g/8$ wavelength broadside couplers and the upper line is connected to the lower line. This configuration results in a coupler with good balance performance. For the mixer, RF and LO ports are designed by stacking reactive matching circuits above and below the middle ground plane to achieve compactness. The IF circuits were designed using the RC matching configuration.

TABLE I
PERFORMANCE COMPARISON OF RECENTLY REPORTED C-BAND SINGLE-CHIP MMIC RECEIVERS AND TRANSCEIVERS (RECEIVE PATH)

Reference	Device technology	Operating frequency (GHz)	NF (dB)	Conversion gain (dB)	Supply voltage (V)
This work	0.25 μm Si bipolar	4.5 - 6	5.25 ± 0.5	13 ± 0.5	< 2
NEC [5]	0.4 μm BiCMOS	5 - 5.4	7	18	2.6 - 5
Rockwell [6]	0.35 μm CMOS	5.2	8	5	-3.3
Nortel [7]	IBM SiGe HBT	5	5.9	19	3.5
OKI [8]	0.5 μm GaAs MESFET	5.8	4.1	20.4	3
Mitsubishi [9]	1 μm GaAs MESFET	5.8	5.6	13.5	3
Hittite [10]	0.6 μm GaAs MESFET	5.7 - 7.5	5.5 ± 0.5	25 ± 1	3

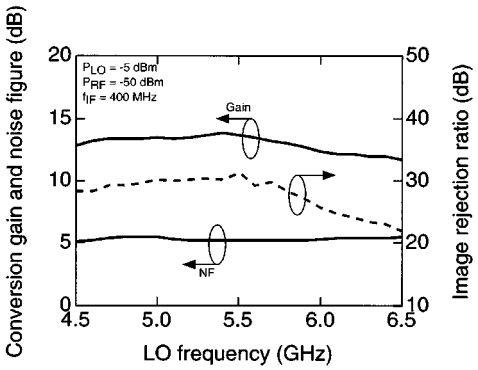

Fig. 3. Measured performance of receiver.

The measured performance of the fabricated receiver MMIC is shown in Fig. 3. The conversion gain and the image rejection ratio are 13 dB $\pm$ 0.5 dB and more than 25 dB over the range of 4.5 GHz to 6 GHz, respectively. The noise figure is less than 5.3 dB. The input third-order intercept point is -24 dBm. The local input power, the RF input power, and the IF frequency are -5 dBm, -50 dBm, and 400 MHz, respectively. The power consumption of the MMIC is 115.5 mW. Table I compares the performance of recently reported single-chip MMIC receivers and transceivers (receive path). The fabricated receiver MMIC achieves the lowest noise figure and the widest operating range of the Si MMIC's reported to data. Its performance is competitive with that of GaAs MESFET MMIC's, despite its 2 V operation.

These results indicate that the Si 3-D MMIC technology can offer cost-effective single-chip solutions to C-band applications.

IV. CONCLUSIONS

This letter demonstrated a C-band single-chip receiver 3-D MMIC. Its performance approaches that of GaAs MESFET

MMIC's despite its 2 V operation. This demonstration indicates that the Si 3-D MMIC technology has high potential in reducing the cost of C-band MMIC's.

REFERENCES

[1] I. Toyoda, K. Nishikawa, T. Tokumitsu, K. Kamogawa, C. Yamaguchi, M. Hirano, and M. Aikawa, "Three-dimensional masterslice MMIC on si substrate," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2524–2529, Dec. 1997.

[2] K. Nishikawa, I. Toyoda, K. Kamogawa, T. Tokumitsu, C. Yamaguchi, and M. Hirano, "K-band si MMIC amplifier and mixer using three-dimensional masterslice MMIC technology," *ISSCC Dig. Tech. Papers*, pp. 252–253, Feb. 1998.

[3] K. Nishikawa, K. Kamogawa, I. Toyoda, T. Tokumitsu, and M. Tanaka, "C-band si 3-D MMIC transceiver for wireless applications," *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, pp. 35–38, June 1999.

[4] M. Ugajin, J. Kodate, Y. Kobayashi, S. Konaka, and T. Sakai, "Very-high f_T and $f_{\max}$ silicon bipolar transistors using ultra-high-performance super self-aligned process technology for low-energy and ultra-high-speed LSI's," *IEDM'95 Tech. Dig.*, pp. 735–738, Dec. 1995.

[5] M. Madihian, T. Drenski, L. Desclos, H. Yoshida, H. Hirabayashi, and T. Yamazaki, "A 5-GHz-band multifunctional BiCMOS transceiver chip for GMSK modulation wireless systems," *IEEE J. Solid-State Circuits*, vol. 34, pp. 25–32, Jan. 1999.

[6] K. Runge, D. Pehlke, and B. Schiffer, "On-chip matched 5.2 GHz differential integrated mixer with RF and LO preamplification, fabricated in 0.35 μm CMOS technology," *Electron. Lett.*, vol. 35, pp. 1545–1546, Sept. 1999.

[7] S. Voinigescu, M. Copeland, D. Marchesan, P. Popescu, and M. Maliepaard, "5 GHz SiGe HBT monolithic radio transceiver with tunable filtering," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, June 1999, pp. 131–134.

[8] E. Low, H. Nakamura, H. Fujishiro, and K. Yan, "A plastic package GaAs MESFET 5.8 GHz receiver front-end with on-chip matching for ETC system," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, June 1999, pp. 43–46.

[9] M. Hieda, K. Nakajima, N. Suematsu, E. Taniguchi, Y. Tsukahara, S. Sakamoto, K. Miyawaki, M. Hisada, Y. Iyama, and T. Takagi, "A 6 GHz band transceiver front-end MMIC for ETC" (in in Japanese), in *Proc. IEICE Electronics Society Conf.*, vol. C-2-43.

[10] C. Trantanella, P. Blount, and M. Shifrin, "A GaAs +3 V low noise integrated downconverter for C-band applications," in *IEEE GaAs IC Symp. Dig.*, Nov. 1999, pp. 199–202.