Temperature and Process Insensitive Circuit Design of a Voltage Variable Attenuator IC for Cellular Band Applications

Luciano Boglione and Ray Pavio

***Abstract*—This letter describes circuit design solutions for a 900 MHz voltage variable attenuator (VVA) integrated circuit that aims to achieve straight line attenuation slope versus control voltage as well as process and temperature insensitivity. Power linearity is also taken into account. Measured results will be presented in order to compare the new VVA to the original circuit and to confirm the robustness of the new design.**

***Index Terms*—Attenuators, FET circuits, integrated circuit manufacture, temperature, voltage control, yield optimization.**

I. Introduction

VOLTAGE variable attenuators (VVA's) are important components for today's wireless market and gallium arsenide technology has demonstrated that can provide the high yield necessary for supporting the ever growing demand [1]. Power linearity has always been a major issue [2]–[4]; temperature variations have also been tackled, with either off-chip [5] or on-chip [6] solutions. Devices specifically suited for VVA applications [7] as well as circuit techniques have also been demonstrated [8] for various purposes.

The motivations for this paper stem from the design of a 900 MHz GaAs multifunction upconverter for CDMA handsets [9] that makes use of a VVA to control its gain.

In the constant strive to improve yield and overall performance, a study focused on the VVA has been carried out. The study aims to make the attenuation S_{21} (in dB) over control voltage V_{ctrl} as linear as possible (slope linearity); and to make S_{21} versus V_{ctrl} as independent as possible of the variations due to both process and temperature (attenuation uniformity). These goals are to be achieved without affecting the VVA power handling capability (power linearity).

After outlining some features of the initial VVA, each aspect (slope linearity, attenuation uniformity and power linearity) are addressed and the circuit solution discussed. Measurements carried out over a number of samples and temperatures will be presented.

II. Features of the Original VVA

The VVA embedded in the upconverter consists of three MESFET's arranged as a T-shaped attenuator (Fig. 1). The GaAs devices have a 0.5 μm gate, and their mean pinchoff voltage value is -1.1 V. The VVA does not have a dedicated pad for the control line; off-chip capacitors provide a RF ground to the shunt FET source terminal to which V_{ctrl} is connected. The VVA has been simulated and then tested in a glopped 16 pin open top package on a FR4 board with SMA connectors. The operating frequency is 824–849 MHz and the evaluation is carried out at 836 MHz. The control voltage V_{ctrl} ranges from 0 to 3 V and the attenuation must span down 20 dB or more from its maximum value, -3 dB. These specifications must be met over the operating temperature range -30 °C – $+85$ °C ($+25$ °C typical).

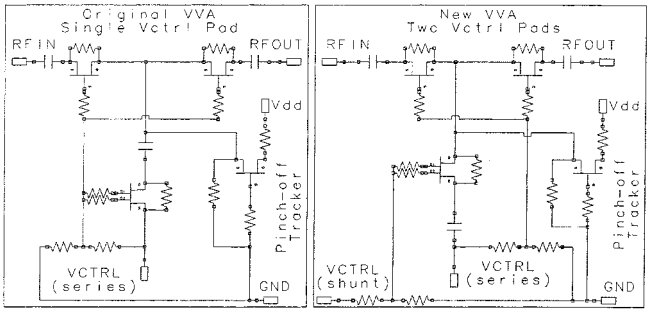

Fig. 1. Variable voltage attenuator: sketch of the original and new design.

A pinchoff tracker has been incorporated into the VVA design. The pinchoff tracker makes the gate to source voltage V_{gs} of the series FET's track the variation in pinchoff voltage over process and temperature; and supplies a constant voltage at the common point between the series FET's. The series FET V_{gs} variation is described by

$$\Delta V_{gs} = \Delta V_g - \Delta V_s = -\Delta V_s = -\Delta V_{po} \qquad (1)$$

since $V_g = V_{ctrl}$ is constant and V_{po} is the pinchoff voltage (without sign) supplied by the pinchoff tracker—here, $V_{po} = +1.1$ V. This tracking system is paramount if a constant attenuation is to be achieved independently of temperature as well as process variations.

The pinchoff tracker of the existing VVA, however, affects only the series FET's since a capacitor is required at the drain of the shunt FET branch as dc block and for resonating out the package bond. V_{ctrl} controls the shunt FET through a voltage divider. This approach does not compensate for the changes in pinchoff voltage of the shunt FET. Consequently, the attenuation set by a V_{gs} value of the shunt FET close to the pinchoff voltage

Manuscript received October 20, 1999; revised May 8, 2000.

L. Boglione is with the Conexant Systems, Inc., Boston Design Center, Chelmsford, MA 01824 USA.

R. Pavio is with the Multi-Function Group, ISBU M/A-COM, Lowell, MA 01853 USA.

Publisher Item Identifier S 1051-8207(00)06506-5.

of the device, is very sensitive to temperature and part to part variations.

III. Improving the VVA

A discussion of the goals to be achieved by the VVA, is now detailed and circuit solutions suggested. The new topology (Fig. 1) is obtained by applying the following considerations.

A. Slope Linearity

Ideally, the VVA attenuation S_{21} is linearly dependent on the control voltage V_{ctrl} at the frequency of interest. Unfortunately, MESFET devices are inherently non-linear and a simple T-shaped VVA cannot fulfill that requirement [10].

The slope linearity is a tradeoff with input and output matches through the devices' periphery. The analysis of the cascade of three linear circuits (linear circuit A followed by a VVA followed by linear circuit B) can show that the overall transmission coefficient S_{21} is equal to

$$S_{21}=\frac{1}{1-S_{11}^{B}S_{22}^{\mathrm{VVA}}}\,S_{21}^{A}\cdot S_{21}^{\mathrm{VVA}}\cdot S_{21}^{B}\,\frac{1}{1-S_{22}^{A}\Gamma_{in}^{\mathrm{VVA}}(S_{11}^{B})} \quad (2)$$

where terms are self-explanatory. Equation (2) guarantees that good power transfer from the input to the output port can be achieved with good output and input matches of the stages A and B preceding and following the VVA respectively, even though the VVA has poor return losses. Furthermore, a match to a characteristic impedance different from 50 Ω can be considered for a VVA embedded in a multifunction chip.

The way the control voltage is applied to the devices also affects the slope of the attenuation. A single voltage divider is too simple an approach for the FET's to change their channel resistance in the correct fashion that guarantees a linear slope in S_{21} versus V_{ctrl}. Two voltage dividers can improve the situation and two separate control voltages would also help out although at the expense of higher complexity for the end user.

Based on these considerations, the device gate-to-source voltages are driven by two control voltages through two independent voltage dividers. Peripheries have been redesigned in order to improve the slope linearity while keeping the return losses to practical values in a 50 Ω environment.

B. Attenuation Uniformity

The 900 MHz upconverter has been prone to showing variations of S_{21} over process and temperature for control voltage values in the region of the pinchoff voltage of the shunt FET. The reason has already been identified in the lack of a pinchoff tracker for the shunt FET. It has also been shown in (1) that the compensation of the changes in V_{po} requires $\Delta V_{gs}=-\Delta V_{po}$. This result suggests that the control voltage is to drive the gate terminal and the pinchoff tracker the source terminal of the shunt FET. This is easily achieved by moving the top capacitor from above to below the shunt FET. This allows the pinchoff tracker to set the voltage of the source terminal of the shunt FET and at the same time to preserve the double use of the pin connected to the shunt FET as both dc control line and RF ground. However, the shunt FET gate potential must decrease from a value around $V_S = V_{po}$ to 0 to make the attenuation smaller and smaller as

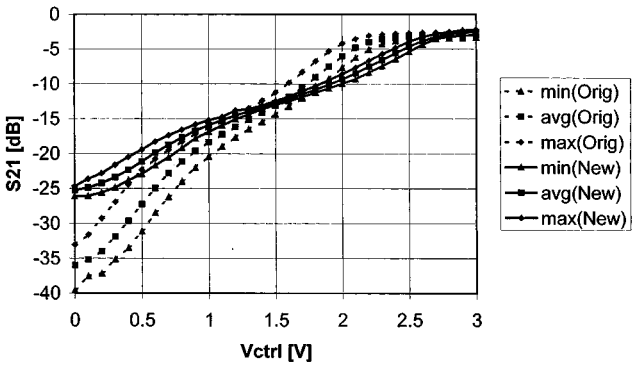

Fig. 2. Spread of the tested insertion loss versus V_{ctrl} for the original (dashed) and the new (solid) VVA at 836 MHz. Both temperature ($-30\,^{\circ}$C, $+25\,^{\circ}$C, $+85\,^{\circ}$C) and process variations are used to find minimum, average, and maximum values at each VVA setting.

V_{ctrl} is increased. At the same time the series FET gate potential must increase to V_{po}. The circuit solution is to have two control voltages, V_{ctrl} (series) and V_{ctrl}(shunt), driving respectively series and shunt FET's; chip area is preserved because it does not require a second pinchoff tracker. The series and shunt voltages are not independent:

$$V_{ctrl}^{shunt}=3-V_{ctrl}^{series} \quad (3)$$

where V_{ctrl}(series) ranges between 0 and 3 V. A simple sign changer op-amp [11] or more sophisticated digital solutions can drive the control voltages. On-chip solutions may be feasible at the expense of the size of the chip.

C. Power Linearity

The VVA has a double gate shunt FET in order to provide good power linearity, in particular when the shunt FET V_{gs} is around its pinchoff value [9], [12]. Based on company expertise, an original circuit topology has been used in order to reduce changes in V_{gs} of the shunt FET when the input power into the VVA is large and to guarantee good linearity.

IV. Results

A new VVA has been designed according to the above guidelines and fabricated on the same wafer along with the original VVA. Results as a function of the control voltage for the new VVA assume $V_{ctrl} = V_{ctrl}$ (series) as independent variable; V_{ctrl}(shunt) is then set according to (3).

About 14 samples of each type of VVA have been packaged and tested on the same board in order to correlate the measured data. Scattering parameters have been measured, the input power being set at -25 dBm at the probes. Adjacent channel power ratio (ACPR) measurement according to IS95 recommendations has also been carried out. Some of the spread for small values of V_{ctrl} can be attributed to higher measurement uncertainties due to the small power coming out of the VVA under test.

Fig. 2 compares the spread of S_{21} versus V_{ctrl} over temperature ($T = -30$ C, $+25$ C, $+85$ C) as well as over part to part variations for the original and the new VVA. The improvements in slope linearity and attenuation uniformity are remarkable.

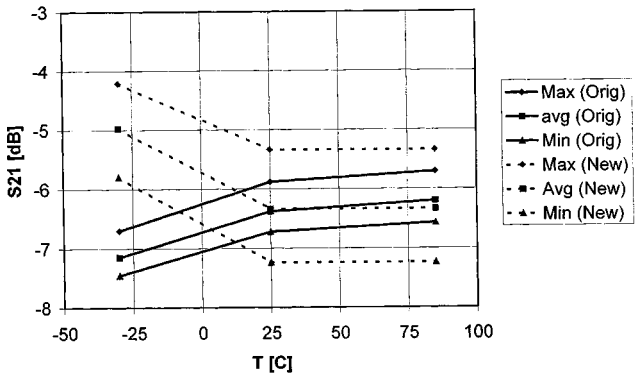

Fig. 3. Spread over part variations of the tested attenuation versus temperature for original and new VVA. V_{ctrl} settings are 2.3 V and 2 V for the new and original VVA, respectively.

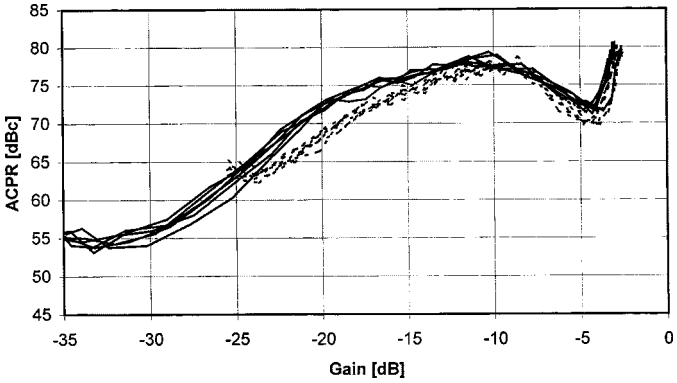

Fig. 4. Comparison of the tested ACPR versus gain performance between six original VVA's (solid lines) and six new VVA's (dotted lines) at 836 MHz, $+25\,^{\circ}C$, $P_{in} = -10$ dBm.

The slopes of S_{21} versus V_{ctrl} of the original and new VVA's are different, leading to the maximum attenuation of the new VVA of about 25 dB. In the original design, the 20 dB minimum attenuation range is achieved by designing a steeper slope to cope with variations in the attenuation over both part to part and temperature variations. The new topology allows the designer to set the upper knee at higher V_{ctrl} setting as well as to contain the spread over temperature and process for a given control voltage. The net result is that the new attenuation range is about 10 dB smaller than the range of the original VVA leading to a more efficient use of the control voltage.

Fig. 3 shows the spread of the attenuation over measured part variations versus temperature at a fixed V_{ctrl} setting. These voltages 1) are in the proximity of the attenuation knee; and 2) deliver similar attenuation values at 25 °C. The compensation over temperature achieved by the new design is highlighted as well as the tighter spread over process variations; the spread over parts at each temperature point is reduced by about 50%.

The return losses of the original and new VVA's have also been tested and found comparable.

ACPR measurements have also been carried out. Fig. 4 shows a comparison of the ACPR performance between original and new VVA's at 836 MHz and 25 °C for a constant input power ($P_{in} = -10$ dBm). A small input power setting (e.g., -25 dBm) can make the measurement at high attenuation levels unreliable since the output power delivered by the VVA can approach the noise floor of the CDMA receiver. ACPR is plotted versus gain in order to ensure a fair comparison between original and new VVA: the result demonstrates that new and original circuit topologies provide comparable power handling capability.

V. Conclusion

A discussion on the elements that provide a remarkable improvement in the VVA performance over temperature and process variations has been carried out and a circuit solution demonstrated. Measured results confirm the robustness of the new circuit design and show that the power handling capability of the new VVA is preserved.

Acknowledgment

The first author acknowledges one of the reviewers for the suggestions regarding Fig. 3, and Dr. S. Beaussart for reviewing the manuscript.

References

[1] W. Mickanin, "Don't rule out the MESFET!," *Microw. J.*, pp. 112–120, July 1998.
[2] M. J. Schindler and A. Morris, "DC-40 GHz and 20-40 GHz MMIC SPDT switches," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 2985–2601, December 1987.
[3] R. Gutmann and N. Jain, "Comments on GaAs MESFET baseband-to-microwave passive switches," *IEEE Trans. Microwave Theory Tech.*, vol. 37, no. 7, pp. 1154–1155, July 1989.
[4] R. H. Caverly, "Distortion in broad-band Gallium arsenide MESFET control and switch circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 713–717, April 1991.
[5] L. Raffaelli and R. Goldwasser, "Temperature compensation for microwave GaAs FET amplifiers," *Microw. J.*, pp. 315–321, May 1986.
[6] G. Lizama, T. Andrade, and R. Benton, "1–6 GHz GaAs MMIC linear attenuator with integral drivers," in *IEEE 1987 Microwave and Millimeter-Wave Monolithic Circuits Symp.*, Las Vegas, NV, June 8–9, 1987, pp. 105–107.
[7] K. Miyatsuji, H. Ishida, T. Fukui, and D. Ueda, "A technique for improving the distortion of GaAs variable attenuator IC using squeezed-gate FET structure," in *IEEE 1996 Microwave and Millimeter-Wave Monolithic Circuits Symp.*, San Francisco, CA, June 17–18, 1996, pp. 43–46.
[8] H. Kondoh, "DC-50GHz MMIC variable attenuator with a 30 dB dynamic range," in *19th Eur. Microwave Conf. Proc.*, New York, May 25–27, 1988, pp. 499–502.
[9] K. Harrington, B. McNamara, M. Murphy, B. Khabbaz, and M. Hafizi, *et al.*, "Highly integrated MMIC upconverters/drivers for cellular and PCS CDMA handsets," in *1999 Radio Frequency Integrated Circuits (RFIC) Symp.*, Anaheim, CA, June 13–15, 1999, pp. 77–80.
[10] B. Maoz, "A novel, linear voltage variable MMIC attenuator," *IEEE Trans. Microwave Theory Tech.*, vol. 38, no. 11, pp. 1675–1683, November 1990.
[11] W. G. Jung, *IC Op-Amp Cookbook*, Second ed. Carmel, IN: Howard W. Sams, 1983.
[12] H. J. Sun, W. Wu, and J. Evans, "A 2–20 GHz GaAs MESFET variable attenuator using a single positive external drive voltage," in *19th Eur. Microwave Conf. Proc.*, Long Beach, CA, June 12–13, 1989, pp. 1270–1275.