Effects on the Linearity in Ka Band of Single or Double-Recessed PHEMT's

C. Gaquiere, *Student Member, IEEE*, F. Bue, P. Delemotte, Y. Crosnier, B. Carnez, and D. Pons, *Associate Member, IEEE*

***Abstract*—The effects of the gate recess topologies on the linearity performance of PHEMT's have been investigated in Ka band. The letter highlights the reasons why, at a given output power level, the double recessed device exhibits a very large improvement of its intermodulation performance as its drain source bias voltage is increased whereas its linearity is inferior to that of the single recessed device at low drain source bias voltage. The effect of the load impedance on the linearity behavior has also been investigated. At a given output power the load impedance contour of the double recess structure is shown to exhibit a much more large variation of the intermodulation ratio than that of the single recess structure.**

I. INTRODUCTION

WITH the development of local multipoint distribution (LMDS), there is now considerable activity in Ka band. Communication services, such as television, video on demand, distance learning, Internet access, etc., are at the basis of this one. This tremendous need has created considerable interest in the development of Ka band power amplifiers. On the other hand, modulation schemes such as quadrature phase-shift keying (QPSK) or quadrature amplitude modulation (QAM), used to handle high capacity data transfer, require from these amplifiers to be very linear [1]. In this context, a good understanding of the technological parameters that determine device distortion characteristics is necessary. The linearity behavior, in terms of third- and fifth-order intermodulation (IM3, IM5) and intermodulation ratio (IMR), needs to be correlated with the main device process parameters. This letter deals with this problem and provides a comparison between two PHEMT's, which essentially differ by their gate recesses. One has a single recess, the other has a double recess. Both of them exhibit the same drain-source spacing, gate length and total gate width.

II. DEVICES DESCRIPTION

The devices have been achieved on usual PHEMT epilayers, on GaAs substrate, with delta doping, and exhibit a drain current density at open channel ($V_{gs} = 0.5$ V) around 600 mA/mm. The 0.25 μm gate is centered in the drain-source spacing and in the recess. Same total gate widths of 2×75 μm have been used for this study. The operating frequency is 26 GHz. For the device with a single recess the distance between the gate edge and the edge of the cap layer, usually named "ungated recess," is of about 30 nm. The double recess device has the same narrow gate recess as the previous device, but with in addition a second wide recess of 1000 nm centered on the gate.

TABLE I
MAIN DC AND SMALL SIGNAL CHARACTERISTICS OF THE SINGLE AND DOUBLE RECESS

	I_{Dmax} (mA/mn) Vgs= 0.5V	Vp(V) (V_{DS} = 3 V)	Vbr(V) diode	Vbr (V) open channel	F_T(GHz) (3V ; -0,2V)	F_{max}(GHz) (3V ; -0,2V)
Single recess	580	-0,65	7	4	68	133
Double recess	560	-0,6	9,5	8	55	140

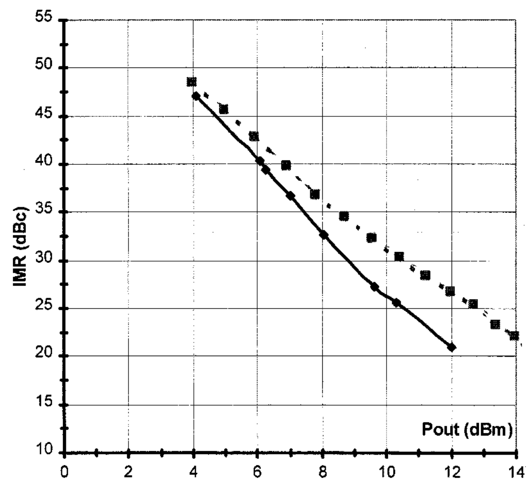

Fig. 1. Intermodulation ratio versus output power level at $V_{ds} = 3$ V and $V_{gs} = -0,2$ V (dashed lines) single recess (solid line) double recess.

III. RESULTS

As it can be noted in Table I, the maximum drain current densities (at $V_{gs} = 0.5$ V) and pinch off voltages of the two devices have the same values. As it could be expected, the breakdown voltages, defined at 1 mA/mm gate current either in diode (with source floating) or in transistor configurations, are better in the case of the double recess. Indeed, at same bias conditions, this structure allows the electric field to spread and hence results in a diminution of its maximum at the drain side corner of the gate compared to a single recess [2]. Small signal microwave performance of the two devices are nearly similar at the same bias conditions (Table I). Large signal measurements have been first

Manuscript received March 9, 2000; revised May 24, 2000.

C. Gaquiere, F. Bue, P. Delemotte, and Y. Crosnier are with the Institut d'Electronique et de Microélectronique du Nord, UMR-CNRS 8520, Département Hyperfréquences et Semiconducteurs Cité Scientifique, 59652 Villeneuve d'Ascq Cedex, France.

B. Carnez and D. Pons are with the United Monolithic Semiconductors, 91401 Orsay Cedex, France.

Publisher Item Identifier S 1051-8207(00)06508-9.

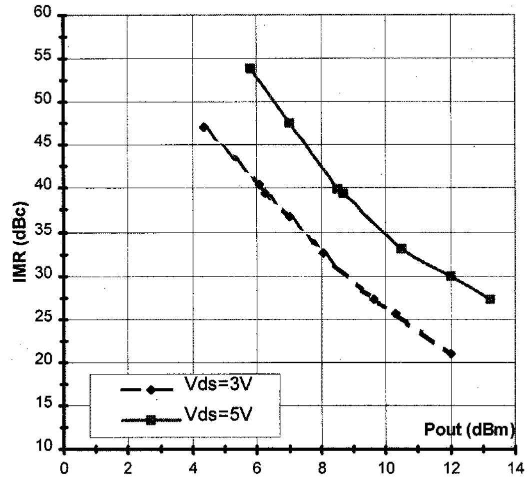

Fig. 2. Intermodulation ratio versus output power level for the double recessed device at two V_{ds} for $V_{gs} = -0,\ 2$ V (dashed lines) $V_{ds} = 3$ V; (solid line) $V_{ds} = 5$ V

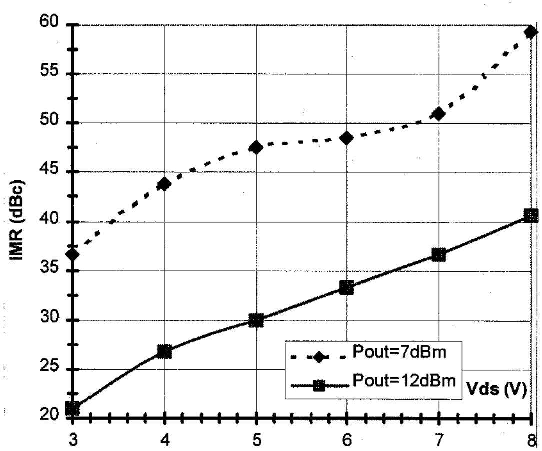

Fig. 3. Intermodulation ratio of the double recess device versus V_{DS} for two constants output power levels at $V_{gs} = -0,\ 2$ V. (Dashed lines) Pout $= 7$ dBm; (solid line) Pout $= 12$ dBm.

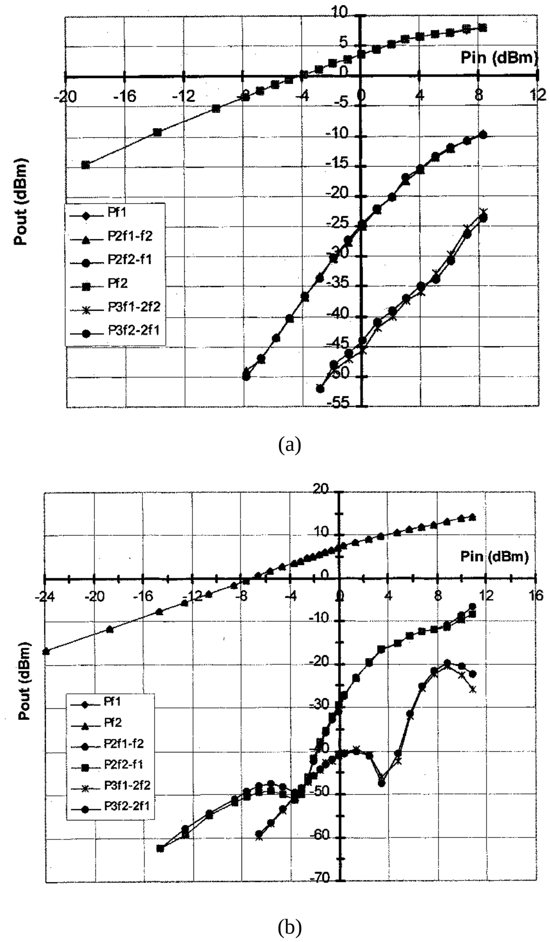

Fig. 4. Output power response third and fifth IM products versus total input power level for two tone excitation (a) single recessed device, at $V_{ds} = 3$ V; $V_{gs} = -0,\ 2$ V; (b) double recessed device, at $V_{ds} = 5$ V; $V_{gs} = -0,\ 2$ V.

performed on the two devices, at 26 GHz, under single-tone and two-tone conditions, at the same class A biasing: $V_{ds} = 3$ V, $V_{gs} = -0.2$ V.

Under single-tone conditions, results obtained with the single recess device are substantially superior to that of the double recess device at any output power level and power added efficiency. Such a difference is probably due to the fact that surface states are affecting the double recess structure and prevent the RF drain current swing from being as large as expected from dc characteristics. Pulsed I (V) measurements (width 300 ns, period 10 μs), with a class A quiescent bias point, have been achieved and have highlighted this assumption. Indeed, no drain current variation was noted with the single recess whereas a decrease of about 10% was observed for the double recess between dc and pulsed conditions. This behavior explains the lower power density of the double recess compared to the single recess (340 mW/mm, 420 mW/mm). Owing to its high breakdown voltage the double recess device has been then tested at a higher drain source voltage $V_{ds} = 5$ V, for the same $V_{gs} = -0.2$ V. Under these conditions, its maximum power density increased from 340 mW/mm to 550 mW/mm. Indeed, higher breakdown voltage allows higher operating drain voltage, which translates to a higher power density as long as the power gain is sustained.

Then the same devices have been studied with a two-tone measurement system at 26 GHz with a 1 MHz tone spacing [3]. First of all, a decrease of the maximum output power has been observed between the single-tone and the two-tone modes. This behavior has been already noted at lower frequencies [4]. It is related to the instantaneous envelope variation which arises from the beat-like two-tone signal. Indeed, for a same total input power level, the gate forward conduction clipping occurs earlier in the two-tone mode than in the single-tone mode. Fig. 1 shows the measured IMR versus the output level at the same bias conditions, $V_{ds} = 3$ V; $V_{gs} = -0.2$ V, for the two devices. In these conditions, the single recess is better than the double recess, as found previously for the single-tone excitation, whatever the parameter under consideration (power level, linearity, power added efficiency). Hence, at low drain source voltage (3 V), in class A, the single recess device is better suited than the double recess device to linear applications. A similar study has been performed for the double recess but at $V_{ds} = 5$ V and $V_{gs} = -0.2$ V. An important improvement of the device

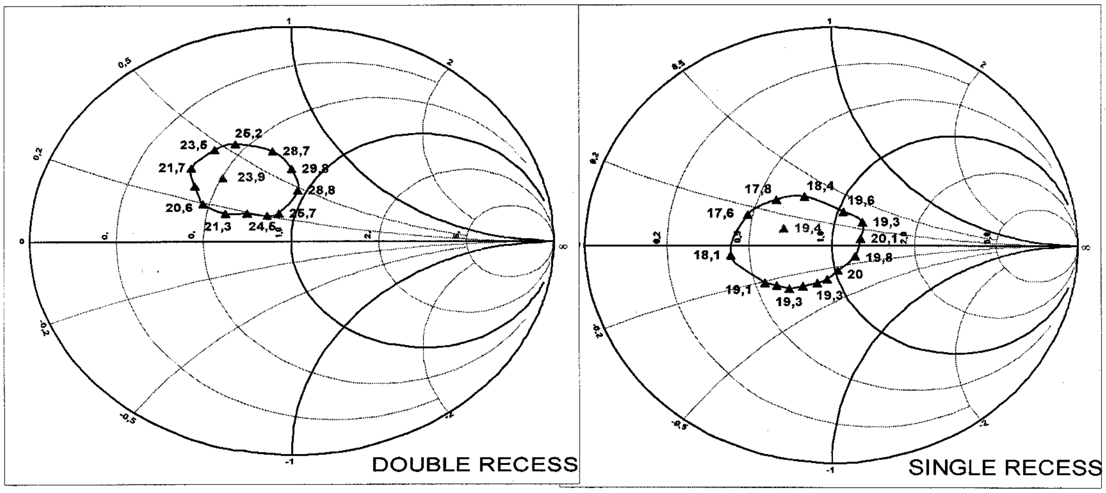

Fig. 5. Constant output power contour and the corresponding IMR for a constant input power level single recess ($V_{ds} = 3$ V; $V_{gs} = -0, 2$ V). Double recess ($V_{ds} = 5$ V; $V_{gs} = -0, 2$ V).

linearity has resulted (Fig. 2) from this drain-source voltage increase. On average the IMR is 10 dBc better for $V_{ds} = 5$ V than for $V_{ds} = 3$ V, at the same V_{gs}. In order to confirm this trend the two-tone measurement has been achieved from $V_{ds} = 3$ to 7 V with a step of 1 V at $V_{gs} = -0.2$ V. As shown in Fig. 3, where are reported the IMR measurements for two output power levels, the increase of V_{ds} is continuously beneficial to linearity, and, therefore, the previous results are clearly confirmed. Nevertheless $V_{ds} = 5$ V seems to be relatively optimum to ensure simultaneously good performance in terms of IMR, output power, power added efficiency (24 dBc, 400 mW/mm, 22% at 1 mA/mm average gate current).

An other interesting aspect lies in the various rate of rise exhibited by the third order intermodulation product IM3 versus the input signal level. First, at $V_{ds} = 3$ V, the IM3 product varies classically with a slope which remains approximately around 3, up to a relatively high power level, both for the single and the double recess devices [Fig. 4(a)]. But the situation is quite different for the double recessed device when its V_{ds} bias voltage is increased to 5 V [Fig. 4(b)]. A slope of 3 is only obtained at low power level, and as the input power level rises the slope falls down, which corresponds to a quasi cancellation of the IM3 product. Then, the slope reincreases strongly before the occurrence of saturation. Such a phenomenon is typical of devices which have high drain-source voltage handling capabilities. In particular, it is currently observed in LDMOS [5]. It is usually interpreted as a contribution of higher odd order intermodulation products to the IM3 response. Indeed, at medium power level the overall distortion at IM3 frequency is the vector sum of distortions generated by the third and fifth nonlinearities. When the two contributions are comparable in magnitude and nearly out of phase (180°) cancellation between these distortions can occur. It seems to be typically the case in Fig. 4(b) due to the fact that the IM5 response becomes equal to the IM3 response exactly at the point where this one is falling down.

A last aspect, but not the least, deals with the effect of the output load on the device linearity. The constant output power contours obtained in the Smith chart at a constant injected power level exhibit strong differences between the single recess and the double recess devices. This is clearly shown in the example of Fig. 5. Indeed, at the same output power level of 14.5 dBm, an IMR variation of 9 dB for the double recess and only 2.5 dB for the single recess can be obtained with the load optimization. In order to know whether this improvement is due to the double recess structure or to the high drain source bias voltage, the same study has been carried out for the double recess with $V_{ds} = 3$ V. In this case, the IMR variation is strongly reduced and joins approximately that of the single recess.

IV. Conclusion

In this letter, the influence of recess topologies on PHEMT's linearity performance has been studied in Ka band. It clearly shows that a single recess is preferable as long as the drain-source bias voltage is limited to a few volts. But, the double recess, owing to its particular topology, can handle higher operating bias voltage and it results from this ability both a substantial increase of the output power and a beneficial contribution of the IM5 product to the IM3 performance. Hence, the power level and more especially the linearity behavior are strongly improved. These considerations will guide Ka band communications systems designers in their choice of device topologies.

References

[1] R. Gupta and D. J. Allstot, "Fully monolithic CMOS RF power amplifiers: Recent advances," *IEEE Commun. Mag.*, pp. 94–97, April 1999.

[2] C. Gaquière, B. Bonte, D. Théron, Y. Crosnier, P. Arsène-Henri, and T. Pacou, "Breakdown analysis of an asymmetrical double recessed power MESFET's," *IEEE Trans. Electron Devices*, vol. 42, pp. 209–214, February 1995.

[3] F. Bué, C. Gaquière, Y. Crosnier, B. Carnez, and P. Quentin, "A 26–40 GHz on wafer intermodulation measurement system," in *Eur. Microwave Conf.*, Münich, Germany, October 4–7, 1999, pp. 452–454.

[4] R. Hajji, F. Beauregard, and F. M. Ghannouchi, "Multitone power and intermodulation load-pull characterization of microwave transistors suitable for linear SSPA's design," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1093–1099, July 1997.

[5] C. Blair, "LDMOS devices provide high power for digital PCS," *Appl. Microw. Wireless*, pp. 84–88, October 1998.