High Efficiency Monolithic Gallium Nitride Distributed Amplifier

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***Abstract*—The first gallium-nitride monolithic distributed amplifier is demonstrated. A nonuniform design allows the removal of the drain line dummy load with a concomitant increase in efficiency. An optimized nonuniform design shows a 10% increase in efficiency over an optimized uniform design having the dummy termination.**

***Index Terms*—Circuit optimization, distributed amplifiers, MMIC.**

I. Introduction

Distributed amplifiers (DAs) offer broadband operation because of the synthetic lumped-element approximate transmission line realized by the active device capacitances and intervening inductances. While DAs were realized long ago [1], virtually all contemporary implementations using field effect or bipolar device technologies utilize a uniform DA topology, where each of the series inductances is the same (for example, [2], [3]). All of these uniform DA implementations require a drain (using FET nomenclature) line dummy termination (to absorb the backward "traveling wave"), which consumes significant power and hence reduces the power added efficiency (PAE). While ideal gain elements and perfect transmission lines allow the elimination of the backward wave at all frequencies [1], such a solution is not transferable to a practical situation due to device and transmission line nonidealities. While the concept of varying parameters in a distributed amplifier using optimization has been introduced [4], the issue of power dissipation in the drain line dummy load remained. To address the efficiency issue, we present a nonuniform distributed amplifier (NDA) concept where the drain line dummy load is removed and the broadband design is achieved using nonlinear optimization with an appropriate cost function and constraint set. We show through comparison with an optimized uniform DA that the bandwidth is not compromised with an NDA implementation and that significant improvements in efficiency can be achieved.

GaAs-related III–V compounds have reached a level of maturity as to allow the realization of monolithic microwave integrated circuits (MMICs), and much work related to DAs has involved MMIC realization [2], [4]. However, both the low thermal conductivity of GaAs substrates and the bandgap limit the achievable power densities relative to gallium-nitride (GaN) compounds, grown on sapphire and silicon carbide substrates. For example, a CW power density of 6.9 W/mm of gate periphery has been achieved with a GaN high electron mobility transistor (HEMT) on a SiC substrate [5]. This high power density potential has driven recent interest in GaN, and a hybrid amplifier with flip-chip bonded GaN HEMTs on an AlN substrate has been demonstrated [6]. We report here the first GaN MMIC, an implementation of a NDA.

Manuscript received February 14, 2000; revised May 19, 2000. This work was supported by the Office of Naval Research under Contracts N00014-98-1-0371 and N00014-96-1-1223.

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Publisher Item Identifier S 1051-8207(00)07177-4.

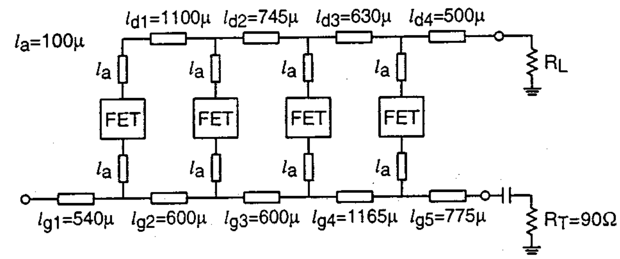

Fig. 1. Circuit schematic for the fabricated NDA.

II. Amplifier Design, Fabrication, and Characterization

Piezoelectrically-doped $Al_{0.3}Ga_{0.7}N/GaN$ HEMTs [7], grown using organo-metallic vapor phase epitaxy (OMVPE) on a sapphire substrate, and having 0.32 μm gate lengths and 0.5 mm gate peripheries (from the same wafer used to build the amplifier), were used in the amplifier. A Curtice nonlinear model [8] was developed using a 125 μm periphery device, and this was used in the design. Using nonlinear optimization in the Agilent EEsof Libra package with a reasonable initial solution (for example, a uniform design or a lumped element approximation for a stepped impedance design [1]), the design of Fig. 1 was achieved. The inductances are realized using 80 Ω coplanar waveguide (CPW) lines (12 μm center conductor width, 32 μm gap between center conductor and ground plane) throughout, with the lengths indicated in Fig. 1. Note the absence of the drain line dummy load and the varying CPW line lengths between each of the four gain stages, indicative of the nonuniform inductance values.

The GaN MMIC process, which has been developed for amplifier fabrication, consists of seven mask levels:

1) ECR mesa isolation dry etch;
2) Ti/Al/Ti/Au ohmic contact formation;

(a)

(b)

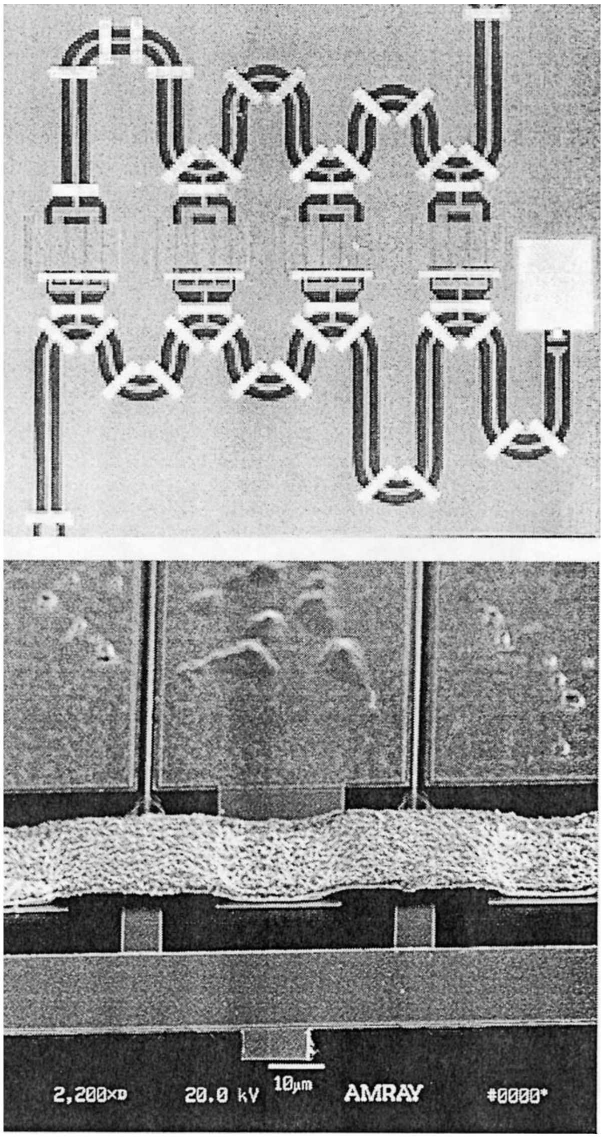

Fig. 2. (a) Monolithic GaN nonuniform distributed amplifier photograph and (b) SEM micrograph of the source airbridges.

3) 3500 Å thick Ni/Au T-gates;
4) interconnect metal (1 μm thick Au);
5) NiCr resistors (90 Ω/□);
6) selectively deposited SiO_2 MIM capacitors (120 pF/mm^2);
7) 2.5 μm thick plated air bridges.

The use of CPW for the passive transmission line inductive elements obviates the need for ground via access.

A photograph of the fabricated 1.72×1.55 mm^2 four-stage amplifier is shown in Fig. 2(a), with the air-bridged sources showing two of the gate fingers in Fig. 2(b). The measured and simulated small signal S-parameters for this NDA in a 50 Ω system (biased at $V_D = 10$ V, $V_G = -4.5$ V for peak g_m) are shown in Fig. 3. The $|S_{21}|$ is slightly over-estimated because the measurement-based CPW line model used was for 3 μm Au (2.40×10^{-4} dB/μm) and this amplifier used 5000 Å thick metal. In a large signal measurement, 1.25 W peak output power, 25% peak PAE, and a gain of 7 dB were obtained at 3 GHz in

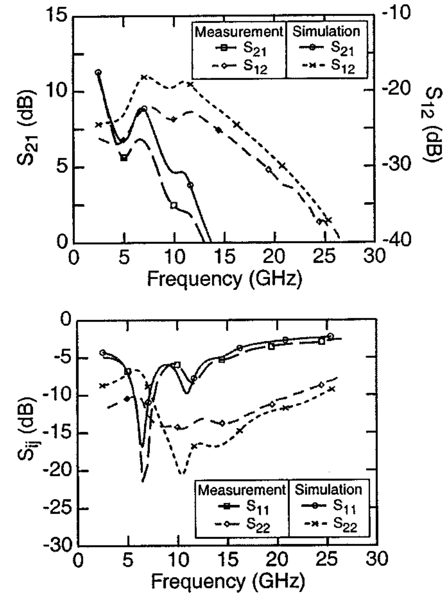

Fig. 3. Comparison of measured and simulated S-parameters.

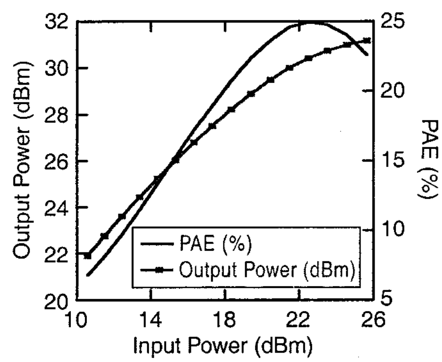

Fig. 4. Measured power spectrum and PAE at 3 GHz with 25 Ω source and load impedances in Class A operation.

Class A operation ($V_D = 15$ V, $V_G = -3.6$ V); the power spectrum is shown in Fig. 4.

III. Additional Simulation

Additional Class A NDA designs were investigated to evaluate their PAE relative to that achievable from uniform DAs. With the drain line dummy load removed from the conventional DA, circuit parameters, i.e., gate and drain inductive line lengths, were iteratively adjusted. The optimization goals were specified so that the four-stage DA has a flat gain and high efficiency throughout the band (1–12 GHz).

The procedure began with an initial solution based on a uniform lumped element design. With the drain line dummy load removed, line lengths were iteratively perturbed using Libra. The genetic algorithm (GA) optimizer was used initially, followed by a gradient search optimizer. The optimization goals were specified as maximizing the efficiency over 9–12 GHz, because it is generally difficult to achieve good efficiency nearer to the cut-off frequency.

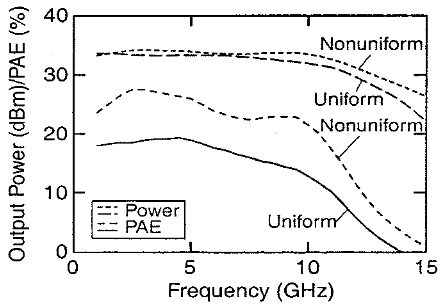

Fig. 5. Efficiency and output power of optimized NDA compared with an optimized uniform DA with $l_{g1} = 310$ μm, $l_{g2} = 670$ μm, $l_{g3} = 579$ μm, $l_{g4} = 608$ μm, $l_{g5} = 670$ μm, $l_{d1} = 925$ μm, $l_{d2} = 1309$ μm, $l_{d3} = 945$ μm, $l_{d4} = 316$ μm, and $R_T = 12$ Ω.

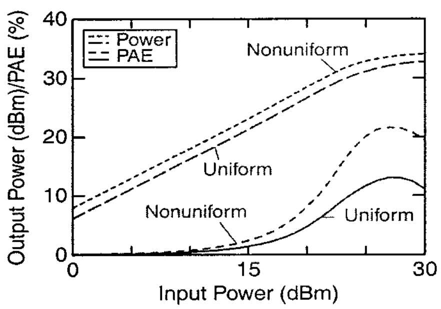

Fig. 6. Power saturation of optimized NDA and optimized uniform DA at 10 GHz.

Each gain cell (with a measurement-based model) has a 0.25 μm gate length and a periphery of 4×125 μm, and is biased for Class A operation ($V_D = 15$ V, $V_G = -2.6$ V). The simulation results for output power and PAE for this amplifier are given in Fig. 5. The optimization-based design results in a 10% increase in PAE across the entire band relative to that achievable with a uniform DA whose performance has also been optimized. In the case of the uniform DA, an initial design based on 50 Ω lines using C_{GS} and C_{DS} was optimized with two variables, the intervening gate and drain lines representing the series inductances. In the range of 1–10 GHz and with 50 Ω source and load impedances, the optimized NDA performance shows a PAE of over 20%, output power up to 2.22 W (1.11 W/mm), and an associated gain of over 9.3 dB. The power spectrum at 10 GHz, again with comparison to the uniform design, is shown in Fig. 6.

The drain lines are longer than the gate lines to compensate for $C_{GS} > C_{DS}$, i.e, to achieve approximate phase matching between the gate and drain lines. Our simulation studies have shown that phase matching is more important than impedance matching in achieving large gain-bandwidth products.

IV. Conclusion

This realization of the first monolithic GaN distributed amplifier was driven by the need for wide bandgap semiconductors on high thermal conductivity substrates in order to achieve high power densities. Both the nonuniform design and the fabrication approach presented can be applied for higher-power designs having high efficiency.

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