

A Broadband and Miniaturized V-Band PHEMT Frequency Doubler

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Abstract—In this letter, we present the design and measured performances of a Ka-band frequency doubler fabricated using 0.15 μm GaAs pseudomorphic HEMT transistors and the three-dimensional (3-D) MMIC technology. Thank to the use of an improved 180° rat-race hybrid, the frequency doubler exhibits high spectral purity over a large bandwidth. Isolation better than 30 dB is achieved on a frequency range from 31.7–36 GHz and fundamental frequency rejection better than 35 dB is achieved between 31.5 GHz and 37.5 GHz. Conversion loss measured at 32.5 GHz is 8.5 dB for an input power of 14 dBm. Both the broadband spectral purity and the small size of 1 mm² make it suitable for the realization of high-quality and widely tunable V-band frequency sources. For the future developments of millimeter-wave wireless communication systems, it offers good perspectives toward the fabrication of single-chip V-band transceiver including the frequency source.

Index Terms—Broadband, circuit theory and design, frequency doubler, rat-race hybrid, 3-D MMIC technology.

I. INTRODUCTION

THE INCREASING demand for millimeter-wave wireless communication systems has raised the necessity to realize high-quality millimeter-wave sources. For this purpose, frequency multipliers are attractive devices. Indeed, the use of frequency multipliers to create millimeter-wave sources provides more reliability and accuracy than the direct design of millimeter-wave frequency oscillators. Moreover, the phase noise generated by an oscillator composed of a microwave source and a frequency doubler is lower than the one of an equivalent millimeter-wave oscillator.

Several developments of millimeter-wave oscillators using frequency doublers have been successfully reported [1], [2]. The main disadvantage of this technique is the tight frequency band over which the doubler can be used for proper fundamental rejection and isolation, therefore strongly limiting the frequency tuning capability of the source. In addition, large size sets against the integration of millimeter-wave circuits on the same chip resulting in a multi-chip and high-cost configuration [1].

In order to overcome the previous disadvantages, the purpose of this work is to develop a V-band frequency doubler that exhibits high spectral purity over a large bandwidth. For this design, the balanced configuration was considered because it provides efficient rejection of the fundamental and the odd-harmonic frequencies. Improvement of the bandwidth can be efficiently achieved by the use of a novel 180° rat-race hybrid pre-

viously reported [3]. Moreover, in order to overcome the conventional drawback of balanced doubler which is large area, the doubler is design using the three-dimensional (3-D) MMIC technology that provides high integration level [4].

II. MMIC DESIGN AND FABRICATION

The circuit schematic of the proposed frequency doubler is shown in Fig. 1. It consists in two identical, 0.15 μm long, 200 μm (50 $\mu\text{m} \times 4$) wide, Panasonic pseudomorphic HEMT's [5] feed by signals of identical power and with a phase difference of 180°. These devices have an intrinsic transit frequency f_T of 70 GHz and a maximum oscillation frequency f_{\max} of 120 GHz. In order to decrease the power consumption and help the generation of the second harmonic, the transistors are biased in the pinchoff region.

The Ka-band input matching and the V-band output matching of the transistors are designed to provide broadband operation. In order to reduce the chip size, the transistors biasing circuits are integral part of the input and output matching networks. Unconditional stable operation is achieved by the addition to the input matching network of a RC parallel network shorted to the ground.

The main improvement of the design consists in the use of a novel topology for the 180° rat-race hybrid [3]. This new topology simply consists in a conventional the rat-race hybrid with a quarter-wavelength short transmission line added at one of the output. At the center frequency f_0 for which the rat-race hybrid is designed, we can show that this additional short transmission line do not modify the 180° phase difference requirement between the two outputs [3]. However, near the center frequency, it introduces a phase contribution inversely proportional to its characteristic impedance. This phase contribution enables to tune the phase signal variation between the input port and output port where the short is positioned to the one between the input port and the other output port. Therefore, a convenient choice of the characteristic impedance of the short transmission line enables to improve the phase balance characteristic of the hybrid over a large bandwidth. The improved rat-race hybrid previously measured exhibits a return loss of 1.6 dB. The measured power dividing balance error and phase balance error are, respectively, less than 1.1 dB and 2° from 28.8 to 39.4 GHz.

Fig. 2 shows the microphotograph of the frequency doubler fabricated using a cooperation process between Panasonic PHEMT and the NEL 3-D interconnection process [6] that was developed by NTT Laboratories. The intrinsic size of the device is 1 mm².

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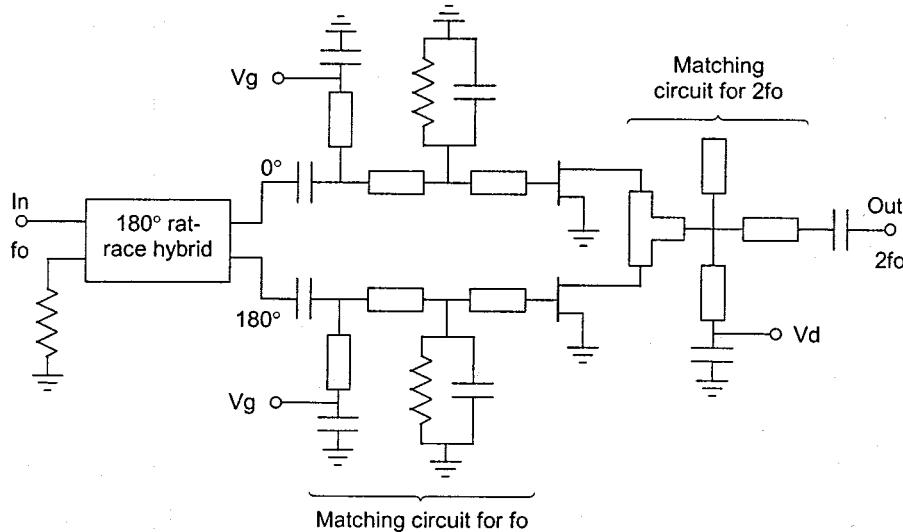


Fig. 1. Circuit schematic of the balanced doubler.

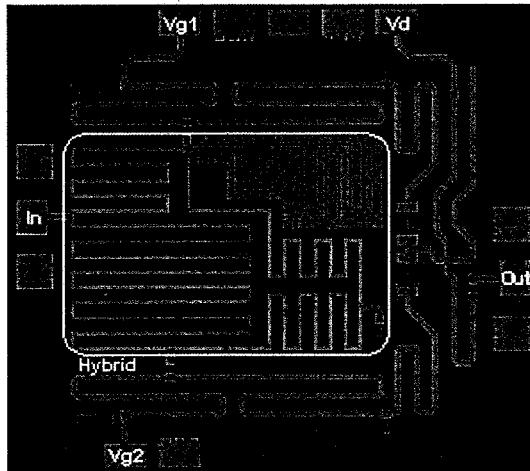


Fig. 2. Microphotograph of the frequency doubler.

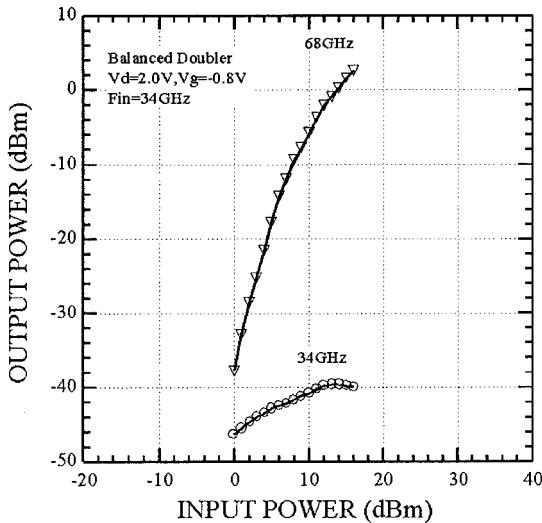


Fig. 3. Measured fundamental and second harmonic output power versus input power at 34 GHz.

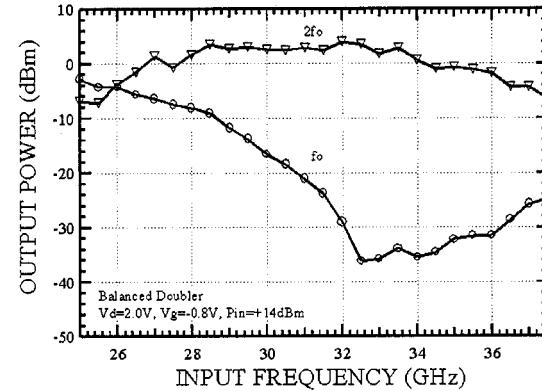


Fig. 4. Measured output power versus input frequency for an input power of 14 dBm.

The hybrid has been designed using $70\ \Omega$ quarter-wavelength and three quarter-wavelength thin film microstrip (TFMS) transmission lines constructed on the surface of the top polyimide layer, 10 μm above the ground plane. The characteristic impedance of the quarter-wavelength short transmission line used to improve the phase balance of the hybrid is $32\ \Omega$. In order to reduce the space of this line, it is constructed on the surface of the top polyimide layer with a ground plane laying 7.5 μm bellow.

III. EXPERIMENTAL RESULTS

Fig. 3 shows the measured output power versus input power of the frequency doubler at 34 GHz. The measurements are performed with a drain voltage of 2.0 V and a gate voltage of -0.8 V that is near the pinchoff voltage. The dc power consumption of the doubler is 50 mW. Due to the lack of precise nonlinear model of the transistors, the output load of the devices has not been optimized for maximum power transfer at the second harmonic. Therefore the resulting conversion loss of the doubler is high. Measured conversion loss is 11.38 dB at 34 GHz, and 8.5 dB at 32.5 GHz.

Fig. 4 shows the frequency response of the doubler for an input power of 14 dBm. The device exhibits a high spectral purity with a measured fundamental rejection of 48 dB and a measured isolation of 40 dB at 32.5 GHz. The device also exhibits ultra broadband operation due to the improved phase and power balance of the hybrid. Isolation better than 30 dB is achieved from 31.7 to 36 GHz. A fundamental frequency rejection better than 35 dB is measured from 31.5 GHz and 37.5 GHz where the upper limit of this bandwidth is limited by our measurement capabilities.

IV. CONCLUSION

A balanced V-band frequency doubler has been designed in the 3-D MMIC technology using $0.15 \mu\text{m}$ pseudomorphic HEMT transistors. This MMIC is of very small size due to the advantageous use of the 3-D technology. Moreover, considering the state of the art of V-band frequency doubler, the realized device exhibits both high spectral purity and ultra broadband operation

which are suitable for the realization of high-quality and widely tunable V-band frequency sources.

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