A New Method for Active Device Load Equivalent Circuit Extraction for MMICs

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***Abstract*—Active device loads for monolithic microwave integrated circuits (MMICs) have been extensively studied and a new procedure for the extraction of their equivalent circuit has been developed. The procedure requires the availability of a coplanar three-terminal device for accurate model extraction. The new procedure is accurate, general, and easy to apply. Its validity has been demonstrated by extracting a scalable bias-dependent small-signal equivalent circuit of PHEMT-based active device loads up to 40 GHz. A good agreement between measured and modeled data has been obtained, confirming the validity and the accuracy of the proposed method.**

***Index Terms*—Circuit simulation, circuit synthesis, HEMT, load, MMIC, modeling.**

I. Introduction

In the last several years, active devices have been increasingly used as a replacement for passive elements in the design of monolithic microwave integrated circuits (MMICs), with the advantage of smaller dimensions and better reproducibility. Active device loads, i.e., transistors with gate and source terminals connected together [Fig. 1(a)], belong to this category. An accurate computer-aided design of integrated circuits including active device loads requires the availability of their equivalent-circuit model. Usually, the same device used for the active device load is available as a three-terminal device, with the source connected to ground through a via hole [Fig. 1(b)]. A straightforward modification of its equivalent circuit [Fig. 2(a)], by simple removal of the source inductance and connection of the source to the gate [Fig. 2(b)], does not give a satisfactory model for the active device load. In fact, on the one hand, the intrinsic elements corresponding to the active region of the device (Fig. 2, within dashed line), are not affected by the active load connection. On the other hand, however, the removal of the via hole and of the air-bridge, and the metal connection from source to gate modify the electro-magnetic field distribution, changing the values of the parasitic elements of the active device load's equivalent circuit with respect to those of the three-terminal device. In this work, we describe an effective procedure for the modeling of the active device load. It includes a simpler equivalent circuit model and a simpler extraction procedure with respect to other proposed methods for the active device load modeling [4]. The procedure requires the availability of a coplanar three-terminal device for the correct determination of the intrinsic elements whereas a simple method is described for the evaluation of the active device load parasitics.

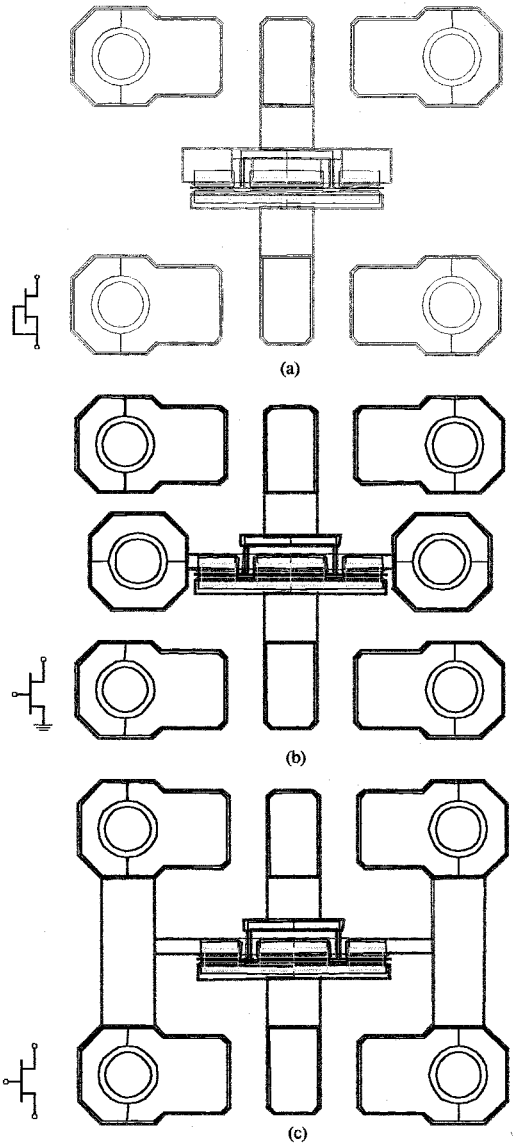

Fig. 1. Layout of (a) the active device load, (b) of the three terminal FET, and (c) of the coplanar three-terminal FET

II. Active Load Modeling Procedure

A family of PHEMT active device loads with 100, 200, 300, and 400 μm gate peripheries, and a family of the same devices in three-terminal coplanar configuration, have been fabricated on the same wafer [Fig. 1(a) and (c)]. The S-parameters have

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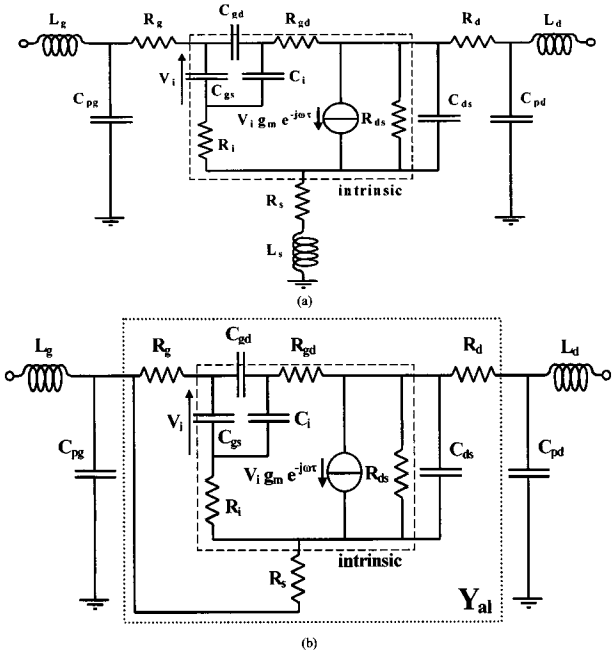

Fig. 2. (a) Three-terminal device equivalent circuit. (b) Active device load equivalent circuit.

been measured from 0.5 to 40.5 GHz at several bias points, in our case, in the range $V_{gd} = 0 \div 4$ V for the active device loads and $V_{gs} = 0.4 \div -1.4$ V, $V_{ds} = 0 \div 4$ V for the three-terminal devices, with a few additional "cold-FET" bias points ($V_{ds} = 0$ V, $V_{gs} > V_{bi}$), for accurate parasitics evaluation [1]–[3].

The coplanar three-terminal devices are more suitable for active device load modeling, because of the closer resemblance of their layout to that of the active device loads with respect to via-hole grounded three-terminal devices [Fig. 1(b)]. The scalable bias-dependent small-signal equivalent circuit model of the coplanar three-terminal devices has been extracted using the standard equivalent-circuit model of Fig. 2(a) and a well-established standard extraction procedure [3]. The extracted values of the intrinsic elements are used also for the active device load at the same bias points, i.e., for $V_{gs} = 0$ V, $V_{ds} = V_{dg}$. The values of the coplanar three-terminal devices' parasitic resistances are also used for the active device load equivalent circuit. All reactive parasitics, on the other hand, must be reevaluated, since the removal of the source via hole changes the field lines distribution between the pads and between pads and ground. For reactive parasitics evaluation, the Y and Z parameters of the active device load measured at two bias points are used. The parasitic capacitances are evaluated from the low-frequency imaginary parts of the measured Y-parameters at saturated drain current bias point ($V_{ds} = V_{gd} > V_{knee} \cong 1$ V) where the output conductance is lowest. For this bias condition the effects of the parasitic inductances can be neglected in the low-frequency range, and the active device load can be modeled by a π equivalent circuit with the following expressions:

$$Y_{11} \cong Y_{a1} + j\omega C_{pg} \tag{1}$$

$$Y_{12} = Y_{21} \cong -Y_{a1} \tag{2}$$

$$Y_{22} \cong Y_{a1} + j\omega C_{pd} \tag{3}$$

TABLE I
COMPARISON BETWEEN THE REACTIVE PARASITIC ELEMENTS OF THE PHEMT ACTIVE DEVICE LOADS (A.D.L.) AND THE REACTIVE PARASITIC ELEMENTS OF THE PHEMT COPLANAR THREE-TERMINAL DEVICES (C.T.T.D.)

	Total gate periphery (μm)				
	100	200	300	400	
L_g (nH)	55	55	55	55	C.T.T.D.
	52	56	60	64	A.D.L.
C_{pg} (fF)	30	30	30	30	C.T.T.D.
	26	28	30	32	A.D.L.
L_d (nH)	20	25	30	35	C.T.T.D.
	56	56	56	56	A.D.L.
C_{pd} (fF)	8	8	8	8	C.T.T.D.
	22	22	22	22	A.D.L.

where Y_{a1} is the admittance of the inner active device load [Fig. 2(b)]. The parasitic capacitances are evaluated from the low-frequency slope of the Y-parameters imaginary parts vs frequency

$$C_{pg} = \frac{\text{Im } Y_{11} + \text{Im } Y_{12}}{\omega} \tag{4}$$

$$C_{pd} = \frac{\text{Im } Y_{22} + \text{Im } Y_{12}}{\omega}. \tag{5}$$

The low-frequency imaginary part of the measured Z-parameters in the ohmic region ($V_{ds} = V_{gd} < V_{knee} \cong 1$ V) gives the necessary information for the parasitic inductances evaluation. At that bias condition, the current through the output channel conductance shunts the intrinsic capacitances, and the following expressions for the Z-parameters can be used to model the low-frequency behavior of the active device

$$Z_{11} \cong \frac{C_{pd}^2}{G \cdot (C_{pg} + C_{pd})^2} + \frac{1}{j\omega \cdot (C_{pg} + C_{pd})} + j\omega \cdot L_g \tag{6}$$

$$Z_{12} = Z_{21} \cong -\frac{C_{pg} C_{pd}}{G \cdot (C_{pg} + C_{pd})^2} + \frac{1}{j\omega \cdot (C_{pg} + C_{pd})} \tag{7}$$

$$Z_{22} \cong \frac{C_{pg}^2}{G \cdot (C_{pg} + C_{pd})^2} + \frac{1}{j\omega \cdot (C_{pg} + C_{pd})} + j\omega \cdot L_d \tag{8}$$

where G is the low-frequency conductance of the inner active device load ($G = \lim_{\omega \to 0} \text{Re}[Y_{a1}(\omega)]$). Since the poles in $\omega = 0$ cancel, the parasitic inductances are evaluated from the low-frequency slope of the imaginary part of the Z-parameters versus frequency as

$$L_g = \frac{\text{Im } Z_{11} - \text{Im } Z_{12}}{\omega} \tag{9}$$

$$L_d = \frac{\text{Im } Z_{22} - \text{Im } Z_{12}}{\omega}. \tag{10}$$

The equivalent-circuit model of the active device load is now complete and available. Table I shows the comparison between the values of the reactive parasitic elements of the PHEMT active device loads and those of the PHEMT coplanar three-terminal devices. A scalable bias-dependent small-signal equiva-

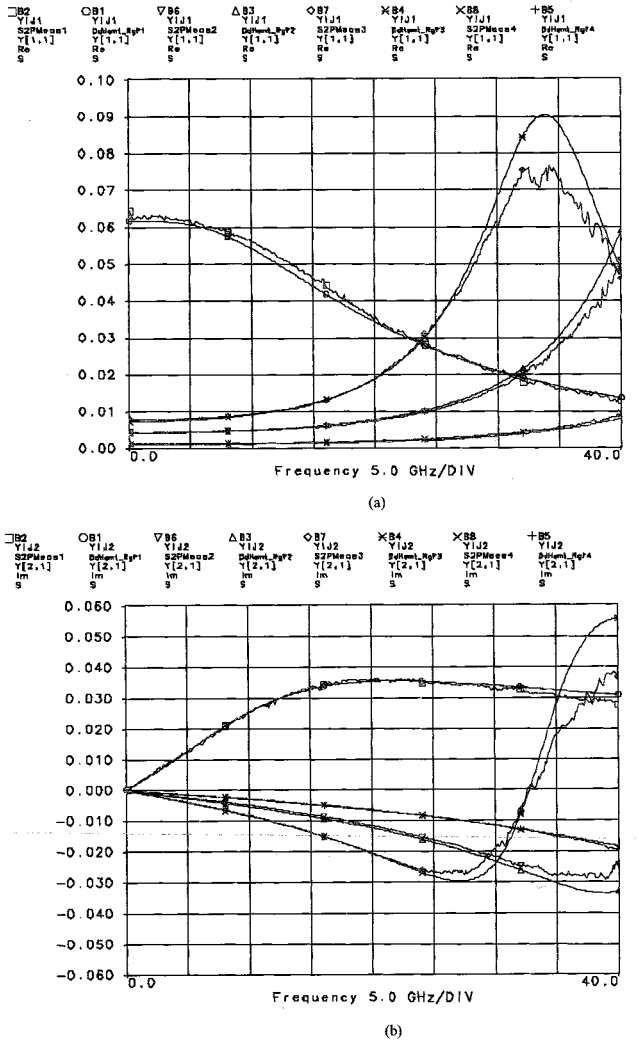

Fig. 3. (a) Measured and modeled real part of Y_{11} and (b) imaginary part of Y_{21} for 100 μm gate periphery active device load at $V_{gd} = 3.4$ V, a 200 μm gate periphery active device load at $V_{gd} = 1.6$ V, a 300 μm gate periphery active device load at $V_{gd} = 2.6$ V, and a 400 μm gate periphery active device load at $V_{gd} = 1.2$ V.

lent circuit for the PHEMT active device loads is therefore obtained combining those parasitics with the intrinsic elements of the scalable bias-dependent small-signal equivalent circuit of the coplanar three-terminal devices. The good agreement between the measured and modeled Y-parameters of the active device loads at several bias points for different gate peripheries (Fig. 3) proves the accuracy of the model, and the validity and robustness of the extraction method.

III. Conclusion

A new method for the extraction of the equivalent circuit of an active device load has been developed. It is based on the availability of a coplanar three-terminal device, for the intrinsic and resistive parasitic elements evaluation, and on a simple extraction procedure for the evaluation of reactive parasitic elements. The method has been applied to the extraction of a scalable bias-dependent small-signal equivalent circuit of 0.25 μm gate PHEMT active device loads, with gate peripheries from 100 to 400 μm, up to 40 GHz. The comparison of the measured and modeled Y-parameter of the active device loads proves the feasibility of the new procedure and the accuracy of the extracted model.

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