K-Band 3-Bit Low-Loss Distributed MEMS Phase Shifter

Yu Liu, Andrea Borgioli, Amit S. Nagra, and Robert A. York

***Abstract*—In this letter, we present a 3-bit K-band distributed phase shifter circuit that employs microelectromechanical systems (MEMS) capacitive switches. The measured results demonstrate an average 1.7 dB insertion loss at 26 GHz with return loss better than −7 dB. Insertion phase shifts of all switching states are measured and show phase error less than 8.5° for all states. The low loss K-band 3-bit phase shifter demonstrated in this letter can potentially be extended to more-bit-controlled phase shifter applications.**

***Index Terms*—Distributed phase shifter, K-band, MEMS, multi-bit, switches.**

I. Introduction

MICROELECTROMECHANICAL systems (MEMS) technology has emerged as a key approach for building low-loss phase shifters, which is essential for modern radar and communications systems. Radio Frequency (RF) MEMS concepts have been successfully applied in the past few years to the development of low-loss RF switching devices and variable capacitors [1]–[3]. RF MEMS capacitive switches have demonstrated many merits compared with conventional switches such as lower loss, lower parasitics and higher linearity. Utilizing these switches in multi-bit phase shifters can drastically reduce loss, thus can significantly reduce cost and weight for phased array antenna where thousands of phase shifters are mounted. Recently, researchers have reported several ways to implement multi-bit phase shifter [4]–[8]. A one-bit distributed phase shifter based on MEMS switching devices was implemented with low insertion loss [[4]]. This technique can then be extended to cascade several 1-bit distributed MEMS phase shifters together to form a multi-bit-controlled distributed phase shifter. Compared with many other topologies, the distributed phase shifter presented here demonstrates much lower insertion loss [[9]]. We fabricated and measured a 3-bit distributed MEMS phase shifter for K-band applications. Fabrication and measurement details are described in this paper.

II. Circuit Design and Fabrication

Fig. 1 (a) shows the photograph of a K-band 3-bit MEMS phase shifter. The 3-bit phase shifter consists of three one-bit phase shifters for 180°, 90°, and 45° phase shift, respectively. Each one-bit phase shifter consists of a coplanar waveguide (CPW) transmission line loaded periodically with several shunt MEMS capacitors. Thus the circuit can be considered as a synthetic transmission line whose phase velocity can be varied by switching the MEMS capacitive switches up and down. DC control bias for each one-bit phase shifter is connected to the ground pad of CPW transmission line while the signal line is connected to dc ground. When a dc bias is applied, the voltage difference between the signal line and ground pad generates a strong electric field underneath the membrane of MEMS switch, which will force the membrane to snap down. The inherent elasticity of metal will help to bounce the membrane back to original state after bias is released. DC block capacitors are added between consecutive ground pads to isolate different dc control bias. Metal-Insulator-Metal (MIM) capacitors with SiN as the dielectric layer are used as the dc blocks in this circuit. The spacing between adjacent ground pads is 20 μm. The area of the MIM capacitor is 100 μm × 100 μm and the thickness of SiN is 6000 Å. To prevent signal leakage from the discontinuity at ground pad, dc block capacitors are connected close to the edge of the ground pad. It should also be noted that the pads for CPW probing at both input and output ports must be dc decoupled from bordered ground pads in order to prevent the ground reference in network analyzer from being connected directly to outer dc power supply.

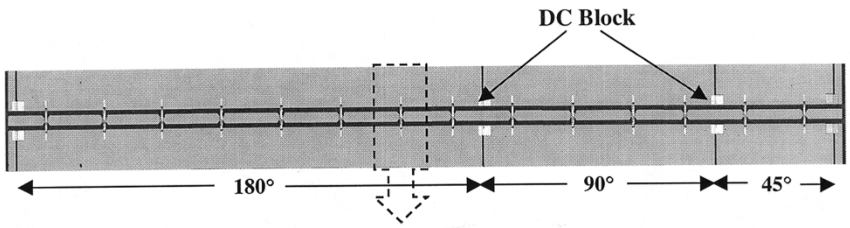
The circuit is fabricated on a glass substrate $(\varepsilon_r = 5.7, \tan(\delta) = 0.001)$. The total length of the circuit is 11 mm. The spacing between the MEMS capacitors is 780 μm. The CPW transmission line has 100 μm central conductor width and the ground-to-ground spacing is 190 μm. This provides us a high impedance transmission line $(Z_{\mathrm{UP}} = 67\ \Omega)$ when MEMS capacitive switches are at UP states. When switches are snapped down, the transmission line is periodically loaded with MEMS DOWN- state capacitors and will resemble a low impedance transmission line $(Z_{\mathrm{DOWN}} = 37\ \Omega)$. In this way, we can get desired phase shift without sacrificing too much in return loss.

In order to maintain an acceptable matching over a wide band, small DOWN state capacitance value for MEMS switches is required. In this circuit, the UP state capacitance per period is approximately 5 fF and a 0.1 pF DOWN state capacitance value is necessary for good matching. To reduce the DOWN state capacitance value of the single MEMS switch, one possible approach is to use series connected MEMS switch configuration [4]. The drawback in this approach is the capacitance value of the fixed capacitor is usually required to be ultra small, which means the area of this capacitor will be too small to be

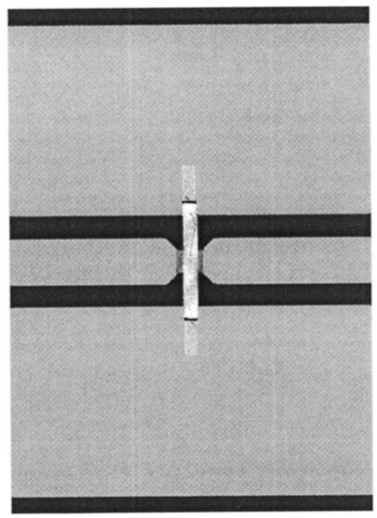
Manuscript received May 18, 2000; revised July 27, 2000. This work was supported by Air Force Research Laboratory under the Toyon program (Agency Contract Number F19628-99-C-0017) and by DARPA under the FAME program (Agency Contract Number DABT63-98-1-0006).

The authors are with the Electrical and Computer Engineering Department, University of California at Santa Barbara, Santa Barbara, CA 93106 USA.

Publisher Item Identifier S 1051-8207(00)09720-8.



(a)



(b)

Fig. 1. (a) Photograph of the 3-bit distributed MEMS phase shifter circuit fabricated at UCSB. (b) Close-up of MEMS switch.

used in multi-bit phase shifter. In this circuit, the central conductor is tapered from 100 μm to 50 μm at the place where MEMS switch is built, as shown in Fig. 1(b). 6000 Å SiN layer is deposited. Thus the DOWN state capacitance value can be significantly reduced.

The 3-bit phase shifter is fabricated by first patterning and evaporating 200/10 000 Å layer of Ti/Au as CPW transmission line on a glass substrate. A 6000 Å plasma-enhanced chemical vapor deposition (PECVD) SiN layer is deposited at 290 °C chamber temperature and patterned on top. Next, a 3 μm thick sacrificial photoresist layer, which determines the height of the MEMS bridge, is patterned. A 30-min reflow bake on 250 °C hotplate is taken to guarantee the airbridge can be supported steadily. A 200/20 000 Å Ti/Al layer is then evaporated on top of the sacrificial layer. The sacrificial photoresist is then removed and a critical point drying system is used to release the MEMS bridges. The width and the span of the membranes are 30 μm and 200 μm respectively.

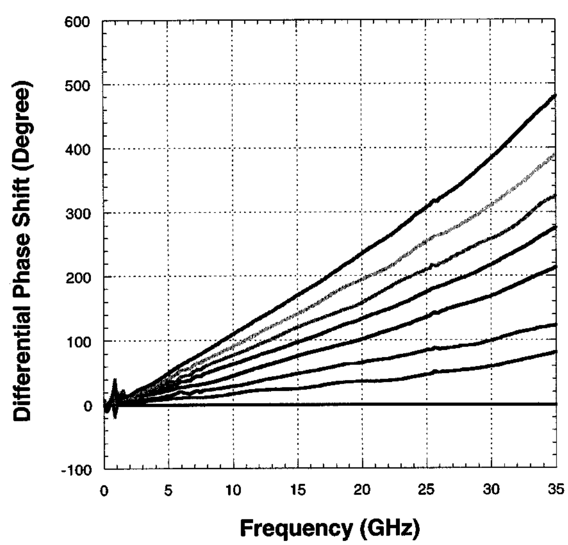


Fig. 2. Measured differential phase shift versus frequency at all MEMS switching states.

III. Measurement Results

RF measurements were made on a HP 8722D network analyzer, calibrated using on-wafer standards. The two-port s-parameters of the circuit were recorded up to 35 GHz. Fig. 2 illustrates the differential phase shift as a function of frequency for all eight switching states. The actuation voltage for MEMS switch is about 60 V. Fig. 3 shows the insertion loss and the return loss for all of the switching states. The circuit was designed to have 360 ° phase shift at 26 GHz. The average insertion loss is 1.7 dB at 26 GHz and the worst-case insertion loss is 2.6 dB. Return loss is better than −7 dB. Besides conductive loss, the mismatch between two consecutive sections will generate wave reflection and will deteriorate loss and matching performance, which accounts for the poor input match at frequency over 30 GHz. Thus it is expected to improve circuit performance by choosing appropriate circuit parameters to match the circuit for all switching states. Measurement shows the circuit will shift

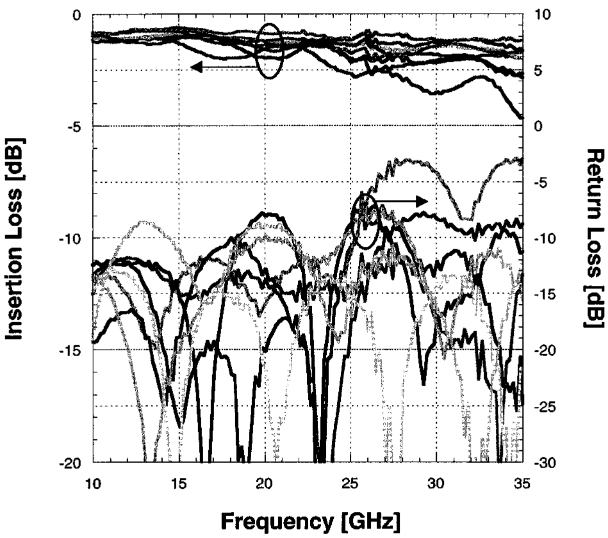


Fig. 3. Measured insertion loss and return loss versus frequency at all MEMS switching states.

TABLE I
THREE-BIT PHASE SHIFT DATA AT 26 GHz

Phase State	0.0°	45.0°	90.0°	135.0°	180.0°	225.0°	270.0°	315.0°
Measured	0.0°	49.5°	85.6°	143.3°	183.7°	219.3°	262.9°	321.3°
Phase Error	0.0°	-4.5°	4.4°	-8.3°	-3.7°	5.7°	7.1°	-6.3°

phase from 0° to 315° with 45° phase step at 26 GHz and the measured phase error for all switching states are less than 8.5°. Detailed phase shift data is listed in Table I.

IV. CONCLUSION

In summary, we have designed, fabricated and tested a K-band 3-bit distributed MEMS phase shifter on a glass substrate. The phase shifter demonstrates an average 1.7 dB insertion loss at 26 GHz with return loss better than −7 dB. The circuit produces a phase shift from 0° to 315° with 45° phase step and the measured phase error for all switching states is less than 8.5°. This work can potentially be extended to more-bit-controlled phase shifter applications.

REFERENCES

[1] C. Goldsmith, T. H. Lin, B. Powers, W. R. Wu, and B. Norvell, "Micromechanical membrane switches for microwave applications," *1995 IEEE MTT-S Dig.*, pp. 91–94.

[2] E. Brown, "RF-MEMS switches for reconfigurable integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1868–1880, Nov. 1998.

[3] E. K. Chan, E. C. Kan, R. W. Dutton, and P. M. Pinsky, "Nonlinear dynamic modeling of micromachined switches," *1997 IEEE MTT-S Dig.*, pp. 1511–1514.

[4] A. Borgioli, Y. Liu, A. S. Nagra, and R. A. York, "Low-loss distributed MEMS phase shifter," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 7–10, Jan. 2000.

[5] J. S. Hayden and G. M. Rebeiz, "Low-loss cascadable MEMS distributed X-band phase shifters," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 142–144, Apr. 2000.

[6] N. S. Barker and G. M. Rebeiz, "Distributed MEMS true-time delay phase shifters and wide-band switches," *IEEE Microwave Guided Wave Lett.*, vol. 46, pp. 1881–1890, Nov. 1998.

[7] A. Malczewski, S. Eshelman, B. Pillans, J. Ehmke, and C. L. Goldsmith, "X-band RF MEMS phase shifters for phased array applications," *IEEE Microwave Guided Wave Lett.*, vol. 9, pp. 517–519, Dec. 1999.

[8] B. Pillans, S. Eshelman, A. Malczewski, J. Ehmke, and C. Goldsmith, "Ka-band RF MEMS phase shifters," *IEEE Microwave and Guide Wave Lett.*, vol. 9, no. 12, pp. 520–522, Dec. 1999.

[9] A. S. Nagra and R. A. York, "Distributed analog phase shifters with low insertion loss," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 1705–1711, Sept. 1999.