A 26.5 GHz Silicon MOSFET 2:1 Dynamic Frequency Divider

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***Abstract*—A bulk silicon divide-by-two dynamic frequency divider with maximum clock speed of 26.5 GHz has been achieved. The dynamic divider operates from 6.5 GHz to 26.5 GHz. The design is based on n-channel MOSFET's with an effective gate length of 0.1 μm.**

***Index Terms*—CMOS digital integrated circuits, frequency divider, high-speed integrated circuits.**

I. Introduction

With the recent explosion of the communications industry, the consumer market has an increasing need for radio frequency (RF) circuits in high volume, with high performance, and with low cost. In addition to being a key component needed for a phase locked loop in many communication systems, high-speed frequency dividers are used as a benchmark for high-speed technologies. Frequency dividers based on compound semiconductor technologies using HBT and HEMT's have demonstrated performance up to 80 GHz [1]–[3]. Recently, there have also been studies showing SiGe HBT based frequency dividers operating up to 82 GHz [4], [5]. With an increase in demand, comes pressure to implement circuits in a technology more developed for high levels of integration and potentially lower cost. This has sparked many studies to increase the performance of silicon MOSFET's [6]–[8]. In this letter, we present a dynamic digital frequency divider fabricated in a 0.1 μm bulk silicon MOSFET technology that operates up to 26.5 GHz. To the author's knowledge, this is the fastest silicon MOSFET digital frequency divider reported to date.

II. Device Technology and Circuit Design

The fabrication process was a standard digital CMOS process. The minimum drawn gate length was 0.15 μm, giving a 0.1 μm effective gate length. The devices were made in a single n-well process, employing a 1–2 Ω-cm p-type substrate and two levels of metallization. The gate oxide was 30 Å thick. At a drain to source bias of 0.8V and a gate to source bias of 0.8V, a 0.1 μm $\times$ 20 μm NMOS device has a dc transconductance of 500 mS/mm. NMOS devices have an f_t of 95 GHz. The devices have a breakdown voltage of over 3V.

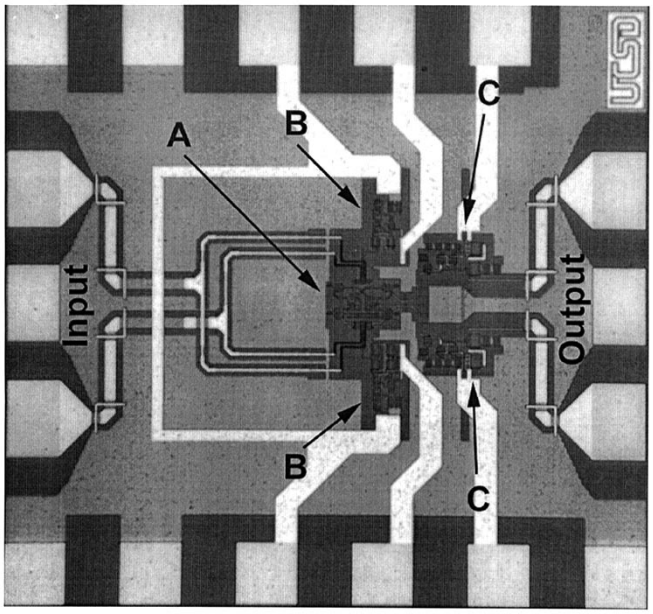

Fig. 1. Microphotograph of frequency divider circuit. Circuit dimensions limited by probe pads. Circuit 830 μm $\times$ 780 μm. A: Flip-flop 97 μm $\times$ 66 μm B: Current sources 40 μm $\times$ 79 μm each. C: Output buffer 110 μm $\times$ 45 μm each.

The process had no resistor layer, so diode-connected devices were used as active loads. In order to achieve the highest possible clock speed, an all NMOS design in source coupled FET logic (SCFL) was used. The use of SCFL made it possible to make a fully balanced design. The layout was made as symmetrical as possible. The size of the circuit was limited by the size of the probe pads. The circuit was placed as close to the output pads as possible, with coplanar lines connecting the clock pads to the circuit input. A die photograph is shown in Fig. 1. Although the size of the circuit is 830 μm $\times$ 780 μm, the flip-flop takes up only 97 μm $\times$ 66 μm of space while the current sources take up 80 μm $\times$ 79 μm. The output buffer has dimensions 110 μm $\times$ 90 μm.

The circuit design is similar to that of a clocked oscillator employing two logic stages (one of which is inverting). A simplified schematic of the circuit is shown in Fig. 2. The logic stages, in addition to a main differential pair (the reading pair), contain a cross-connected transistor pair (the latching pair) driven by

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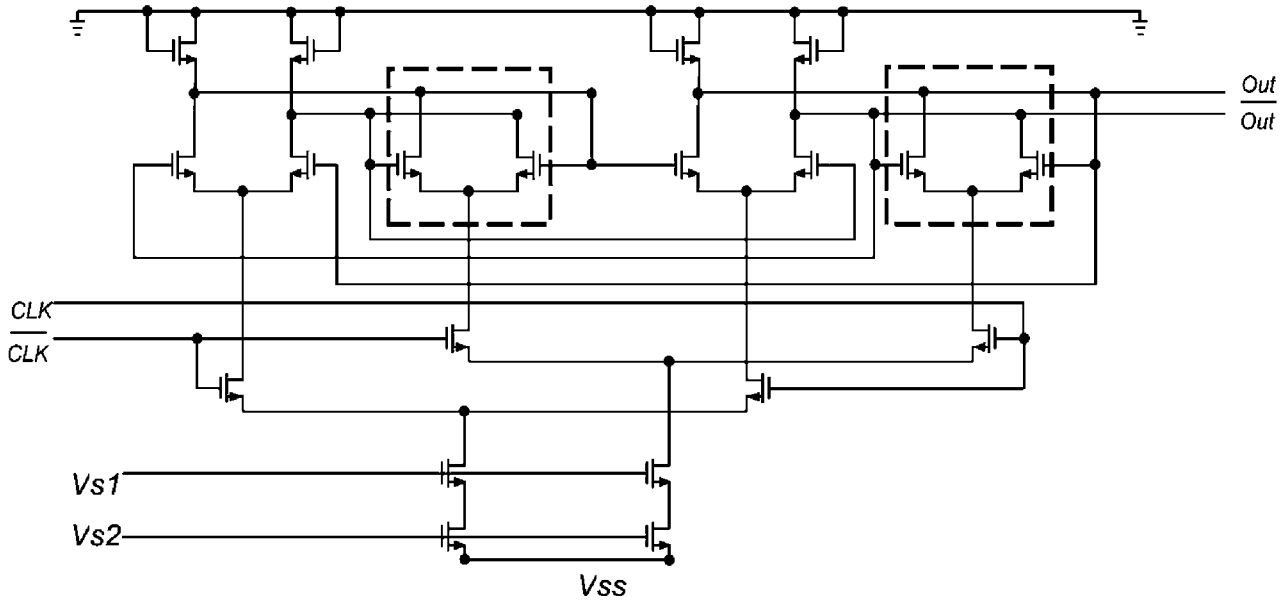

Fig. 2. Simplified circuit schematic. The latching stages are enclosed in dashed boxes. V_{s1} and V_{s2} from on-chip cascode current source.

the same phase of the clock. When the reading pair of the logic stage begins to change state, the latching pair boosts the current to speed up the output voltage swing. The latching pair provides positive feedback to increase the gain of the stage. Since the latching pair does not maintain the output logic level with the clock transistor off, this circuit is a dynamic divider.

Simulations indicate that the rise and fall times of the logic stage vary roughly inversely with the ratio of WL to WR. For increasing values of WL/WR, power dissipation increases. In our circuit, the width of the n-MOSFET's used in the reading pair was 24 μm (WR) and that of the latching transistors was 9 μm (WL). This gives a WL/WR value of 0.375, which provides a boost in speed with only a moderate increase in power.

The circuit design shares many features with the dynamic HLO-FF [9] frequency divider. The HLO-FF makes use of stages which contain reading and latching pairs of different width. However, in HLO-FF dividers the reading and latching transistor pairs are driven with different phases of the clock, and in the limit of WL/WR $= 1$ the circuit becomes a conventional static divider. This is not the case in the present design.

The outputs of SCFL circuits are referenced to V_{dd}. To reduce potential effects of line bounce on V_{dd}, V_{dd} was made to be ground, and all other voltages are negative. A negative bias was applied to the p-substrate in order to prevent leakage currents. The top rail of the current source is connected to a pad rather than ground, so that the current through the flip-flop can be adjusted. To be able to adjust the output buffer independently of the flip-flop, the bottom rail of the output buffer has its own V_{ss} pad separate from the rest of the circuit. Voltages V_{s1} and V_{s2} in Fig. 2 are generated on chip with a cascode current source.

III. Results

Tests were performed on wafer. High-speed signal-ground-signal probes were used for the clock input and the divide by two output. Power probes with bypass capacitors close to the probe tip were used to provide dc biasing. A dc bias voltage was provided as reference to both inputs. One of the inputs was also fed with the clock input while the other input was ac terminated off-chip with 50 Ω to ground. The output signal was measured differentially with an external 180° hybrid. -10 dB couplers were used on the input and output to plot the input waveform and measure the output spectrum respectively. An HP54120 50 GHz oscilloscope was used to measure the waveforms, while an HP8565E spectrum analyzer was used to measure the output spectrum.

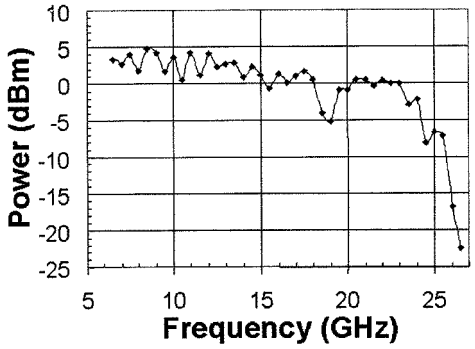

Fig. 3. Measured input sensitivity versus input clock frequency for single-ended drive with second input ac terminated off chip.

The input sensitivity versus input frequency is shown in Fig. 3. For most of the bandwidth, the divider needs a single ended input power of about 0 dBm to operate. This is within ± 4 dB of the input power needed by other reported dynamic frequency dividers that do not have an input buffer to amplify the clock signal [1], [2], [9]. Many frequency dividers have a null in input power versus frequency where the divider self-oscillates. Although our dynamic divider does not self-oscillate, the dip in required input power shows it to be close to oscillating at 26 GHz. Fig. 4 shows dc power consumed by the flip-flop plus current sources versus frequency and the dc power consumed

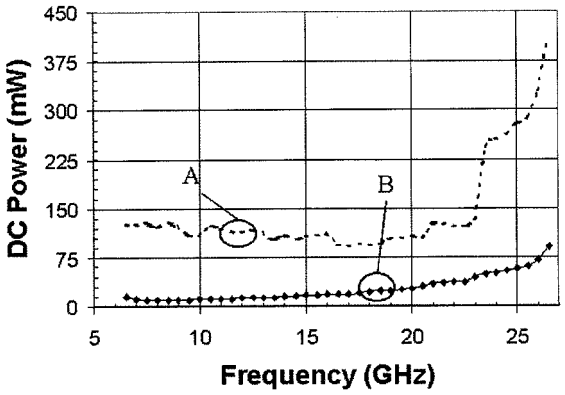

Fig. 4. A: Measured dc power consumed by output driver. B: Measured dc power consumed by the flip-flop and current sources.

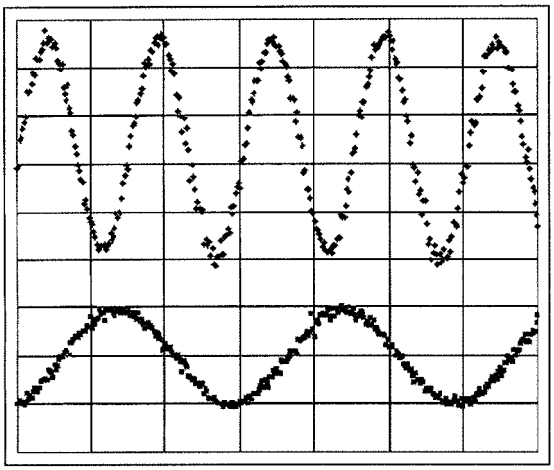

Fig. 5. Measured input (top) waveform at 26.5 GHz and output (bottom) waveform at 13.25 GHz. (25 ps/div., 5 mV/div.)

by the output buffer versus frequency. For input clock frequencies up to 20 GHz, the flip-flop and current sources use less than 26 mW of dc power. This power is substantially lower than that used in many other high-speed frequency dividers. At the maximum frequency of 26.5 GHz, the flip-flop uses 90 mW of dc power. Fig. 5 shows the input clock at 26.5 GHz and the divide by two output. Measurements of the frequency range and output power agree well with circuit simulations. The simulations show correct operation of the circuit from 6 GHz to 25 GHz. The simulated output power is within 1 dB of the measured output power. The relatively low measured output power can be attributed to the very simple output buffer design used. The output buffer was designed primarily to buffer the divider from the large pad capacitance and provides attenuation rather than voltage gain. Simulations indicate that the on-chip differential voltage swing in the divider core was 250 mV for operation at 25 GHz (and up to 600 mV at 20 GHz).

IV. Conclusion

We have shown that scaled bulk silicon 0.1 μm CMOS technology can be used for digital circuits clocked above 20 GHz. A bulk silicon MOSFET 2 : 1 dynamic frequency divider was shown to operate up from 6.5 GHz to 26.5 GHz. The flip-flop plus current sources use only 26 mW of dc power at a clock frequency of 20 GHz. To our knowledge, this is the fastest frequency divider in CMOS technology reported to date.

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