$BaSrTiO_3$ Interdigitated Capacitors for Distributed Phase Shifter Applications

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***Abstract*—In this letter, $BaSrTiO_3$ (BST) interdigitated capacitors on sapphire substrates have been investigated. The tunability and quality factor of interdigital capacitors has been optimized for microwave and millimeter wave applications. A monolithic K-band phase shifter circuit that employs voltage tunable $BaSrTiO_3$ (BST) interdigitated capacitors is presented here.**

***Index Terms*—$BaSrTiO_3$, distributed phase shifter, interdigital.**

I. Introduction

Modern phased array antenna systems require low loss, low cost microwave phase shifters. Phase shifters using Barium Strontium Titanate ($Ba_xSr_{1-x}TiO_3$), which has high tunability, low loss tangent and high power handling capability, are very promising as a replacement for traditional ferrite and semiconductor devices phase shifters. Several groups are investigating the possibility of implementing phase shifter circuits using barium strontium titanate (BST). Among recent demonstrations, ferroelectric material (BST) either forms the entire microwave substrate [1], [2] on which the conductors are deposited (thick films/bulk crystals) or a fraction of the substrate with thin BST films sandwiched between the substrate and conductors [3]–[5]. These approaches result in either inefficient use of ferroelectric materials or high conductor losses. Distributed phase shifter, compared with other types of phase shifters, has the advantage of true time delay which is required for phased array antenna applications. Distributed phase shifters consisting of coplanar waveguide lines that are periodically loaded with BST parallel plate varactors have been implemented and showed 27.6°/dB performance [6]. The main limitation in this approach is that the quality factor of BST parallel plate capacitors is quite low (dominated by series resistance in electrodes). To further reduce insertion loss interdigitated BST capacitors were used as replacements for parallel plate BST capacitors in periodically loaded phase shifter circuits. In addition to lower losses, phase shifters using interdigitated BST capacitors also have the additional advantage of being easier to fabricate.

In this paper, BST interdigitated capacitors have been designed and characterized for microwave and millimeter-wave applications. The BST film thickness, finger width and spacing were optimized to achieve maximum tunability. The optimized capacitor showed 1.75 : 1 tunability and quality factor larger than 20 up to 24 GHz. Distributed analog phase shifters periodically loaded with these optimized BST interdigitated capacitors were fabricated and tested at 20 GHz. The phase shifters reported here had a figure of merit of 32°/dB at 20 GHz, which is very promising.

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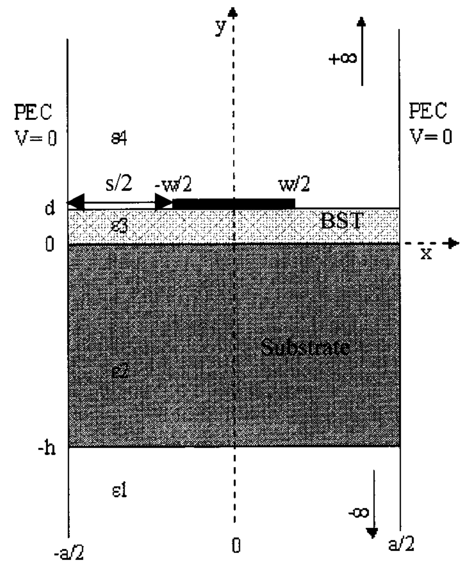

Fig. 1. Schematic of BST interdigitated capacitor for the static field analysis.

II. Characterization

Static field analysis was used to analyze the capacitance and tunability of BST interdigitated capacitors. Adjacent fingers are considered to be at a potential of $+V/2$ and $-V/2$ so that the plane of symmetry between the two fingers can be replaced with a perfect electric conductor. Fig. 1 shows the section used to make the static field analysis. As shown in Fig. 1, the finger width is $\boldsymbol{w}$, the finger spacing is $\boldsymbol{s}$, BST thin film thickness is $\boldsymbol{d}$ and the substrate thickness is $\boldsymbol{h}$. Poisson's equation was applied to each layer. By meeting the boundary conditions between consecutive layers the amount of charge Q on the finger can be determined as a function of applied dc bias. Interdigitated capacitor can be modeled as parallel resistor-capacitor, then the capacitance can be easily determined.

An important goal was to maximize the tunability of the BST interdigitated capacitor. Several structures were investigated. While the above simulation shows that increasing ferroelectric thin film thickness $\boldsymbol{d}$ could increase the tunability,

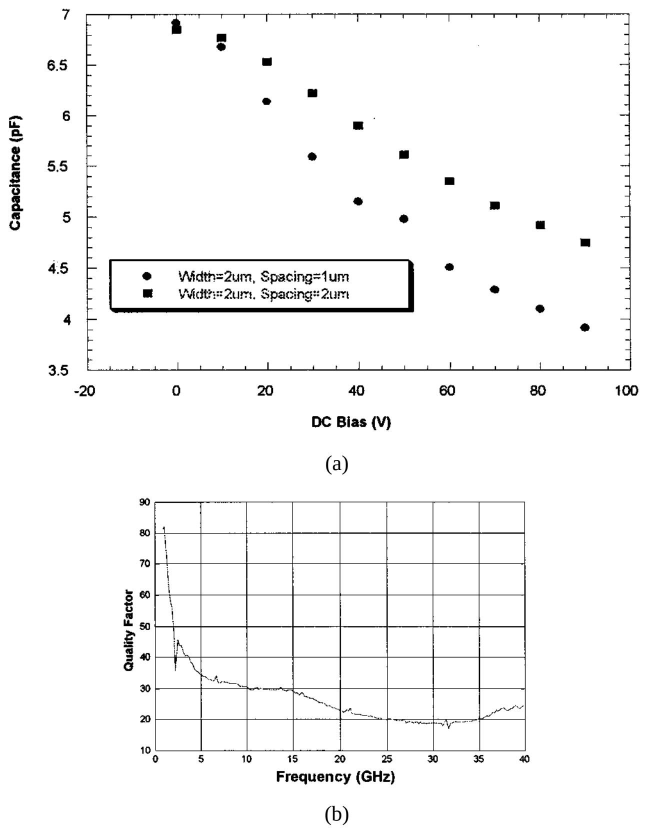

Fig. 2. (a) Capacitance versus dc control bias for 1) finger width = 2 μm, spacing = 1 μm; 2) finger width = 2 μm, spacing = 2 μm. (b) Quality factor versus frequency.

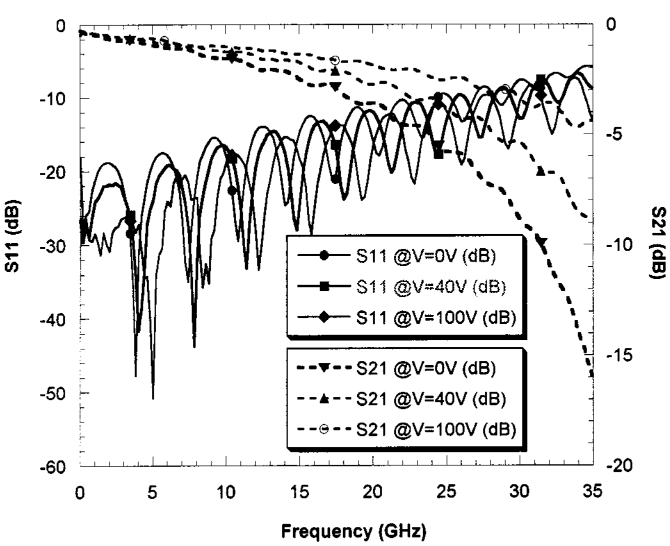

Fig. 3. S_{11} and S_{21} of BST interdigitated capacitor loaded distributed phase shifter at 0 V, 40 V, and 100 V dc bias.

it also increases dielectric loss. Fig. 2(a) shows the measured capacitance variation as a function of dc bias for two capacitor structures on a 100 nm BST sample. From the plot it can be seen that the capacitor with spacing 1 μm can effectively tune the capacitance from 7 pF at 0 V dc bias to 3.8 pF at 90 V dc bias (tunability of 1.75 : 1). The capacitor with spacing 2 μm has much lower tunability because the dc bias is not large enough to tune the capacitor effectively. Since the dielectric constant of BST is controlled by the electric field inside the material, with the same dc bias, the electric field in the thin film with spacing 2 μm will be much lower than the one with spacing 1 μm. To further reduce required dc bias, we could shrink the spacing between adjacent fingers to as small as possible.

The motivation for using interdigital structures was its inherently high-Q value and ease of processing. So it was essential to characterize the quality factor of BST interdigitated capacitors. Characterization was made by one-port reflection measurements on a HP 8722D network analyzer with on-wafer open and short calibration. The measured s-parameters were then used to extract the quality factor and the capacitance value. Fig. 2(b) shows the quality factor of a BST interdigitated capacitor with 100nm BST film thickness, 2 μm finger width and 1 μm finger spacing. The quality factor is larger than 20 from 0 to 24 GHz. This, in addition to the high tunability, made it possible to use BST interdigitated capacitors in microwave phase shifter circuits.

III. Distributed Phase Shifter Design

The distributed phase shifter circuit is comprised of a high impedance (Z_i) transmission line periodically loaded with voltage variable capacitors (C_{var}) with spacing L_{sect}. Using the proper design technique [7], the synthetic transmission line can have maximum phase shift with lowest possible insertion loss while maintaining good matching at the input port. The operating frequency for the phase shifter presented here was designed to be 20 GHz. The Bragg frequency for the periodically loaded line was chosen to be 40 GHz. For the design of the interdigital capacitors, a BST thin film thickness of 100 nm, finger width of 2 μm and finger spacing of 1 μm was used. The zero bias capacitance of each interdigitated capacitor used in the design was 82 fF. Due to symmetry considerations, the capacitor was divided in half (41 fF each) and connected in parallel from the center CPW line to each ground pad. The circuit was fabricated on sapphire (c-axis orientation) using standard monolithic fabrication techniques. BST for the tunable capacitors was deposited by RF magnetron sputtering and 4000 Å thick gold was evaporated on BST to make the interdigital pattern. The BST in the capacitor active region was covered by photoresist and BST film elsewhere was etched away by buffered hydrofluoric acid. Finally, 1.5 μm gold was deposited as the coplanar transmission line.

RF measurements were made on a HP8722D network analyzer that was calibrated using on-wafer standards. The two-port s-parameters of the phase shifter circuit were recorded up to 35 GHz. Fig. 3 shows the return loss and insertion loss of the phase shifter circuit at 0 V, 40 V and 100 V dc biases. Fig. 4 shows the differential phase shift (with respect to the zero bias insertion phase) as a function of frequency for dc biases at 40 V and 100 V. The circuit shows 0–110° phase shifts at 20 GHz with a maximum insertion loss of 3.4 dB. The return loss is less than -14 dB over all phase states.

IV. Conclusion

$BaSrTiO_3$ interdigitated capacitors have been investigated and their design has been optimized for high tunability and

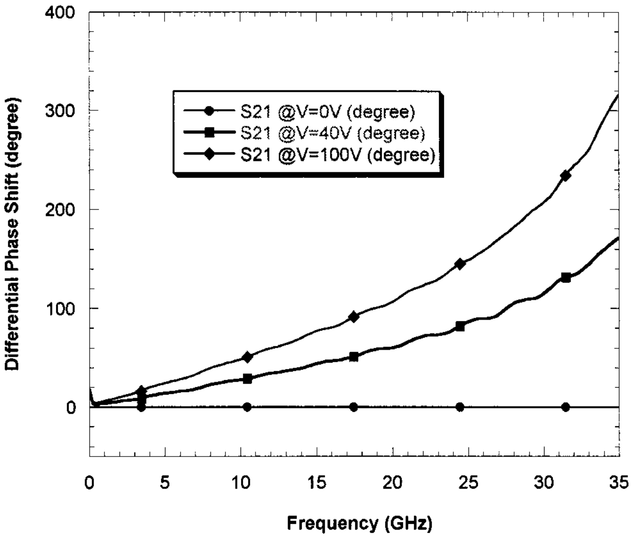

Fig. 4. Differential phase shift at 40 V and 100 V dc control bias.

large quality factor. A monolithic K-band phase shifter circuit that employs voltage tunable BaSrTiO3 interdigitated capacitors has been designed, tested and fabricated. The phase shifter demonstrated continuous phase shift from 0 to 110° at 20 GHz with a maximum insertion loss of 3.4 dB. The phase shifter performance will benefit strongly from the ongoing efforts to further improve the tunability and quality factor of the BST interdigitated capacitors.

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