Microwave Noise Modeling of InP Based MODFETs Biased for Low Power Consumption

J. M. Miranda, M. Nawaz, P. Sakalas, H. Zirath, and J. L. Sebastián

***Abstract*—This paper presents the fabrication, experimental characterization and modeling of 0.15 μm gate-length lattice matched MODFETs based on InP technology. The variation of the drain noise temperature of the Pospieszalski model (T_D) with the applied bias has been investigated under very low power consumption conditions, and a noticeably complex dependence of this factor on the drain current has been observed. In fact, T_D can decrease with increasing drain currents, and suffers a strong increase as a function of the drain voltage even at very low values of the drain current. However, all of these effects can be qualitatively explained from physical considerations.**

***Index Terms*—Microwave FETs, MODFET, noise measurements, semiconductor device noise.**

I. Introduction

InP-MODFETs offer state of the art low-noise performance and superior high frequency response. The high mobility and carrier velocity in the InGaAs-layer enable these devices to provide excellent noise and gain behavior at extremely low drain to source voltages. Pospieszalski model [1] has emerged as one of the most accurate and convenient ways to obtain the noise parameters of these devices in CAD tools [2]. It is well known that one of the main limitations of this model is found in the neglection of the correlations between the gate and the drain current. The aim of this work is to study if the approach of Pospieszalski yields to noticeable inaccuracies in the noise parameter calculations when the transistor is biased for very low power consumption operation. With this aim in mind, we have made investigations which cover the fabrication, on wafer noise testing and simulation of 0.15 μm gate length MODFETs based on InP technology.

II. Description of the Devices

The measured devices are lattice matched MODFETs with single $Al_{0.52}In_{0.48}As/In_{0.53}Ga_{0.47}As$ channel that have been grown on 3-in InP substrate with molecular beam epitaxy (MBE). They were processed with a combination of optical and electron beam lithography techniques. The source-drain ohmic contacts were fabricated with Ni/Ge/Au metallization (180/500/1000 Å), and the gates were defined with a trilayer resist (PMMA/PMGI/PMMA) and single electron beam exposure [3] with modulation of the exposure dose. The gate metallization consists of two fingers of 50 μm width and 0.15 μm length made with Ti/Pt/Au (200/100/3200 Å). Finally, the devices were passivated with 800 Å sputtered Si_3N_4.

The transistors exhibit excellent gate leakage and pinchoff characteristics, as well as I–V curves in which no kink effects were observed. The gate-drain breakdown voltage measured at 1 mA/mm gate current is close to 5 V. These devices provide a cutoff frequency of 100 GHz and a maximum oscillation frequency of 300 GHz. The maximum gate current obtained in the measurements presented here was 15 nA, and a minimum noise figure of 1.3 dB was measured at 20 GHz for a drain voltage of 1.1 V.

The small signal equivalent circuit of the devices was extracted using an inhouse Labview program based on the cold FET method [4]. In order to test the accuracy of the circuital model, an error function has been estimated in the simulation of the S and noise parameters. This function is obtained from the rms values of the discrepancies between the S and the noise parameters averaged over all the frequency points, as described in [5].

III. Noise Measurement and Simulation

On wafer noise and S parameter measurements were performed in the range 2–26 GHz with a probe station, a network analyzer (HP8510) and an automated noise measurement system ATN NP5. In order to optimize the accuracy in the small signal modeling, the noise and S parameter measurements needed for the cold FET extraction method were all made without any intermediate removal of the probes from the contact pads.

The drain and gate temperatures (T_D and T_G) of the Pospieszalski method [1] were initially extracted from the noise measurements and then tuned by direct optimization at each bias point. This optimization was necessary at the lowest bias currents where the inaccuracies in the calculation of T_G did not led to a smooth dependence of this parameter on the drain current. These inaccuracies arise from the weak influence of T_G on the noise parameters. The optimization of T_G implicitly keeps T_G close to the room temperature when the initial values are set to this temperature. Although this is highly convenient to find closed form expressions for T_G as a function of V_{DS}, it must be pointed out that the gate to source junction can be the origin of strong excess noise, especially

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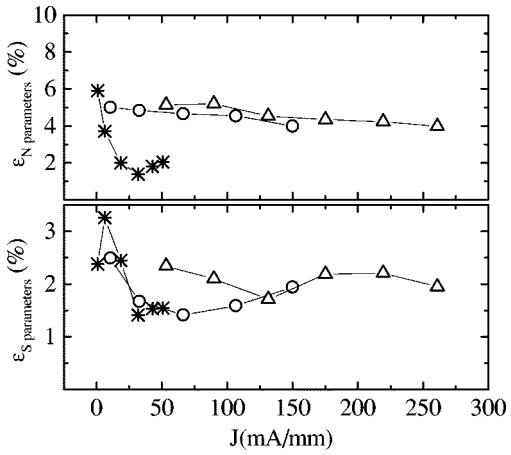

Fig. 1. Errors in the calculation of the S and noise parameters. Asterisks: $V_{DS} = 0.1$ V. Circles: $V_{DS} = 0.6$ V. Triangles: $V_{DS} = 1.1$ V.

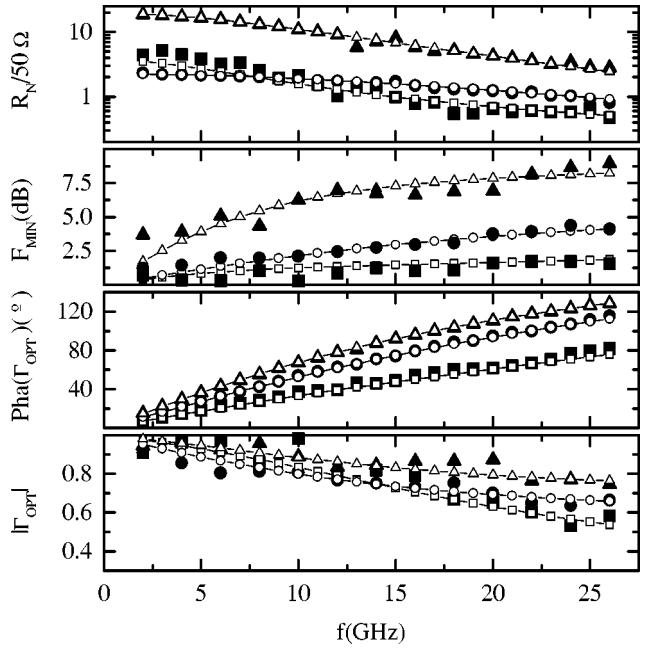

Fig. 2. Comparison between measured (solid symbols) and simulated (open) noise parameters for $V_{DS} = 0.1$ V. Squares: $V_{GS} = -0.8$ V. Circles: $V_{GS} = -0.6$ V. Triangles: $V_{GS} = -0.3$ V. These bias points correspond to the first, third and sixth points of the error curves shown in Fig. 1, and the corresponding transconductances are 6%, 27% (maximum g_m at this drain voltage) and 14% of the maximum transconductance achieved by the device, respectively.

under highly reversed gate to source voltages. Therefore, under these circumstances T_G does not provide information on the true noise behavior of the device input, no matter how accurate are the noise parameter predictions.

Fig. 1 shows the errors in the S and noise parameters obtained in the simulations. The S parameters were calculated with a reasonable accuracy at all the bias points, being the maximum error around 3.5%. The accuracy was particularly good at the lowest drain voltages (0.1 and 0.6 V) and for current densities between 25 and 100 mA/mm, where the error is below 1.5%. On the other hand, a maximum error of 6% was obtained in the simulation of the noise parameters.

A direct comparison between the simulated and measured noise parameters is shown in Fig. 2 for a drain voltage of 0.1 V. At this voltage the peak transconductance is only 27% of the maximum transconductance achieved by the device, which was 480 mS/mm. This figure includes the worst case fit obtained, which corresponds to a gate voltage of -0.8 V, a drain current of 0.8 mA/mm and a transconductance of 31 mS/mm. A combination of different reasons made this bias point particularly difficult to measure 1) the minimum noise figure is still low, below 2 dB at 26 GHz, 2) the noise resistance is relatively high, reaching around 250 ohms at 2 GHz, and 3) the associated gain is very low even at 2 GHz, being 6 dB at this frequency and dropping to -1 dB at 26 GHz. However, even under this extreme situation the simulations presented in this work were able to provide a reasonable accuracy. The measured gate current for maximum negative gate to source voltage was fairly low: 6 nA for $V_{DS} = 0.1$ V, 6 nA for $V_{DS} = 0.6$ V and 14 nA for $V_{DS} = 1.1$ V. Therefore, we do not expect important noise contributions coming from neither gate leakage nor impact ionization, such as those reported in [6] and [7], respectively.

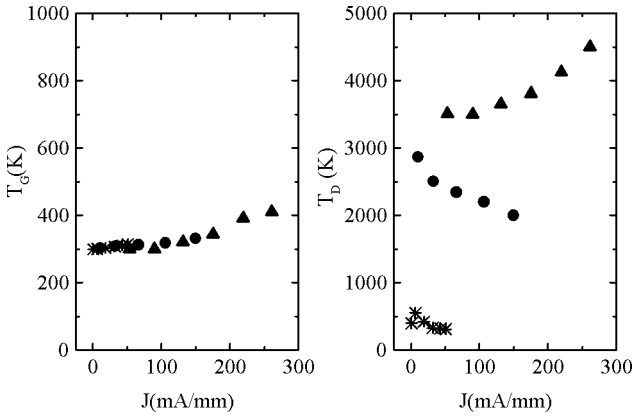

Fig. 3. Calculated drain and gate temperatures. Asterisks: $V_{DS} = 0.1$ V. Circles: $V_{DS} = 0.6$ V. Triangles: $V_{DS} = 1.1$ V.

The calculated drain and gate temperatures at all the bias points are shown in Fig. 3. The observed influence of the gate temperature on the final values of the noise parameters was very weak. In fact, a modification of more than 30% in T_G makes nearly no difference in the final noise parameters at any of the measured bias points, with the only exception of the last two ones at $V_{DS} = 1.1$ V. The dependence of the drain temperature on the bias current is strongly influenced by the values adopted by the drain to source voltage. Indeed, T_D decreases with the drain current for drain voltages of 0.1 V and 0.6 V. This performance has also been measured at similar bias conditions in commercial GaAs-based MODFETs [8]. P factor of Pucel model, which accounts for the drain current fluctuations, can also exhibit an increase as the drain current decreases [9].

IV. Discussion and Concluding Remarks

The decrease of the drain temperature as a function of the drain current may be justified by assuming the existence of shot noise. It is well known that full shot noise appears in a biased Schottky diode, where the carriers must overcome a potential barrier [10], [11]. Similar conditions are found in a channel of a MODFET when the channel is not fully open, since under these circumstances a net flow of carriers exists and these carriers must cross a

barrier located in the gate to drain path of the channel. This barrier has been measured [12] and simulated [13] with Monte Carlo techniques in different HEMTs, and could act like the space charge zone of a Schottky diode in terms of noise behavior. According to the Viola–Mattauch model, shot noise makes the diode noise temperature to decrease as a function of the bias current from the physical temperature at equilibrium conditions to nearly half this value at moderate currents. The effects of shot noise in the noise temperature of a diode are hidden when the carrier heating is strong enough and other high field noise mechanisms become important. This should also be expected in a MODFET. In fact, Fig. 3 shows that no decrease of T_D exists at the highest drain voltage, $V_{DS} = 1.1$ V, and at currents high enough to avoid strong reverse gate to source voltages which would make Pospieszalski model inaccurate due to gate leakage problems. The main difference between the performance of T_D in a MODFET and that of the noise temperature in a Schottky diode arises from the fact that in the MODFET it is possible to have strong carrier heating with nearly no drain current, and therefore at low currents T_D can reach values noticeably higher than the device physical temperature. In fact, when the gate current remains negligible and the electric field is not high enough to allow for intervalley transitions and real space transfer, electron heating dominates the channel noise performance [14], [15].

In summary, the comparison between the measurements and simulations reported here has shown that Pospieszalsky model is able to accurately predict the noise behavior of submicron lattice matched InP-based MODFETs even under very extreme bias conditions, such as those corresponding to transconductances of less than 10% of the maximum transconductance achieved by the device. As a result, we conclude that the neglection of correlations between the gate and drain noise sources is also a valid assumption at very low currents and drain voltages.

The behavior of T_D as a function of the drain current observed in this work is noticeably more sophisticated than that previously reported, where a systematic increase of T_D with drain current has always been found. Simulations and measurements of the noise parameters in a fairly wide range of bias points have shown us that T_D can decrease as the current increases. This observed decrease is found at low values of the drain voltage and may be explained in terms of the existence of shot noise at the gate to drain path of the channel. This performance could be exploited to optimize the device bias point for low noise operation.

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