Ka-Band High-Power and Driver MMIC Amplifiers Using GaAs PHEMTs and Coplanar Waveguides

A. Bessemoulin, *Member, IEEE*, H. Massler, A. Hülsmann, and M. Schlechtweg, *Member, IEEE*

***Abstract*—We report the design and fabrication of compact 2- and 3-stage coplanar (CPW) microwave monolithic integrated circuit (MMIC) amplifiers having high output power at Ka-band. Based on a 0.15-μm gate length GaAs PHEMT process, a two-stage MMIC driver amplifier has demonstrated at 35 GHz, a linear gain of 11 dB, an output power at 1 dB gain compression $P_{-1\ \mathrm{dB}}$ of 350 mW, and a saturated output power P_{sat} greater than 500 mW. For the same frequency, the high-power CPW 2-stage amplifier achieved a linear gain of 9.5 dB, with $P_{-1\ \mathrm{dB}} = 725$ mW and more than 1 W of saturated output power. Additional thermal management resulted in an increased performance, namely, 10.4 dB linear gain, $P_{-1\ \mathrm{dB}} = 950$ mW and $P_{\mathrm{sat}} = 1.2$ W. To our knowledge, those are the highest output powers ever reported at Ka-band for any uniplanar MMIC.**

***Index Terms*—Coplanar waveguides, GaAs PHEMT, MMIC power amplifiers.**

I. INTRODUCTION

IN CONTRAST to microstrip amplifiers that have demonstrated high output power and good thermal properties (e.g., [1], [2]), the coplanar technology still remains unused for power applications. The poor power handling capabilities of coplanar (CPW) result from the absence of via-holes and close backside process, ensuring the thermal dissipation in microstrip circuits. However, with the emerging packaging techniques like flip-chip, the coplanar technology becomes an advantageous and cost-effective solution for microwave monolithic integrated circuit (MMIC) fabrication [3]. Moreover, in combination with attached thermal bumps, the performance of coplanar power MMIC is significantly improved [4]. In order to advance the state-of-the-art in CPW MMIC design and to address the need of a unified technology in modern packaged modules, millimeter-wave Ka-band compact 2- and 3-stage power amplifiers with high output power were developed. They demonstrated the potential of the coplanar technology to realize lower cost power MMIC devices and circuits for local multipoint and multipoint video distribution system (LMDS and MVDS) applications.

II. MMIC PROCESS AND DESIGN

The coplanar MMIC amplifiers were fabricated using our double δ-doped AlGaAs/InGaAs/GaAs PHEMT process with 0.15-μm T gates on 4″ wafers. The characteristics are a peak RF

Manuscript received August 2, 2000; revised September 27, 2000. This work was supported by the German Ministries for Defense (BMVg), and Education and Research (BMBF).

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Publisher Item Identifier S 1051-8207(00)11565-X.

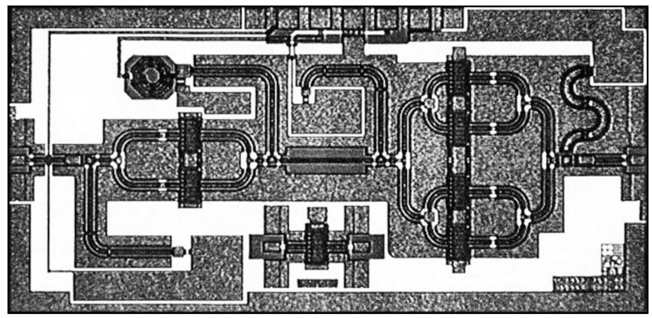

Fig. 1. Photograph of the coplanar driver amplifier (1.45×2.95 mm^2).

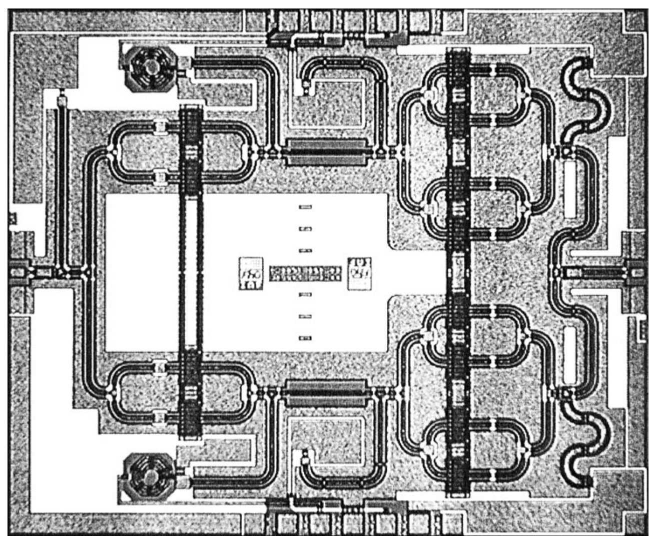

Fig. 2. Photograph of the 2-stage high-power coplanar amplifier (2.45×2.95 mm^2).

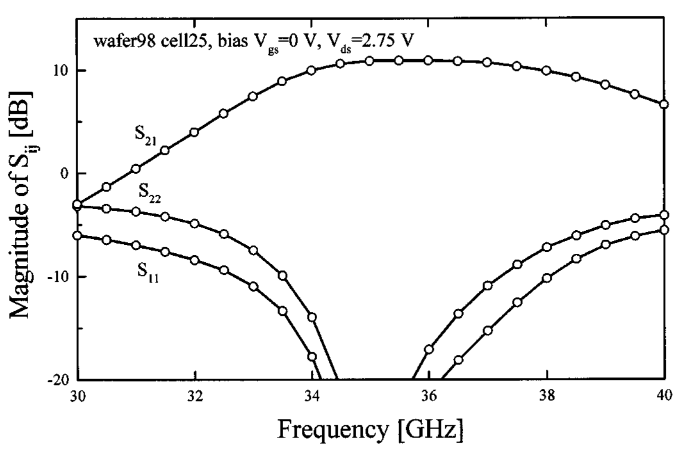

Fig. 3. On-wafer measured small signal gain, input and output return losses versus frequency of the CPW driver amplifier.

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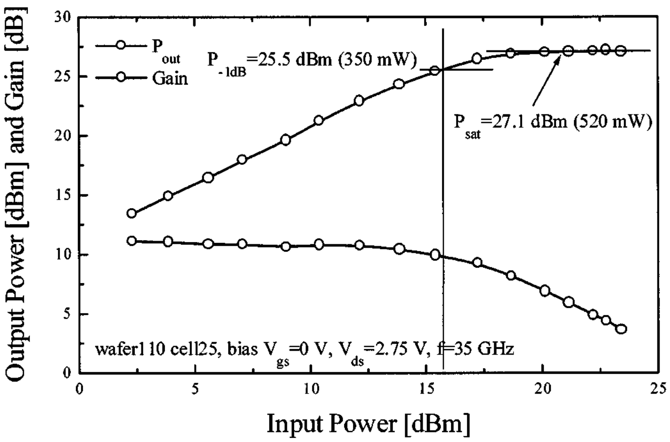

Fig. 4. On-wafer measured output power and gain versus input power of the CPW driver amplifier at 35 GHz.

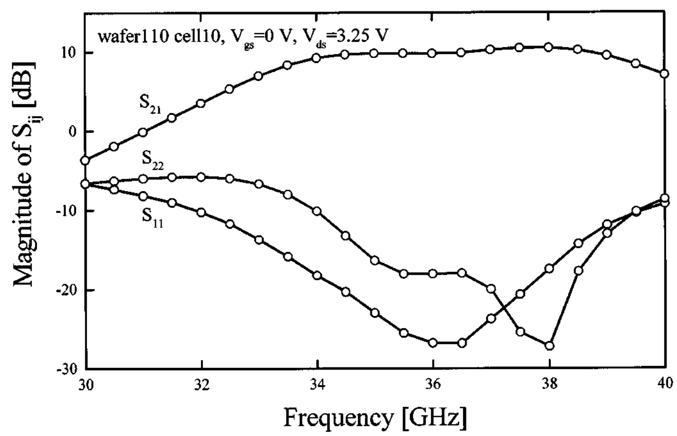

Fig. 5. On-wafer measured small signal gain, input and output return losses versus frequency of the coplanar 2-stage HPA.

TABLE I
TYPICAL ON-WAFER CHARACTERISTICS OF THE COPLANAR POWER AMPLIFIERS AT 35 GHz ($V_{ds} = 3.25$ V$^{(HPA)}$, $V_{gs} = 0.0$ V, T_a =25 °C)

	G_{lin} [dB]	P_{-1dB} [dBm]	P_{sat} [dBm]	PAE_{max}	Chip size (mm^2)
2-stage DPA	11	25.5	27.1	14 %	1.45 × 2.95
2-stage HPA	9.5	28.6	30.1	12 %	2.45 × 2.95
3-stage HPA	13.5	27.5	30	12 %	2.45 × 2.95

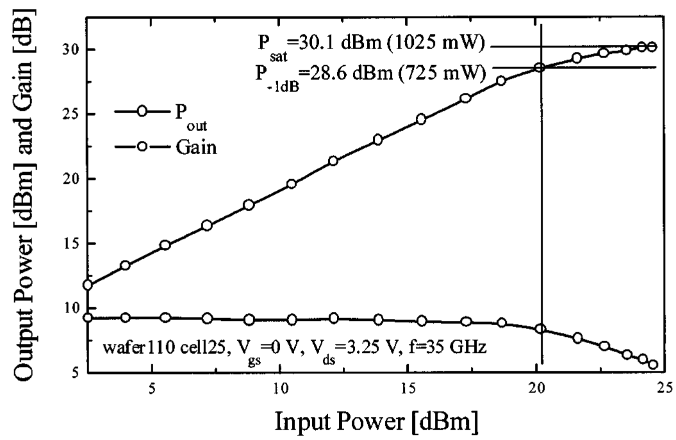

Fig. 6. On-wafer measured output power and gain versus input power of the coplanar 2-stage HPA at 35 GHz.

transconductance g_m of 810 mS/mm, a maximum current density $I_{d,\max}$ of 900 mA/mm, and $BV_{gd} = 5.0$ V off-state breakdown voltage. The MMICs are realized on 625-μm thick substrates and incorporate 50 $\Omega/\square$ NiCr resistors and 225 pF/mm^2 SiN capacitors.

The driver amplifier (DPA) consists of two 8×60 μm devices, driving four identical cells for an output gate periphery of 1.92 mm, and a chip size of 1.45×2.95 mm^2, as depicted in Fig. 1. The two-stage (Fig. 2) and three-stage high-power amplifiers (HPAs) are based on a similar topology, with output gate peripheries of 3.84 mm and chip sizes of 2.45×2.95 mm^2. Based on the load line approach, rigorous design and layout methods including thermal aspects were considered in the optimization of gain, bandwidth, and output power. The matching networks were realized with capacitively loaded and coupled transmission lines enabling flexible impedance matching and size reduction [5]. Large on-chip bypassing capacitors and resistive loading, combined with general and loop stability analysis, were used to prevent low frequency and odd-mode oscillations, ensuring the unconditional stability of the MMICs.

III. POWER AMPLIFIERS PERFORMANCE

The MMIC amplifiers were tested on-wafer under continuous wave (CW) operation at ambient temperature, although for GaAs CPW MMIC, this configuration is one of the worst cases from the thermal point of view. Indeed, the heat generated in the channel region of the devices must travel through a 625-μm substrate having a high thermal resistance. Fig. 3 shows the measured small signal gain and input/output return losses of the driver amplifier. At 35 GHz and for $V_{ds} = 2.75$ V, the small signal gain is greater than 11 dB, with input and output return losses below −35 dB. Fig. 4 shows the output power and gain versus input power at the same frequency, measured with our vector-corrected power measurement system [6]. The output power is 25.5 dBm at 1 dB gain compression (350 mW) and greater than 500 mW in saturation (27.1 dBm). For the Ka-band 2-stage CPW HPA, the measured small-signal S-parameters are depicted in Fig. 5. The HPA has a gain greater than 9.5 dB from 34 to 38 GHz, as well as a very good output matching for an unbalanced topology. Fig. 6 shows the measured output power versus input power at 35 GHz. At $V_{ds} = 3.25$ V and for a total supply current of 1.9 A, the output power is 28.6 dBm at 1 dB gain compression (725 mW) and exceeds 1 W in saturation (30.1 dBm) with 6 dB associated gain. It is worth mentioning that thick wafers, and CW RF measurement result in a relatively high channel temperature T_{ch} of the devices, estimated by three-dimensional (3-D) thermal simulations and measurements to approximately 85°C [4], [7], limiting the intrinsic electrical performance (i.e., reduced g_m and I_d) and reliability. However, on-wafer operation tests, under continuous RF drive for 100 h showed no degradation in performance. The RF functional yield over a 4″ wafer, using $P_{\rm sat} > 30$ dBm as screening criteria, was 88%. The characteristics of the CPW power amplifiers are summarized in Table I.

In packaged solutions, the chip mounting conditions differ considerably from the on-wafer case and additional thermal management has to be performed. In order to verify the benefit

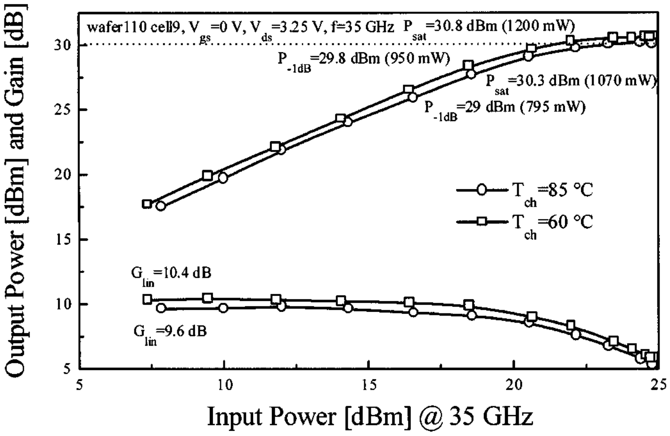

Fig. 7. On-wafer power measurements of the 35 GHz CPW 2-stage HPA with a thermally controlled chuck for device temperatures T_{ch} of 85 °C and 60 °C.

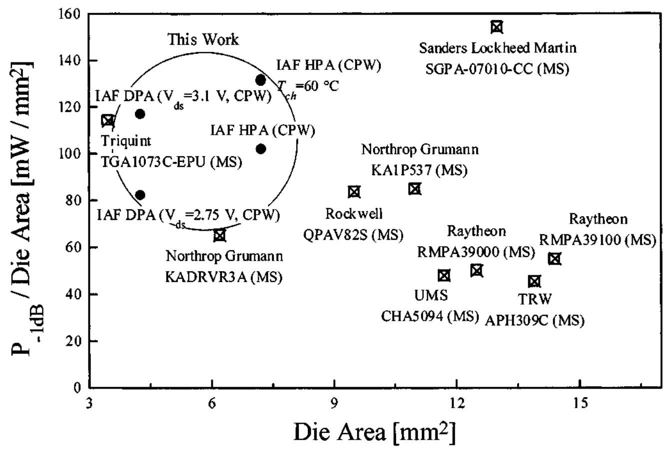

Fig. 8. State-of-the-art Ka-band high-power MMIC amplifiers in microstrip (MS) or coplanar (CPW) technology [2].

of using either a thinned or a flipped MMIC die, a thermally controlled chuck is used to reduce the temperature profile of the FET devices in the HPA by 25 °C (let $T_{ch} \approx 60$ °C). This thermal management is equivalent to that of a chip that is either thinned to 50 μm and placed on aluminum nitride (AlN), or flipped on an AlN carrier with appropriate thermal bumps attached to the source islands [7]. Fig. 7 shows the output power and gain in such a measurement setup. The self-heating reduction clearly shows a significant increased performance, with a linear gain of 10.4 dB, $P_{-1\ \mathrm{dB}} = 950$ mW and $P_{\mathrm{sat}} = 1.2$ W.

IV. Conclusion

Ka-band amplifiers having state-of-the-art output power for coplanar MMICs were fabricated. Thermal management, representative of realistic package mounting conditions, improving the overall performance, was also discussed. With more than 1 W output power, these compact monolithic HPAs are competitive to microstrip power amplifiers (Fig. 8), and demonstrated the potential of coplanar technology for high-power applications.

Acknowledgment

The authors would like to acknowledge the contributions of Dr. M. Demmler for the power measurement system development, and Prof. G. Weimann for his encouragement.

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