# 2-Bit MEMS Distributed X-Band Phase Shifters

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***Abstract*—A wideband distributed coplanar-waveguide (CPW) phase shifter has been developed for X-band operation. The design is based on the distributed MEMS transmission line (DMTL) loaded with MEMS bridges and MIM capacitors. A 2-bit distributed phase shifter was fabricated on a 500-$\mu$m quartz substrate, and achieved a true-time delay operation from 1 to 20 GHz with a reflection coefficient less than −11 dB from 2 to 20 GHz and above. Insertion loss is dominated by a low-$Q$ MIM capacitor (14 at 10 GHz) and the effect of this $Q$ is shown. Increasing the MIM capacitor $Q$ will result in an excellent 2-bit phase shifter with wideband performance at X-band frequencies.**

***Index Terms*—Distributed circuit, MEMS, phase shifter.**

## I. Introduction

THE 1- and 2-bit distributed phase shifters presented here consist of a high impedance line (100 Ω) capacitively loaded by the periodic placement [1], [2] of series MEMS bridges and MIM capacitors. The distributed loading lowers unloaded impedance from 100 Ω to 60 Ω. By applying a bias voltage between the MEMS bridge and coplanar-waveguide (CPW) center conductor, the MEMS bridge capacitance increases, thus increasing distributed loading and further loading transmission line impedance from 60 Ω to 44 Ω.

By changing line impedance, phase velocity changes which results in a phase shift. The phase shift of this slow wave structure can be calculated to be

$$\Delta\phi = \omega\sqrt{L_t C_t}\left(\sqrt{1+\frac{C_{lu}}{sC_t}}-\sqrt{1+\frac{C_{ld}}{sC_t}}\right) = \frac{\omega Z_o\sqrt{\epsilon_{r,\text{eff}}}}{c}\left(\frac{1}{Z_{lu}}-\frac{1}{Z_{ld}}\right) \quad \text{rad/m} \qquad (1)$$

where $Z_{lu}$ and $Z_{ld}$ are the distributed MEMS transmission line (DMTL) characteristic impedances for the low and high MEMS bridge capacitance states, and $L_t$ and $C_t$ are the unloaded CPW line inductance and capacitance, respectively. $Z_o$ is the characteristic impedance of the unloaded CPW line, $c/\sqrt{\epsilon_{r,\text{eff}}}$ is the guided velocity of the unloaded CPW line.

The "digital" distributed MEMS phase shifter is shown in Fig. 1 together with the equivalent circuit model of a single period, $s$. The load capacitance seen by the line is the series combination of the MEMS bridge capacitance $(C_b)$ and the total lumped capacitance $(C_s)$ and is

$$C_l = C_s C_b/(C_b + C_s). \qquad (2)$$

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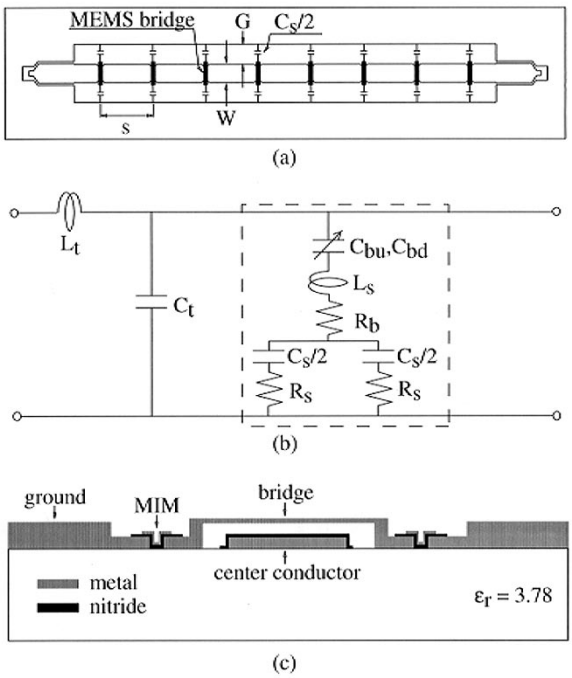


Fig. 1. (a) CPW phase shifter with MEMS bridges and MIM capacitors. (b) Distributed lumped model. (c) Cross section sketch of the MEMS bridge.

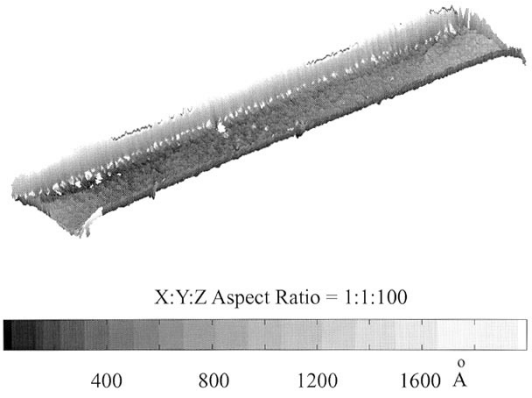


Fig. 2. Light interferometer measurement of a typical MEMS bridge.

When the MEMS bridge is in the up-state position, the bridge capacitance $(C_{bu})$ is, in the limit, much smaller than $C_s$ and the effective capacitance seen by the line, is $C_{lu} \approx C_{bu}$. When a bias is applied on the line and the MEMS bridge is in the down-state position, the bridge capacitance $(C_{bd})$ increases by a factor of 40–80 and becomes much larger than $C_s$, thereby resulting in a load capacitance of $C_{ld} = C_s$. The distributed capacitance can therefore be "discretely" controlled by the independent choice of $C_{bu}$ and $C_s$.

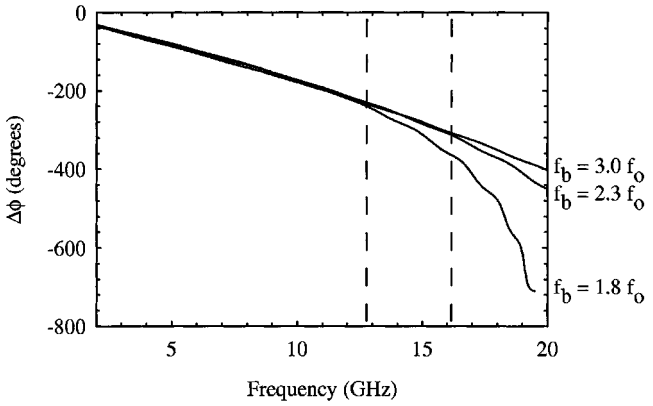


Fig. 3. Modeled comparisons of phase linearity for different Bragg frequencies ($f_o = 10$ GHz).

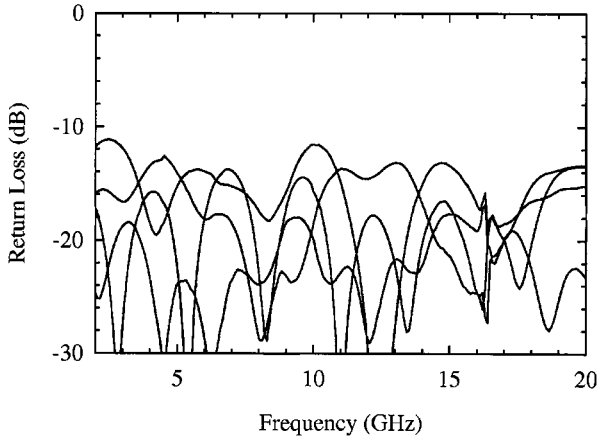


Fig. 4. Return loss measurements of a 2-bit phase shifter (0/90/180/270°) in all four states.

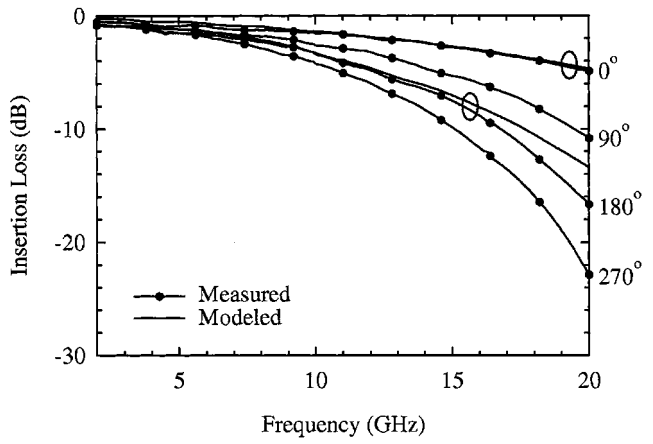


Fig. 5. Insertion loss measurements and modeling of a 2-bit phase shifter (0/90/180/270°) in all four states.

## II. Design of the MEMS Phase Shifter

Phase shift is determined by the impedance change of the DMTL, which also determines the reflection coefficient of the phase shifter. Equation (1) shows that a wider swing in impedance results in more phase shift, but at the expense of higher levels of return loss. In fact, twice as much phase shift is obtainable if the maximum allowable reflection coefficient is −10 dB rather than −15 dB. But because two phase shifter sections (90° and 180°) will be cascaded to result in a 2-bit phase shifter, the maximum reflection coefficient is chosen to be −15 dB such that the cascaded structure will be less than −10 dB [1].

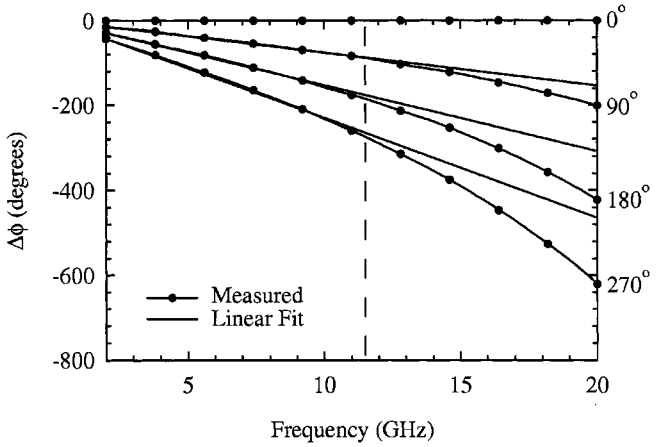


Fig. 6. Phase shift measurements of a 2-bit phase shifter (0/87/182/270° at 11.4 GHz). Linear fit lines are drawn to show phase shift linearity.

## III. Fabrication

The DMTL is designed for 10-GHz operation and is composed of a 900-$\mu$m wide ($W + 2G$) CPW line with 300 $\mu$m center ($W$) conductor. The CPW line is wide for reduced unloaded line loss. The 180° DMTL is composed of 16 MEMS bridges at a spacing of 906 $\mu$m. The bridges are 350 $\mu$m long, 60 $\mu$m wide and suspended at a height of 1.0 $\mu$m above the substrate. A 2000 Å nitride layer is used as the insulating dielectric between the CPW center conductor and the MEMS bridge. The conductor under the MEMS bridge is 8000 Å thick. The CPW center conductor and ground plane are electroplated to 4.5 $\mu$m thick except underneath the MEMS bridge.

Design values for MEMS capacitance ($C_{bu}$) and MIM capacitance ($C_s$) are 138 and 210 fF, respectively. Following (2), the distributed $C_{lu}$ (83 fF) loads the 100 Ω line to 60 Ω, and the distributed $C_{ld}$ (182 fF) loads the line to 44 Ω.

The largest challenge to fabrication is the MEMS bridge because without controlling bulk and gradient stress, the released bridge will easily curl or bow 5 $\mu$m or more. Furthermore, the design is highly dependent on a repeatable up-state MEMS capacitance which is suspended at a low height (1–2 $\mu$m) so that it can be pulled-down electrostatically using 30–50 V.

A remarkably flat MEMS bridge was achieved using a 6000 Å thick metal suspended 1.0 $\mu$m above the insulating nitride. A light interferometer measurement of a typical released bridge (Fig. 2) shows bowing over the long dimension (350 $\mu$m) is less than 2000 Å and curling over the narrow dimension (60 $\mu$m) is less than 1000 Å. Fabrication yield of these bridges with these height, curling, and bowing tolerances is 97–100%. The pull-down voltage of the MEMS bridge alone is 13 V (extracted values: spring constant, $k = 73$ N/m, residual stress, $\sigma = 72$ MPa [3]), and around 60 V with the series MIM capacitor to ground. The MEMS bridges pull down conformally with bias and snap back to their original height without deformation

over numerous actuations, as can be observed in phase measurements. Switching speed has not yet been measured.

## IV. Effect of Bragg Frequency

The Bragg frequency is a cutoff frequency of distributed structures when the guided wavelength approaches the distributed periodic spacing. The linearity of phase shift will increase with Bragg frequency at the expense of smaller separations, $s$, between the MEMS bridges.

It has been found through modeling that the Bragg frequency must be at least 2.3–3 times that of the design frequency, $f_o$, if the maximum reflection coefficient allowable is $<-15$ dB and loaded impedances are 60 and 42 $\Omega$.

Lower Bragg frequency designs are possible if the down-state impedance is increased (Fig. 3). This is necessary in order to keep the reflection coefficient $<-15$ dB at the design frequency, $f_o$ (10 GHz). For example, if the Bragg frequency is $2.3f_o$, and the down-state impedance is 45 $\Omega$, then phase shift is linear to 16 GHz. The phase shift is nonlinear above 16 GHz and the ripple in the phase is caused by the reflection coefficient being more than $-13$ dB. If the Bragg frequency is $1.8f_o$, and the down-state impedance is 46 $\Omega$, then phase shift is linear to only 13 GHz.

The $3.0f_o$ frequency was selected because it gave a reflection coefficient $<-15$ dB up to 20 GHz, nearly linear phase shift to 20 GHz, and a reasonable value of the loading capacitance and spacing between the MEMS bridges.

## V. 2-bit Measurements

The 2-bit design consists of a 90°, 8 MEMS bridge section, cascaded with a 180°, 16 MEMS bridge section. The 2-bit phase shifter is 21.7 mm long. A large MIM capacitor is used in the CPW center conductor between the two bits. The phase shifter is biased through the left and right ports. For 0° the left and right ports are unbiased, for 90° the left port is biased, for 180° the right port is biased, and finally, for 270° both ports are biased.

Measured performance of a 2-bit, 0/90/180/270°, 24 bridge DMTL phase shifter is shown in Figs. 4–6. The DMTL results in excellent return loss ($<-11$ dB) from 2 to 20 GHz and above in all four states. The measured phase shift is 0/87/182/270 degrees at 11.4 GHz ($\pm 3°$ error). An even number of MEMS sections should be used for the 180° case so that the 90° case results in an integer number of MEMS sections. Using (1), 16 and 18 sections result in 163° and 183° of phase shift, respectively, at 10 GHz. Since 16 sections were used, it is expected that 0/90/180/270 degrees of phase shift occurs at a frequency higher than 10 GHz, and in this case, occurs at 11.4 GHz.

Measurement and modeling of insertion loss (Fig. 5) shows the MIM capacitors becoming frequency dependent above 14 GHz. This is clear because for the 0° case, when all MEMS bridges are in the up-state, and the MIM capacitor has a small effect on loading, modeling matches measurements. However, for the 180° case, when 2/3 of MEMS bridges are down and loading is dominated by MIM capacitance, modeling differs from measurements above 14 GHz. Phase shift (Fig. 6) is nonlinear above 11 GHz also because the MIM capacitors are frequency dependent. The cause of this capacitance change versus frequency is currently under investigation.

The insertion loss per section due to the MEMS bridge and MIM resistance can be modeled by (3) [3], [5]. Measured test structures of the MIM capacitors have a $Q$ of 14 at 10 GHz or an equivalent $R_s$ of 10.8 $\Omega$ at 10 GHz. This low $Q$ is due mostly to a very thin (500 Å of Au) metallization layer. Since the metallization is much less than a skin depth, $R_s$ is constant

$$\alpha \approx \frac{R_s Z_l C_l{}^2 \omega^2}{4}. \tag{3}$$

Because the MIM losses dominate the insertion loss of these phase shifters, much better performance can be achieved by simply increasing the MIM $Q$. This can be done by increasing the MIM metallization thickness. The expected insertion loss at 10 GHz is 0.9 dB for a 180° phase shifter with a MIM capacitor $Q = 60$.

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