

A Compact Dual-Polarized 8.51-GHz Rectenna for High-Voltage (50 V) Actuator Applications

Larry W. Epp, *Member, IEEE*, Abdur R. Khan, Hugh K. Smith, and R. Peter Smith

Abstract—This paper describes a dual-polarized rectenna capable of producing a 50-V output voltage that can be used for driving mechanical actuators. This study demonstrates a circuit topology that allows the output of multiple rectenna elements to be combined in order to step up the output voltage. In this paper, an independent rectifying circuit is used for each of two orthogonal polarizations. By proper combination, the output voltage is doubled over that of the single polarization case. Such panels are being explored for use on the next-generation space telescope to eliminate wiring between actuators and provide for true mechanical isolation.

Index Terms—Actuators, free-space power combining and rectification, microstrip patch, rectenna.

I. INTRODUCTION

RECTENNA is an antenna that captures and converts RF or microwave power to dc power. It is useful as the receiving terminal of a power transmission system where dc power needs to be delivered to a load, through free space, where physical transmission lines are not feasible. It is also useful in applications where dc power needs to be distributed to a large number of load elements that are distributed spatially. The power distribution is achieved by the dispersive nature of microwave energy in space, eliminating the need for physical interconnects to individual load elements.

The goal of the rectenna is to convert microwave power into dc power. Essentially, this is the opposite process of modern grid amplifier designs, which convert dc power to microwave power. Analogous to grid amplifiers, a rectenna can use the dispersive nature of the microwave power to combine the power from many elements, which are spatially separated by the element spacing of the array or panel. Therefore, the effective area of the entire rectenna panel determines the total power the panel receives.

A potential application for rectennas involves the transmission of power to actuators, which control the position of individual surfaces of a space-born optical reflector. The work presented in this paper was initiated in part for use with microwave-driven smart material actuators for control of the next-generation space telescope (NGST), which has been proposed by Choi, NASA Langley, Hampton, VA [1]. The use of rectennas simplifies the design of the multisurface reflector by eliminating the

need of a wiring harness to distribute power to the individual actuators. Furthermore, the rectennas could also provide control signals to each actuator by proper modulation of the incident microwave beam.

The actuators required 50 V for operation, therefore, the individual rectennas had to be designed to provide this voltage in the most efficient manner. Tradeoffs include physical rectenna size, diode availability, diode characteristics (breakdown voltage, power handling), efficiency of capturing the microwave energy by the antenna, efficiency of the rectification process, and frequency of the incident power. Of course, these are not independent parameters. Due to the availability of high power *X*-band sources at the Jet Propulsion Laboratory (JPL), Pasadena, CA, and the fact that spacecraft typically use traveling-wave tube amplifiers (TWTA's) sources at *X*-band, it was decided that the frequency of the incident microwave power would be 8.51 GHz.

II. ANTENNA ELEMENT DESIGN

Most previous rectenna designs have employed dipole antennas [2]–[6] and received a single linear polarization. A thin-film printed-circuit dipole rectenna design was proposed initially by Brown [3] and had simple dc removal. This single polarization design minimized the thermal path between the diodes and outer surface. However, the printed capacitors of these thin-film designs restricted their tunability as compared to Brown's original “bar-type” rectenna element [2], [3]. In practice, the “bar-type” rectennas have been demonstrated by Dickinson, in the 1975 JPL Goldstone microwave transmission demonstration, to have efficiencies as high as 82.5% [7], [8].

For dual polarization the extension of the thin-film dipole design quickly encounters significant obstacles to successful implementation. A separate layer, one layer for each polarization, is required for each polarization. Electromagnetic interaction between the dc collection lines, parallel to the dipole on the orthogonal layer, can compromise the rectenna performance. Having one dipole layer “buried” beneath the other also has serious thermal problems.

In addition, the fabrication process of the dual linear dipole design can be quite challenging since diodes and chip capacitors may be potentially buried between layers of foam and/or polyimide film [6]. To avoid this, Alden and Ohno [9] developed a single foreplane design. However, the dipole rectenna designs, in general, suffer from the problem that the feed circuitry and the antenna (dipole) are tightly coupled. The twin-lead transmission-line impedance is related to the dipole impedance, therefore, posing a constraint on the design. Also inherent with a

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L. W. Epp, A. R. Khan, and R. P. Smith are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA.

H. K. Smith was with the Jet Propulsion Laboratory. He is now with Cellular Subscriber Sector Research Laboratory, Motorola, Harvard, IL 60033 USA.

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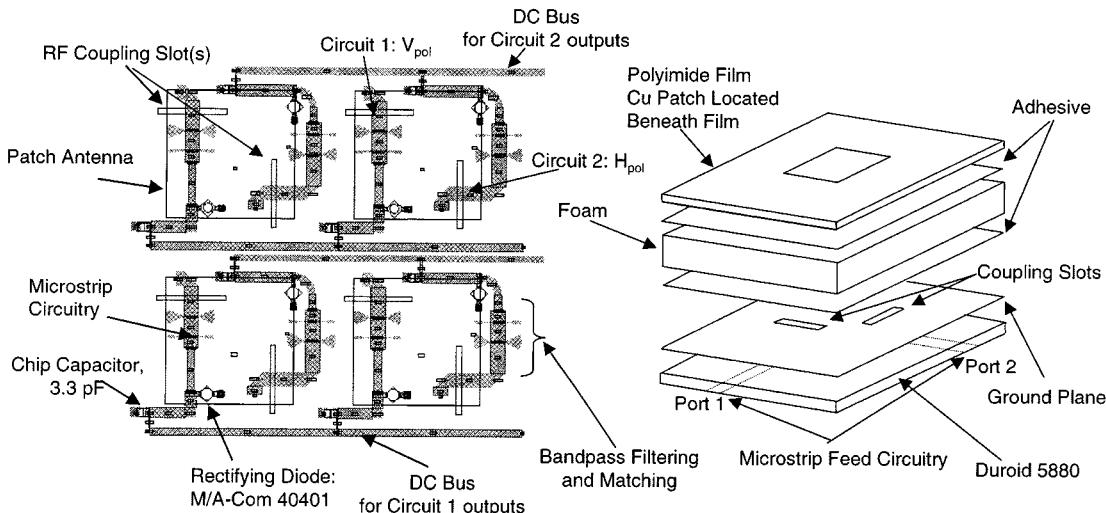


Fig. 1. Foam supported dual-polarized aperture-coupled patch rectenna.

dipole design is the fact the feed circuitry was exposed to the outside world and, therefore, parasitic radiation from these feed lines including harmonic radiation (generated by the diodes) could be an issue.

For dual-polarization needs, a microstrip patch design could potentially alleviate many of the problems mentioned above. The advantage of dual-polarization is twofold: it potentially doubles the receive power per element area and makes the rectenna capable of receiving either dual linear or a single circular polarization. The latter ability to receive circular polarization makes the rectenna panel more suitable for applications such as a circling airplane platform [2], [10].

An aperture-coupled microstrip patch relies on an aperture, or coupling slot, to couple electromagnetic energy from a feed circuit to the microstrip patch antenna, as shown in Fig. 1. In this configuration, the antenna and microstrip feed circuit are isolated from one another. This also allows the diode circuitry to be located behind the ground plane containing the coupling apertures. This ground plane, which separates the patch antenna and feed circuit, protects the feed circuitry from the incident RF energy. As a result, the incident RF energy will not be coupled to the dc lines that collect the output power.

The ground plane also prevents the harmonics, which are generated by the diodes, from radiating back toward the incident wave. A microstrip-line filter is used to prevent radiation back through the aperture feed. Due to the potential interference of generated harmonics, this concept of separating the receiving element and rectifying circuitry to prevent harmonic radiation has also been explored by other researchers [11] using a circular patch and single diode. Other researchers have explored the use of a frequency selective surface [12].

A. Antenna

As shown in Fig. 1, the patch is supported above the ground plane by a lightweight foam support. This foam has a relative dielectric constant of 1.07, which will help reduce the possibility of surface-wave modes that may limit the microstrip patch array performance. In particular, this configuration was first discussed in 1988 by Zürcher in his strip slot foam inverted patch

(SSFIP) concept [13]. Just as important, the ground plane provides a good thermal sink for the diodes with via connections to the ground plane. Recently, microstrip patch antennas have become increasingly popular in rectenna development [10]–[12], [14]–[16] at 2.45 and 35 GHz.

Aperture coupled microstrip patch antennas were first introduced in 1985 by Pozar [17]. In December 1986, Pozar presented a reciprocity-based method for the analysis of aperture-coupled microstrip patch antennas [18]. Other researchers have offered solutions to the single-aperture coupled-microstrip patch antenna using modal or cavity methods [19], [20]. More, recently, Rostan *et al.* have employed Pozar's methods in designing dual-polarized aperture-coupled microstrip patch antennas. These patch antennas, used for synthetic aperture radar (SAR) and satellite reception antennas [21]–[24] were the basis for the design used here.

B. Construction Details of the Aperture-Coupled Microstrip Patch Antenna

The microstrip patch antennas constructed consisted of Rohacell 51 ($\epsilon_r = 1.07$) as the foam spacer, RT/duroid 5880 (0.64-mm thick, $\epsilon_r = 2.2$, copper thickness of 17.5 μm) as the microwave substrate, and Sheldahl's Novaclad G2200 (50- μm thick, $\epsilon_r = 3.3$, copper thickness of 35 μm), which is a copper-clad polyimide film, on which the microstrip patch antenna was etched. Method-of-moments solutions indicate that for every 25- μm change in the foam spacers thickness, a 10-MHz change in resonant frequency will occur. To insure accurate thickness of the foam used, a method was developed to precompress the thickness of the Rohacell to 0.89 mm by using a compression fixture and an oven. A piece of 1.02-mm-thick Rohacell foam is placed in a compression fixture, in which the foam is then preloaded (placed in compression). The entire assembly is then placed inside an oven that is heated above 191 °C, the temperature at which the Rohacell loses its compressive strength. Using 0.89-mm shims sets the final thickness.

Typical solder reflow temperatures are above 205 °C and the Rohacell begins to expand at 191 °C. Therefore, if the Rohacell

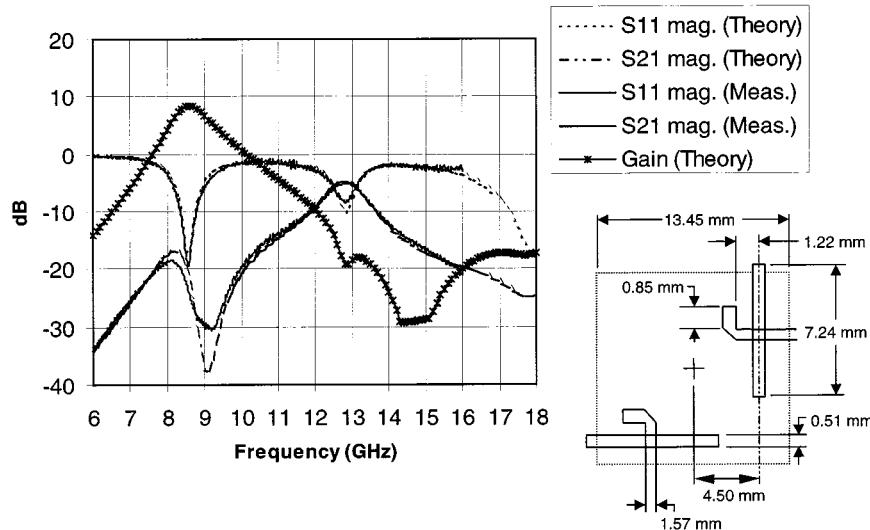


Fig. 2. Comparison of theoretical and measured values for the S -parameters of the dual-polarized patch. Final patch dimensions as given. The calculated results are shown over the entire frequency range, the measurements end at 16 GHz.

is bonded to the RT/duroid prior to the solder reflow process and then exposed to the solder reflow, the foam severely distorts, destroying the rectenna panel. An alternative is to use a room-temperature vulcanizing silicone rubber adhesive, such as Dow Corning 3140 RTV. Using the 3140 RTV Coating allows for components to be wave soldered to the RT/duroid, then the RT/duroid can be bonded to the Rohacell foam. The actual fabrication process uses a Maher bar (grooved bar) to apply a uniform coat of adhesive, thereby insuring repeatability in the fabrication process.

C. Patch Measurement

The goal of the microstrip patch design is to present a low return loss (S_{11} , S_{22}) at 8.51 GHz. It is also desired to have isolation between the two ports (a low S_{21} , S_{12}) of Fig. 1. The scattering parameter data and final patch dimensions are shown in Fig. 2. The measured return loss in Fig. 2 is shown to exceed 18 dB (only port one is shown due to symmetry) at 8.51 GHz.

The measured resonance frequency for optimum return loss was 8.565 GHz. The simulations indicate a worst-case coupling between the two ports greater than -20 dB, while actual measurements were slightly greater than this value. Measurements gave a worst-case coupling between ports of -18.5 dB (at 8.07 GHz) for all frequencies below 10 GHz. To correct for the foam compression, the relative permittivity was increased by the ratio of compressed-to-uncompressed height to $\epsilon_r = 1.2$.

Fig. 2 also shows the predicted gain and scattering parameters up to 18 GHz. This allows the simulated parameters to be shown at the first harmonic of the operating frequency at 17.02 GHz. The measured results stop at 16 GHz where the microstrip line becomes overmoded. (Note the increase in measurement error for S_{11} , as compared to the predicted value, at 16 GHz.) The predicted patch gain at 8.51 GHz is 8.4 dB. At the second harmonic frequency, the gain is less than -17 dB, indicating that the harmonic radiation is not radiated back through the coupling aperture and toward the signal source. The additional low-pass filter,

discussed below, provides further suppression of unwanted harmonic radiation.

III. DIODE MEASUREMENT AND MODELING

A. Diode Background

Most rectenna designs have followed Brown in using a single diode in a clamping circuit configuration rather than a traditional multiple-diode rectifying circuit. At microwave frequencies, these rectenna circuits are highly nonlinear and difficult to design based upon purely analytic equations. Commercially available harmonic-balance simulators are useful, but necessarily limited by the accuracy of the diode model at large signal. Previous works that have developed equivalent circuits for the diode have been validated with experimental results [4], [12], [25].

Since optimal performance of a rectifier requires ideal tuning at harmonics as well as the fundamental frequency, parameters of any diode model must be known at the harmonic frequencies as well as at the fundamental. Experimental large-signal measurements provide a method of extracting and verifying diode models and of searching for maximum efficiency. Since the tuning done here is purely empirical, there is no guarantee that the results actually represent the best that could be achieved with a given device. However, the inverse is true—a properly designed microstrip circuit, especially with extra components (e.g., chip caps, etc.) should certainly do as well as the empirically tuned results presented here. It was also found that optimization of efficiency using nonlinear simulations was time consuming and, of course, inaccurate until diode models were extracted.

B. Diode Measurement

For the purposes of this effort, diodes readily available in a packaged format with large breakdown were chosen. The diode used is the commercially available M/A-Com 40401 Schottky

	Vf1 (V)	Vf2 (V)	Vf3 (V)	Ir1 (A)	Ct (pF)	Vb (V)	Rs1 (Ω)	Rs2 (Ω)
Stimulus	.01mA	.10mA	1.0mA	1.0V	0.0V	.01mA	4.5-5.5mA	9.5-10.5mA
Model	.517	.611	.710	3.0E-11	.229	9.6	15.5	11.5

Fig. 3. Simulation data for M/A-Com 40401 Schottky diodes.

	Vf1 (V)	Vf2 (V)	Vf3 (V)	Ir1 (A)	Ct (pF)	Vb (V)	Rs1 (Ω)	Rs2 (Ω)
Stimulus	.01mA	.10mA	1.0mA	1.0V	0.0V	.01mA	4.5-5.5mA	9.5-10.5mA
Diode#1	.566	.635	.714	2.8E-11	.264	8.18	15.2	11.2
Diode#2	.570	.541	.726	7.5E-11	.228	9.36	20.8	13.6
Diode#3	.549	.618	.698	4.5E-11	.267	7.55	14.4	11.2
Diode#4	.556	.626	.706	3.1E-11	.204	7.97	15.6	9.2
Diode#5	.568	.636	.718	3.5E-11	.266	8.28	15.6	12.0

Fig. 4. Measured data for M/A-Com 40401 Schottky diodes.

diode in package model 213. For the purposes here, the rectification efficiency is defined to be $(P_{DC}/(P_{inc} - P_{ref}))$, where P_{DC} is the dc output power, P_{inc} is the incident RF power, and P_{ref} is the reflected RF power. Overall efficiency is defined by (P_{DC}/P_{inc}) .

Measurement results at the design frequency of 8.51 GHz indicated a maximum overall efficiency of 66% with 65 mW of dc output power, and over 100-mW dc output power for a lower efficiency of 62%. This diode was found to exhibit a higher output voltage and higher efficiency than a similar diode by another manufacturer. Note that by choosing commercially available diodes, these diodes were not optimized for maximum efficiency for this application and, therefore, higher efficiencies are certainly possible. The output voltage increased from 3.2 to 4.1 V at the lower efficiency of 62%, indicative of the tradeoff between maximum output voltage and efficiency expected. The large output voltage of 4.1 V would allow for maximum output voltage if a suitable combination method could be found.

C. Diode Model

The diode is the most critical component in the rectenna element. All aspects of performance of the rectenna depend primarily on the diode parameters. The series resistance, for example, directly limits efficiency through the I^2R loss. The junction capacitance, together with package capacitance and lead inductance, affects how harmonic currents oscillate through the diode. The breakdown voltage limits the power-handling capability of each rectifying circuit. These parameters also affect the match of the circuit. Since the diode, as a power-rectifying element, must operate in a large-signal environment, the diode model needs to be valid for a wide range of biasing. Finally, since high efficiency requires proper termination of harmonic frequencies, the model also needs to be valid over a wide frequency range.

The simulation data for the dc performance is shown in Fig. 3. The voltage, current, and resistance data were taken from the $I-V$ curve, and the total capacitance was measured by resonating the diode with a series inductor. As can be seen, the simulation data of Fig. 3 shows that the diode model agrees

well with the measured data shown in Fig. 4. The breakdown voltage was selected to be slightly higher since it was possible to select diodes, with breakdown around 9.5 V, for use.

IV. RECTENNA CIRCUIT DESIGN

A. Circuit Design

The patch rectenna is most easily implemented using standard microstrip lines. In order to economize the use of real estate, an attempt was made to use a minimum number of stubs for the input filter/matching section. The line lengths were also made as short as possible in order to minimize the RF losses. The corresponding microstrip implementation of V_{pol} and H_{pol} circuits (for vertical and horizontal), for each of the two patch apertures, is shown in Fig. 1. Note the stepped line impedance and chip capacitor performs the final steps of low-pass filtering and matching. The circuits were optimized for an incident power of 100 mW, the expected reflection is 3–4 mW, and the expected overall efficiency was 65%.

B. Measurement of Unit Cells

Measurements of the unit cells (Fig. 1) were first completed without the microstrip patch and dc collection to the next unit cell(s). The device-under-test (DUT) consisted of a single-unit cell with a circuit for H_{pol} and a circuit for V_{pol} in the same layout, as they would appear in an array. The input microstrip lines, however, were extended to the edge of the substrate to coaxial connectors. dc output was picked off the circuit by simply soldering a single-strand wire directly to the dc bus line. A decade box was used as the load.

Initial measurements showed that the reflected power from the rectifying circuitry was much higher than expected, approximately 50%. This difference was due to a discrepancy between the placement of the via holes in the circuit schematic and physical layout. The movement of the via holes turned out to be significant.

With minimal movement of existing components and, therefore, minimal board redesign, simulation and measurement showed that additional tuning stubs could reduce the unwanted

Frequency, GHz	Board #	Incident Power, W	Reflected Power, W	Load Resistance, Ω	DC Output Voltage	Rectification Efficiency	Overall Efficiency
8.51	1	0.106	0.024	250	3.49	59.6	45.9
8.51	1	0.086	0.026	325	3.36	58.3	40.6
8.51	2	0.094	0.000	250	3.81	62.0	61.8
8.51	2	0.090	0.002	325	4.23	62.2	61.1
8.51	3	0.086	0.013	250	3.39	63.2	53.5
8.54	3	0.100	0.021	325	3.93	60.5	47.8

Fig. 5. Typical unit cell results from prototype 2 for V_{pol} circuit.

Frequency, GHz	Board #	Incident Power, W	Reflected Power, W	Load Resistance, Ω	DC Output Voltage	Rectification Efficiency	Overall Efficiency
8.51	1	0.104	0.001	250	4.01	62.5	62.1
8.51	1	0.100	0.000	325	4.42	60.1	60.1
8.51	2	0.098	0.002	250	3.8	60.1	58.9
8.51	2	0.091	0.000	325	4.17	59.2	59.0
8.51	3	0.086	0.004	250	3.53	61.3	58.1
8.51	3	0.078	0.009	350	3.84	61.1	54.0

Fig. 6. Typical unit cell results from prototype 2 for H_{pol} circuit.

reflections. The tradeoff was that the expected overall efficiency was expected to fall to 60%. The unit cell with the additional tuning stubs will be referred to as “Prototype 2.”

C. Analysis and Measurement Comparisons

Several unit cells of this version (Prototype 2) were fabricated and measured. Figs. 5 and 6 show the measured results for three separate boards. Note that the rectification efficiency of all circuits remained close to the design overall efficiency of 60%, with high overall efficiency when reflected power was minimized. The average output voltage of the H_{pol} circuits was 4.14 V at an average overall efficiency of 57.7% when using a load resistance of 325Ω . This desirable result meets the maximum output voltage from the diode measurements.

The average output voltage of the V_{pol} circuits was lower, 3.84 V, at an average efficiency of 49.8% with a load resistance of 325Ω . The tradeoff of the higher output voltage for efficiency is indicated by the lower average output voltage of 3.56 V for the higher average efficiency, 53.7%, when a load of 250Ω is used. Higher sensitivity to variations in component assembly may have contributed to the lower average overall efficiency for the V_{pol} circuits. The fact that V_{pol} circuit of board 2 performed as well as the H_{pol} circuit of board 2 indicates this to be due to variations in component assembly.

V. PANEL MEASUREMENT

A. Rectenna Panel: 3×3 Elements

Rectenna panels consisting of a 3×3 arrangement of unit cells were fabricated using the Prototype 2 circuitry. The average output voltage of the circuits was 4 V, requiring the series connection of 13 circuits to reach the design goal of 50 V. Since each patch provides two circuits, one for V_{pol} and one for H_{pol} , the minimum number of cells required is seven patch elements. Choosing the minimal square array containing at least seven patches leads to an array of 3×3 elements, for nine total patch elements.

The effective area of a single patch element is given by

$$A_p = G_p \frac{\lambda^2}{4\pi} \quad (1)$$

where G_p is the gain of the patch, or 8.4 dB at 8.51 GHz. The effective area for a single patch, before placement in the array, is, therefore, 6.8 cm^2 . In order for the array to absorb all the incident power, it is necessary that the unit cell area be less than 6.8 cm^2 . For rectangular spacing, a minimal cell-to-cell spacing of 2.62 cm is then required. Accordingly, a more dense cell-to-cell spacing of 1.97 cm was chosen to further shrink the overall panel size while still leaving sufficient room for the panel circuitry.

B. Calibration of Measurement Chamber

In order to ensure that the rectenna panel could be efficiently measured in the far field, a custom-built measurement chamber was designed to allow quick access to the panel. Fig. 7 shows the measurement chamber with the rectenna panel holder above the transmit horn. The standard gain horn used to illuminate the rectenna is a Narda 640 Standard Gain Horn. The gain of the Narda 640 @ 8.51 GHz (frequency of the incident microwave energy) is 15.1 dB. Fig. 8 shows the front side of the rectenna panel in the chamber.

The Friis transmission equation is employed to verify the power density on the plane containing the rectenna. An identical Narda 640 standard gain horn is used as the receive horn at the location of the rectenna panel. To calculate the power received by this receive horn, the Friis transmission equation is used, the system calibration is checked, and the measurement chamber accuracy verified. The measured gain of the standard gain horn is 15.03 dB for an error of 0.07 dB.

C. Effective Area Measurement of the Nine-Array Elements

During the diode and unit cell measurements, the overall efficiency was defined to be the total dc output power at the load



Fig. 7. View of the measurement chamber showing the rectenna panel holder above the transmit horn.

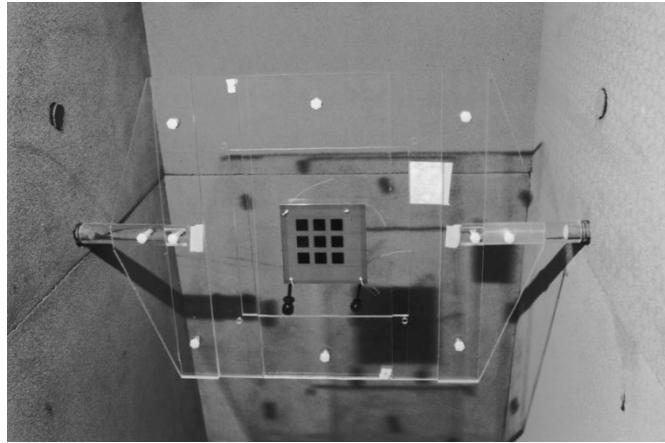


Fig. 8. Front side of the nine-element rectenna panel in the measurement chamber.

in proportion to the incident power. Thus any power that is reflected by the circuitry is not converted into dc power and decreases the overall efficiency. Likewise, in the panel measurement, overall efficiency should be defined such that any reflected power from the panel lowers the overall efficiency. One method of computing overall efficiency for a rectenna panel is to use the power density striking the rectenna panel from the Friis transmission equation multiplied by the physical panel area to compute the received power. For a small panel as used here, a more suitable method of calculating overall efficiency is to use the effective area of the panel.

Using effective area, the received power is given by

$$P_{\text{recv}} = \frac{P_{\text{trans}} G_{\text{trans}} A^{\text{eff}}}{4\pi R^2} \quad (2)$$

where A^{eff} represents the maximum effective area of the panel as the sum of the maximum effective area of each patch in the array configuration. Thus, it can be seen that for rectenna panel applications it is desirable, and possible, for the maximum effective area of the panel to exceed the physical area of the panel, and that the maximum effective area of each patch must be measured in the array configuration under matched conditions, i.e., with no reflection, when mutual coupling is present.

If the overall panel efficiency is then defined as

$$\eta_o = \frac{P_{\text{DC}}}{P_{\text{recv}}} = \frac{4\pi R^2 P_{\text{DC}}}{P_{\text{trans}} G_{\text{trans}} A^{\text{eff}}} \quad (3)$$

any power reflected from the rectenna panel will provide a decrease in the overall efficiency.

To properly compute the maximum effective area of each patch in the array configuration, a rectenna panel was built where a microstrip line leading to an subminiature A (SMA) connector replaced each rectenna circuitry, as shown in Fig. 9. Each port was individually tuned until the return loss for all patches exceeded 21 dB with all other ports matched. By symmetry, only one polarization was measured and the panel rotated for the orthogonal polarization. Thus, only one port is shown in Fig. 9.

The line losses and connector losses were removed by calibration standards for each of the two microstrip feed line configurations. To ensure accuracy of the effective area measurements for the tightly packed array, the mutual coupling between ports was measured and found to be less than 17.5 dB for all ports. This low mutual coupling for this densely packed array can be primarily contributed to the use of the low dielectric foam substrate.

The results of the effective area measurements are shown in Fig. 9. Using symmetry to reduce measurement error, the effective area was averaged between the two measurements representing the two orthogonal ports of each patch. Note that the effective area of the center patch closely matches the unit cell area, as expected. Note also that the effective area of the corner patches is slightly larger than the unit cell area since these patches are on the outside of the array.

In order to minimize the measurement discrepancies in the panel measurements that follow, the corner and center-edge effective area measurements were averaged using a symmetry argument. The total effective area of the 3×3 panel was then found to be 1 cm more than the physical area of the panel, or 3% greater than the physical area. Note that the physical area of the panel is defined to be nine times the unit cell area. Data from Port 8 was thrown out since, due to symmetry conditions, it was evident that the proximity of the SMA connector from Port 5 was affecting the measurement.

D. Panel Results

To maximize the output voltage of the panel, a series combination of all individual rectenna circuits was desired. To make this possible, the ground plane (which contains the coupling apertures) around each individual patch was dc isolated below each patch. Etching a square ring slot in the ground plane below each individual patch provides this dc isolation. To ensure RF

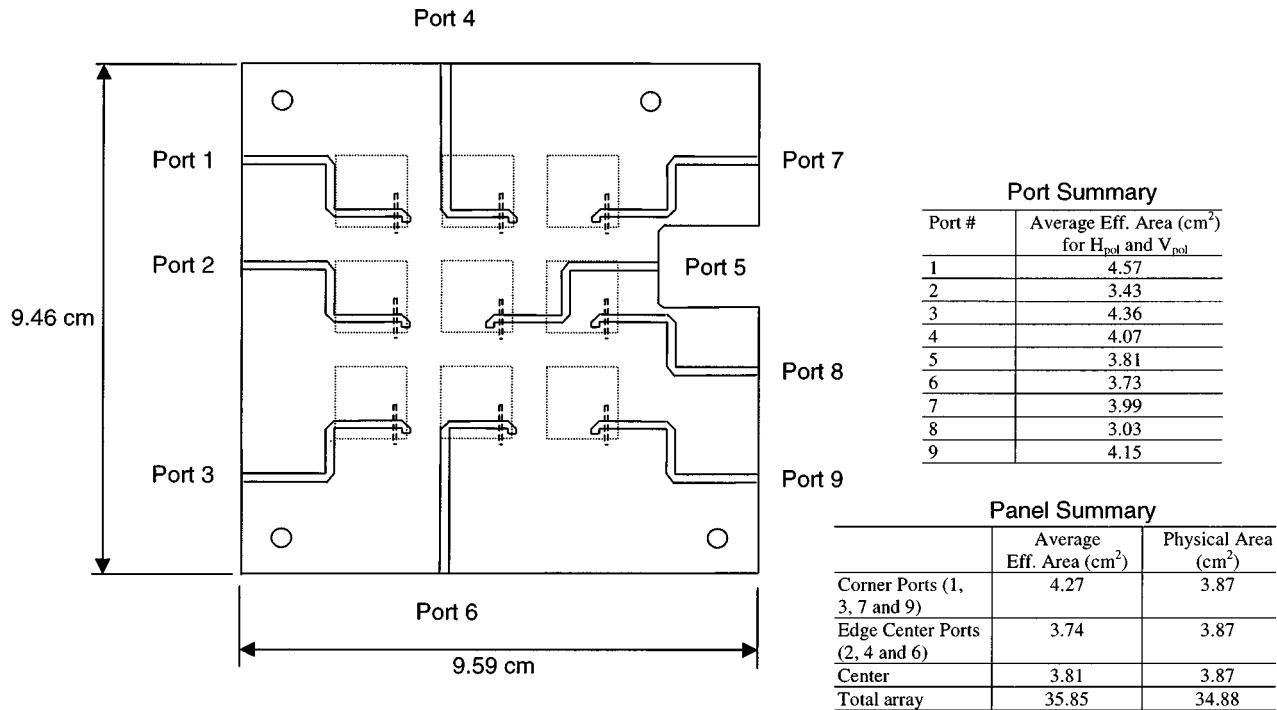


Fig. 9. Definition of ports used to measure the effective area of the panel and the measured effective area at each port.

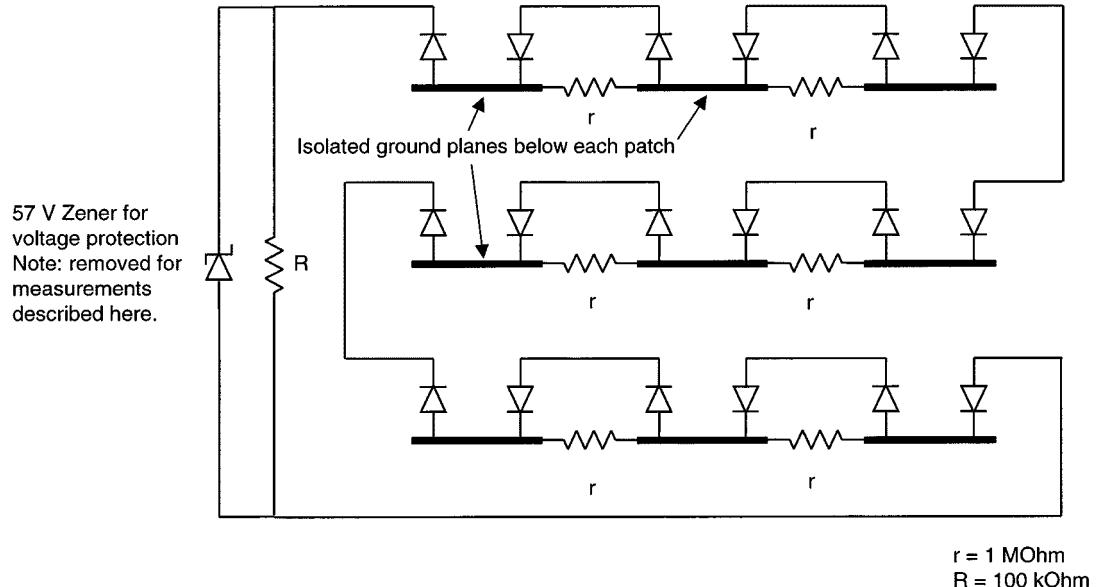


Fig. 10. Series connection of the 18 individual rectenna circuits.

continuity of the ground plane and to prevent re-radiation of harmonics generated by the circuitry through these ground plane slots, a thin layer of copper-coated polyimide was used to ensure capacitive coupling.

The diodes were installed in an opposing manner, as shown in Fig. 10, which allowed for a series output voltage for each patch. It was found that, in order to properly reverse bias in all diodes when power is applied, additional resistance between the isolated ground planes was needed. Also, the additional resistance allowed each isolated ground plane to discharge when power was removed, protecting the diodes.

Fig. 11 shows the measured results of the rectenna panel when loaded for optimum overall efficiency with a load resistance of 5400Ω . The overall efficiency is calculated using (3). The load resistance of the entire panel is, in general, 18 times the unit cell resistance. The series connection of the circuits on the panel involved connecting slightly different (not identical) circuits. Therefore, a starting load resistance of approximately 18×325 or 5850Ω was indeed close to giving optimal overall panel efficiency.

The overall panel efficiency exceeds 52% over a large region of input powers, with a peak of 53% at a receive

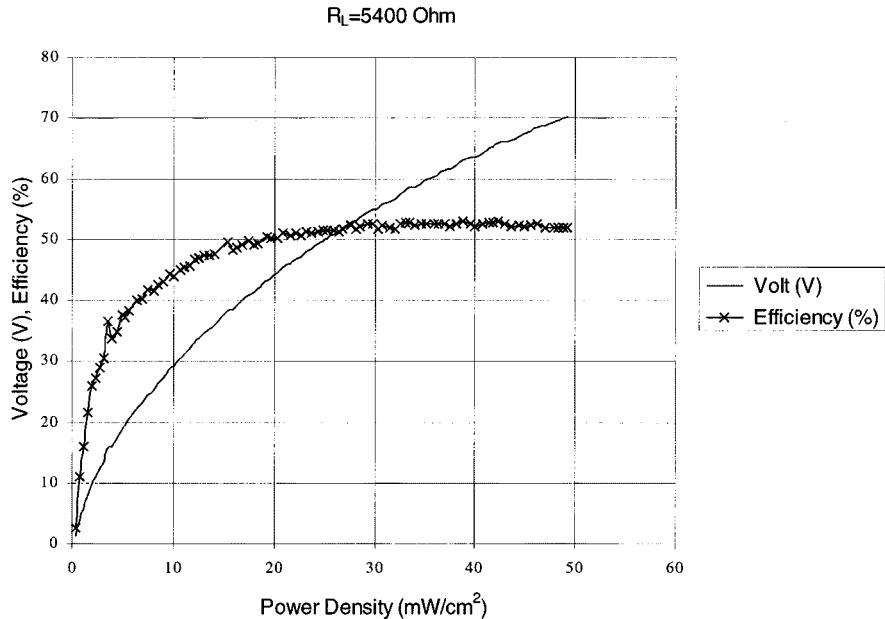


Fig. 11. Output voltage and efficiency for a rectenna panel excited by a Narda 640 standard gain horn. The voltage is the series combination of 18 circuits from two orthogonal polarizations. Nine circuits from H_{pol} and nine circuits from V_{pol} .

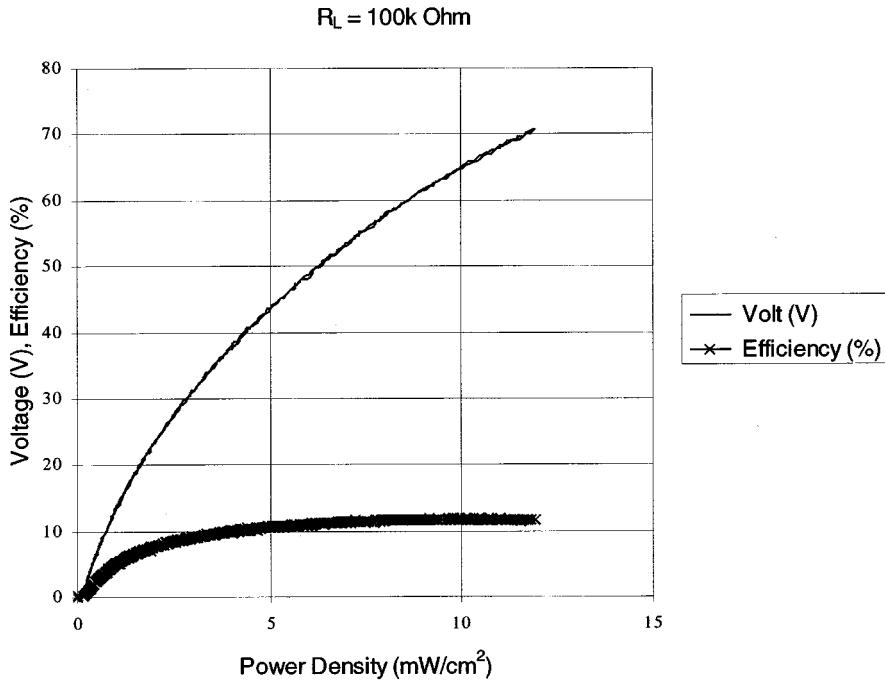


Fig. 12. Output voltage for a rectenna panel with load chosen to maximize activator voltage while minimizing the transmit power needed. Note the corresponding drop in efficiency for this application.

power of 38.8 mW/cm^2 . It also shows that the desired output voltage of 50 V can be achieved for an input power density of 25.2 mW/cm^2 . For the Narda 640 standard gain horn, this requires a transmit power of 13.6 W at a distance of 37.1 cm to provide 50 V of output power. Note that to provide maximum efficiency, the panel requires not only sufficient loading, but sufficient input power to place the diodes in an efficient region of operation. The peak overall panel efficiency is 4% less than the average efficiency of the

H_{pol} unit cell measurements and 1% less than the average V_{pol} unit cell efficiency (measured without the patch via microstrip line). This indicates that additional gains in efficiency are most likely to be obtained by optimization of the unit cell circuitry and not from further antenna optimization.

Fig. 12 shows the results for this application. By increasing the load resistance, the required 50-V output could be obtained for a low incident power density of 6.3 mW/cm^2 . This corresponds to only 3.4 W of transmit power at a distance of 37.1 cm .

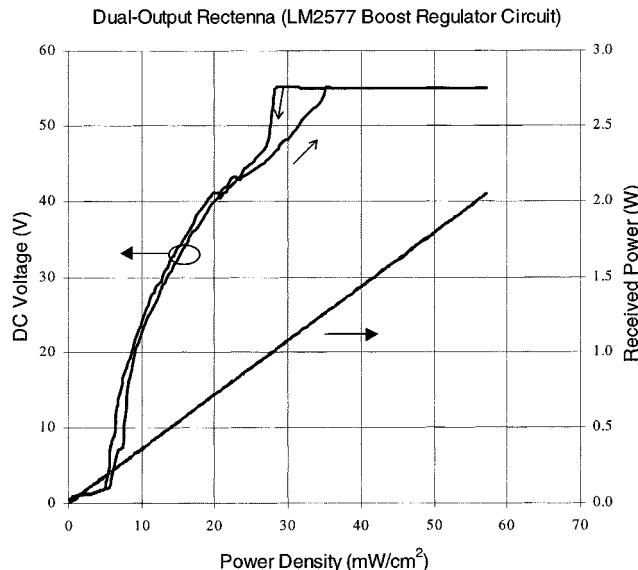


Fig. 13. Representative output voltage of a single rectenna panel using dual boost regulator circuits to provide two dc outputs. 50 V of output voltage can be produced with less than 1.5 W of received power.

Since the expected output voltage of 18 diodes in series could exceed the desired output voltage, a method of producing more than one 50-V output was desired. By attaching commercially available boost regulator circuits, it was possible to obtain two 50-V outputs. The series output of five patches, or ten circuits, was used to drive one regulator and the remainder to drive the additional regulator. Fig. 13 shows typical output when the boost regulator circuits were driving the large impedance of a voltmeter. Although interesting, this capability has not yet been tested for suitability when driving actuators that will have lower impedance.

VI. CONCLUSIONS

A compact rectenna capable of producing a 50-V output suitable for driving mechanical actuators has been demonstrated. The aperture-coupled rectenna configuration has several advantages over previous dipole rectenna designs. By proper isolation of circuits for each of two orthogonal polarizations, this rectenna is capable of receiving either dual linear or circular polarization, making it suitable for circling platforms. In addition, by using the RF ground plane to provide dc isolation of individual patches, the RF ground plane becomes part of the collection circuitry used to combine the dc outputs. This allows for flexibility in combining outputs from the two polarizations of each patch, and for the series connection of outputs from patch to patch. By proper diode placement and addition of resistance between dc isolation pads, it was demonstrated that a series combination of nine patch elements could combine the outputs of 18 diodes for dual-polarization incidence. For actuator applications, it was shown that this allows for large output voltages for low incident power density. For other applications, such as sensors, it was demonstrated that boost regulator circuits could lower the required incident power density even further.

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