A Class-E Power Amplifier Based on an Extended Resonance Technique

Adam L. Martin and Amir Mortazawi, *Member, IEEE*

***Abstract*—In this paper, a class-E power amplifier using four 1-W GaAs MESFET's at 935 MHz is demonstrated using a new extended resonance power-combining technique. A microstrip amplifier based on this technique was designed and fabricated which combines four 1-W Siemens CLY5 GaAs MESFET's with 67% power-added efficiency at 935 MHz.**

I. Introduction

SOLID-STATE power combining at microwave and millimeter frequencies is used to disperse heat more effectively, and/or increase the total available output power. For monolithic-microwave integrated-circuit (MMIC) solutions, power-combining circuits should be compact to minimize production costs as well as to avoid excess circuit loss that can degrade both power-added efficiency and power-combining efficiency. Some of the more widely used power-combining techniques for MMIC applications employ balanced amplifiers using Lange couplers [1], binary or corporate Wilkinson 3-dB hybrids [2]–[4], traveling-wave combiners [5], and power distributed amplifiers using Ginzton tapered lines [6]. The first three techniques provide excellent isolation between the active devices, but they rely on quarter-wavelength transmission lines (or lumped-element equivalents), which are large, particularly at lower frequencies. These techniques also require prematched devices, which consume additional chip area. Meanwhile, power-distributed amplifiers, using Ginzton tapered lines in the output circuit, eliminate the backward traveling wave associated with distributed amplifiers by reducing the characteristic impedance of each transmission-line section in the direction of the load. This is a nonresonant way of combining the current from each device along the output lines while maintaining an equal voltage at each device's output port. The drawback to this technique, however, is that the range of realizable microstrip line impedances severely limits the number of devices that can be combined in this manner.

A method of combining power from solid-state devices was recently introduced, based on an extended resonance technique [7]–[9]. A standing-wave structure similar to a waveguide coupled-cavity filter is realized by resonating the device admittances with each other in order to cancel their susceptance and combine their conductance. The combining process takes advantage of the complex input and output devices impedances, instead of first matching each device to a real impedance (e.g., 50 Ω). Transmission lines or lumped elements may be used to convert the admittance at one device to its conjugate value at the next device, canceling the susceptive components and adding the conductances. This condition guarantees an equal power split among the devices for power dividing/combining purposes. The advantages of using this power-combining technique are that the overall size of the resulting structure is much smaller than with hybrid combiners, and perfect power combining can be achieved without having to taper the output circuit's transmission lines.

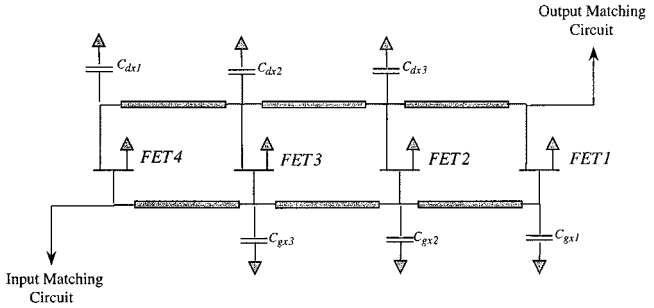

Fig. 1. Four-device extended resonance power-combining amplifier.

Presented herein is an extended resonance power-combining design based on a new more versatile transmission-line circuit topology than that employed in previous works. By introducing another degree of freedom to the circuit design, this new topology allows more flexibility in optimizing size and performance of the overall circuit. Section II addresses this new extended resonance power dividing/combining topology, and Section III discusses the design and results of a four-device class-E extended resonance power-combining amplifier at 935 MHz.

II. Extended Resonance Power Dividing/Combining

An extended resonance technique for combining power from solid-state devices was presented earlier [7]–[9], where both transmission-line and lumped-element power combiners using this technique have been developed. A transmission-line power combiner is implemented for this particular experiment, with a convenient method of impedance matching that was not presented in the previous literature. To illustrate this, a power amplifier (PA) combining four MESFET's is shown in Fig. 1. The divider/combiner circuits each possess a unique design; however, both are consistent in achieving the same phase delay between corresponding devices. The dividing and combining networks are shown separately in Fig. 2. In Fig. 2(a), the input admittance of each device $Y_{\text{in}} = G_{\text{in}} + jB_{\text{in}}$ is transformed into

Manuscript received January 12, 1999

A. L. Martin is with ITT GaAs Tek, Roanoke, VA 24019 USA.

A. Mortazawi is with the Electrical and Computer Engineering Department, North Carolina State University, Raleigh, NC 27695 USA.

Publisher Item Identifier S 0018-9480(00)00214-3.

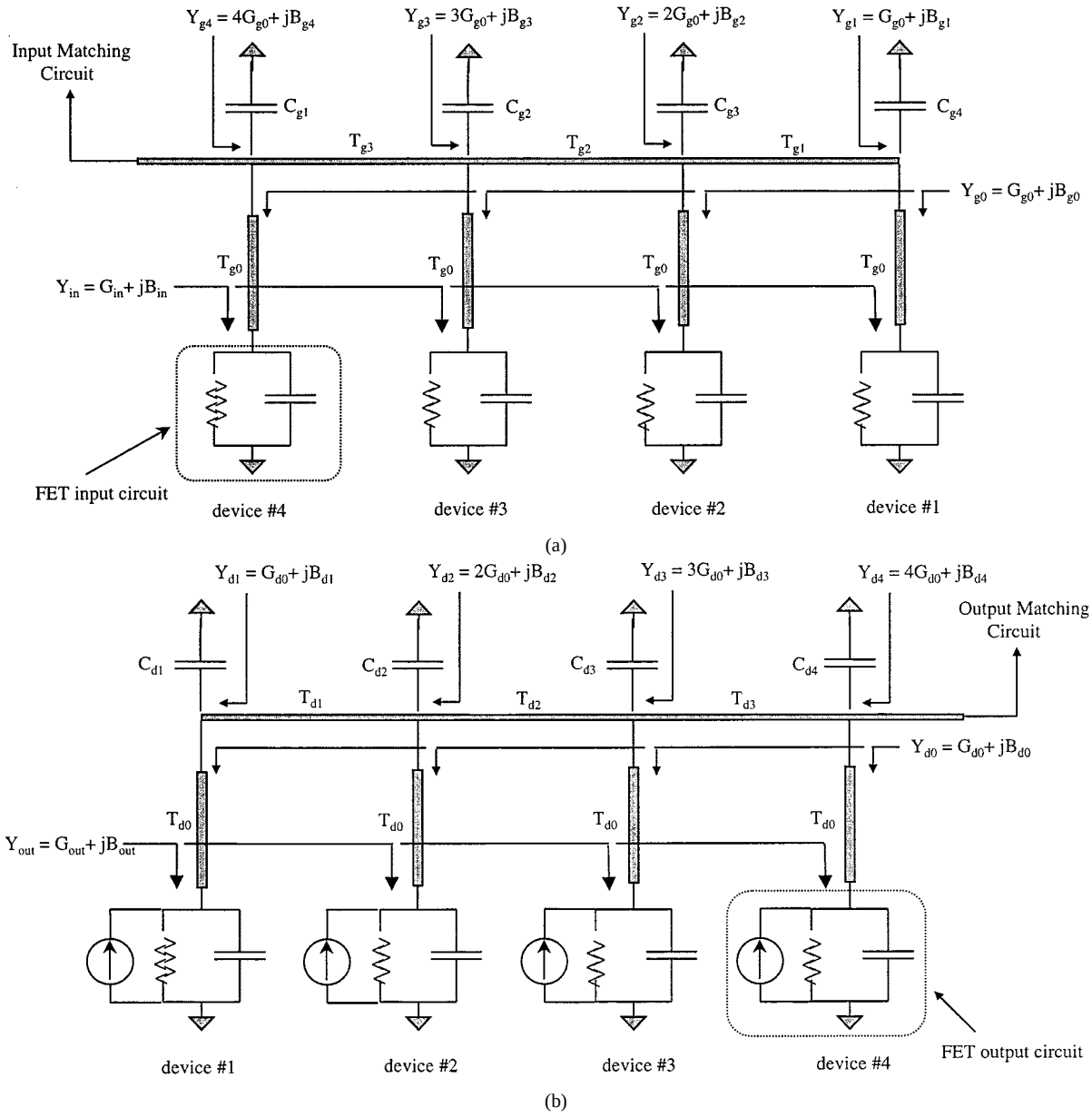

Fig. 2. (a) Extended resonance four-way power divider. (b) Extended resonance four-way power combiner.

a more "suitable" admittance $Y_{g0} = G_{g0} + jB_{g0}$ by transmission line T_{g0}. This "suitable" admittance is one that will ease the task of having to match the phase delays between the input and output circuits, and whose choice depends on the overall number of devices in the dividing/combining circuits. The value of G_{g0} is generally more important than the value of B_{g0} since a shunt capacitor (or inductor) can add or subtract the desired amount to/from B_{g0}. The admittance at each gate junction (beginning at the first device) is transformed to its conjugate value at the adjacent gate junction, thus summing the conductance at each gate junction and forcing the voltage magnitude at each transistor gate to be equal when an input signal is applied. The length of T_{g0} can be chosen so that the real component of the total circuit input impedance is 50 Ω, which simplifies the task of input matching immensely. The power-combining network in Fig. 2(b) is based on the same principle using the equivalent drain admittance of each MESFET. The power-combining network in Fig. 2(b) uses MESFET admittances that are assumed to be the conjugate of the load admittance that is to be presented to the output of each device.

The two dividing/combining circuits in Fig. 2 must be consistent with each other so that coherent power combining is achieved by creating the same phase delay between the corresponding gate and drain sections. Referring to Fig. 2(a), it can be shown that the phase delay between two adjacent transistor gates k and $k+1$ is

$$\varphi_{gk} = -\tan^{-1}\left(\frac{kG_{g0}\tan\beta l_{gk}}{1 - B_{gk}\tan\beta l_{gk}}\right) \tag{1}$$

where βl_{gk} is the electrical length of T_{gk}. Referring to Fig. 2(b), the phase delay between the corresponding drain terminals $k+1$ and k is

$$\varphi_{dk} = -\tan^{-1}\left(\frac{kG_{d0}\tan\beta l_{dk}}{1 - B_{dk}\tan\beta l_{dk}}\right) \tag{2}$$

where βl_{dk} is the electrical length of T_{dk}. For power to be combined coherently between devices k and $k+l$, the phase delay between the drains and gates must be equal [i.e., (1) = (2)]. The values of G_{g0} and G_{d0} are determined by the lengths of transmission lines T_{g0} and T_{d0}, respectively, in Fig. 2. Input/output impedance matching can be avoided when $G_{g0} = G_{d0} = 0.25/50$ S (for a 50-Ω system), and from (1) and (2)

$$\frac{8k - k^2 + 16B_g^2}{(4-k)B_g} = \frac{16 - k^2 + 16B_{d(k+l)}^2}{kB_{d(k+l)}}. \tag{3}$$

The transmission lines connecting the drains and gates are given in (4) and (5), respectively, as follows:

$$\tan \beta l_{dk} = \frac{-32B_{d(k+l)}}{16 - k^2 - 16B_{d(k+l)}^2} \tag{4}$$

and

$$\tan \beta l_{gk} = \frac{-32B_{gk}}{16 - (4-k)^2 - 16B_{gk}^2}. \tag{5}$$

In some cases, one of the transmission lines from (4) and (5) is much longer than the other, making physical layout difficult to realize. That is indeed the case for a portion of the circuit presented here. To alleviate this problem, a shunt capacitance is placed at the center of the longer transmission line and, hence, the overall length of this particular transmission line can be reduced. The phase delay across this modified gate section is

$$\varphi_{gk} = -2 \tan^{-1}\left(\frac{kG_{g0} \tan \beta l_{gk}}{1 - B_{gk} \tan \beta l_{gk}}\right) \tag{6}$$

where βl_{gk} is the reduced electrical length of each transmission line T_{gk}. This technique provides more design leeway, and allows a greater number of transistors to be more easily combined.

Class-E amplifier operation is briefly described in Section III, and then experimental results from a four-device class-E PA using the above design procedure are given.

III. Class-E Amplifier Design

Emerging high-capacity digital communication formats (e.g., QPSK, OQPSK, CDMA) are challenging the design of linear, compact, and efficient PA's for wireless transceivers. PA's generally achieve either high linearity or high power-added efficiency at the expense of the other [10]. For optimal efficiency and linearity, it has become common practice to employ a linearization circuit in conjunction with a power-efficient PA [11]. However, this does not necessarily relieve the PA completely since a certain degree of linearity is still required depending on the linearization technique (e.g., predistortion feed-forward Cartesian feedback). Lately, envelope restoration techniques with bandpass delta–sigma modulators [12] have been investigated for linear amplification using class-E switch-mode PA's [13], [14]. The baseband amplitude information is modulated on the PA supply voltage while the phase variation is contained within the RF input signal, resulting in a pulsewidth modulated class-E amplifier whose output voltage scales linearly with the supply voltage [15]. A very high power-added efficiency is preserved, since the amplifier operates in heavy saturation over the entire range of amplitude variation of the information signal. This is a major advantage that the class-E amplifier has over other amplifier classes. In addition, class-E amplifiers are relatively simple to implement since they do not require multiple bandpass circuits in the output circuit tuned to appropriate harmonics.

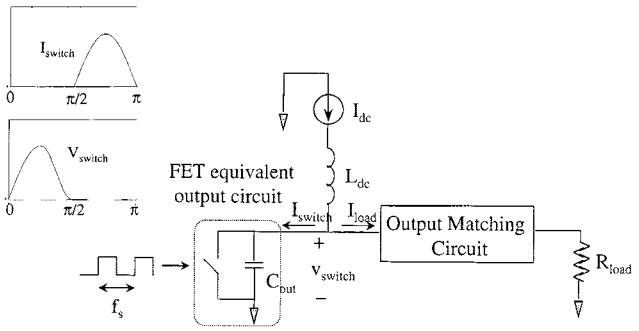

Fig. 3. Class-E amplifier.

A single-device class-E amplifier is shown in Fig. 3, along with the idealized voltage and current waveforms. The active device, in this case an FET, is driven at 50% duty cycle between saturation and cutoff at the frequency of the input drive. The input may be a square wave or it may be a very large amplitude sine wave, which is more often the case for microwave operation. Ideally, either the "switch" voltage $v_{\rm sw}$ or the "switch" current $i_{\rm sw}$ is zero at any given instant in time so that transistor power loss is eliminated. In addition, the slope of $v_{\rm sw}$ at turn on should be zero to minimize energy loss when the input signal is frequency modulated. The "switch" opens and closes at the input drive frequency, and the transistor current is being alternately steered through the small channel resistance $r_{\rm on}$ and the capacitor $C_{\rm ds}$. A high-Q output matching network filters out all harmonic components of the transistor current and provides a clean sinusoidal load current. The amplifier achieves a very high efficiency if $r_{\rm on}$ is the primary contributor to power loss in the circuit. The output matching circuit is tuned so that at turn-on $v_{\rm sw}$ is zero and, therefore, the energy stored in the capacitor at that instant $1/2C_{\rm ds}v_{\rm sw}^2$is also zero.

A convenient formula for finding the appropriate load impedance that will provide the class-E waveforms presented in Fig. 3 has been derived [16] as follows:

$$Z_L = \frac{0.28}{2\pi f C_{\rm ds}} e^{j49.05^\circ}. \tag{7}$$

Note that only the output capacitance $C_{\rm ds}$ and the switching frequency f need be known for calculating the class-E load impedance. The load impedance is independent of both the input drive and drain supply voltage. Therefore, amplitude modulating the drain supply voltage should not have a significant effect on the power-added efficiency. An upper limit, however, must be placed on the supply voltage in order to maintain optimal class-E operation (max efficiency) at a given frequency (assuming this voltage is well short of the breakdown voltage). It has been shown [16] that the maximum frequency at which a particular FET can operate under optimal class-E conditions is

$$f_{\rm max} = \frac{I_{\rm dss}}{56.5 C_{\rm ds} V_{\rm DS}} \tag{8}$$

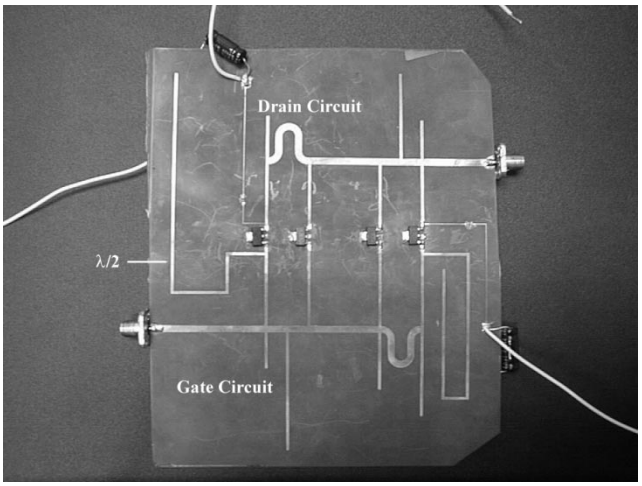

Fig. 4. Four-device class-E amplifier at 935 MHz.

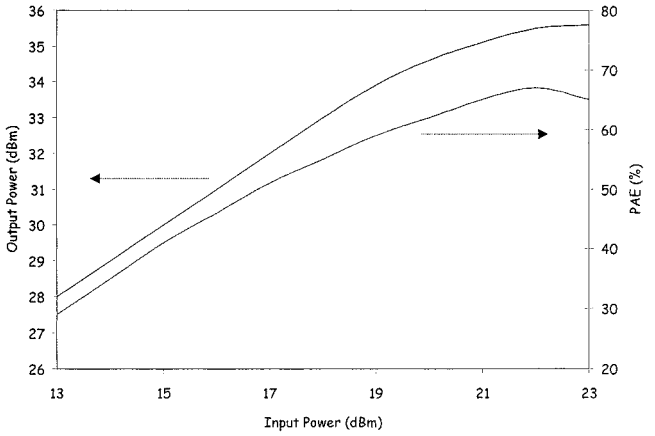

Fig. 5. Output power and power-added efficiency for the four-device extended resonance amplifier.

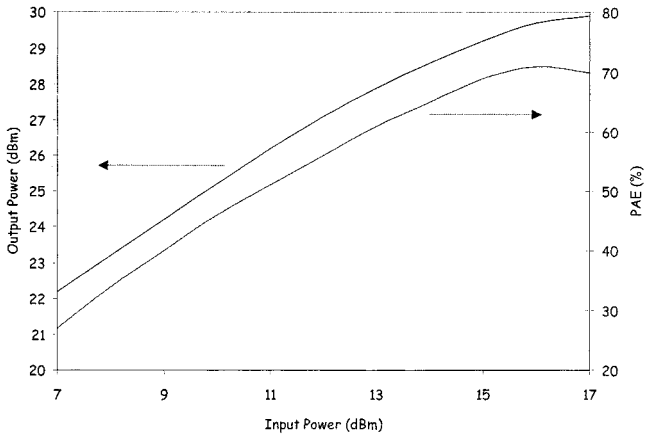

Fig. 6. Output power and power-added efficiency for the single-device amplifier.

where $I_{\rm ds}$ is the maximum transistor current, $C_{\rm ds}$ is the equivalent transistor output capacitance, and $V_{\rm DS}$ is the drain-to-source supply voltage. Obviously, a lower supply voltage results in less available output power, and (8) illustrates a tradeoff between operating frequency and output power when using a single-device class-E amplifier.

IV. Extended Resonance Class-E PA

For this experiment, each transistor is a packaged 1-W GaAs MESFET Siemens model CLY5. The output capacitance, $C_{\rm ds}$ is approximately 2.4 pF, which is obtained from a nonlinear Materka model provided by Compact Software (now Ansoft Inc.), Pittsburgh, PA. The four-device class-E extended resonance power-combining amplifier is fabricated using surface-mount devices on a 31-mil-thick Duroid substrate with $\epsilon_r = 2.2$ and $\tan\,\delta = 0.0012$. The circuit simulations are performed with Microwave Harmonica, Compact Software. From (7), the class-E load admittance for this transistor is $Y_L = I/Z_L = 0.06 - j0.006$ at 935 MHz, and a single device is terminated by this admittance using a single-stub matching network with a 50-Ω load. The lead inductance of the CLY5 package is included as part of the load-matching network. The input admittance is determined from the simulation when the transistor generates nearly a watt of output power with a drain efficiency of approximately 80%. The simulated large-signal input admittance is $Y_{\rm IN} = 0.01 + j0.035$ at 935 MHz, which is matched to 50 Ω using a single-stub matching network, and the simulated power-added efficiency of the single-device class-E amplifier is 75%.

The next step is designing the extended resonance power-dividing and power-combining circuits using the transistor class-E input and output admittances. The output admittance of the transistor can be assumed to be the conjugate of the load admittance determined from (7) minus the series inductance from the package lead. A photograph of the four-device amplifier is shown in Fig. 4. All shunt capacitors have been implemented with equivalent open-circuited microstrip stubs. The open-circuit transmission lines in shunt with the gates of the outer devices are approximately $\lambda/4$ long at 465 MHz in order to prevent subharmonic oscillations. The gate and drain transmission-line lengths have been chosen such that the conductive component seen looking into each of them is (0.02)/4 S, or 0.005 S, so that the power-combiner input and output ports are automatically matched to 50 Ω. It should be noted that the cumulative transmission-line length used in this circuit is almost half that required for quarter-wave hybrid and Wilkinson combiners using the same devices.

When constructing the extended resonance PA, the gate and drain leads are soldered to the microstrip lines, and the source leads are grounded through via holes in the substrate. The drain bias is applied through two separate 68-nH surface-mount inductors, while the gate bias is applied through a bias tee. The drain supply voltage is 6 V, and for class E, the gates are biased just below cutoff, at –3.2 V. The four-device amplifier under test is driven into saturation with a 1-W preamplifier. The dc supply current is monitored for power-added-efficiency calculations. At 935 MHz, the output power and power-added efficiency as a function of input power are plotted for the four-device amplifier in Fig. 5. The best power-added efficiency is 67%, which corresponds to an output power of 34.7 dBm and a gain of 12.7 dB. A similar plot for a single-device class-E amplifier at 935 MHz is shown in Fig. 6. The maximum power-added efficiency for the single-device amplifier is 71% at an output power

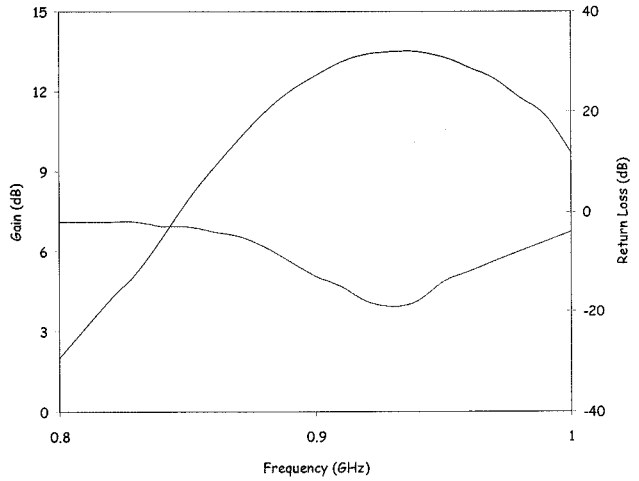

Fig. 7. Large-signal gain and return loss for the four-device extended resonance amplifier.

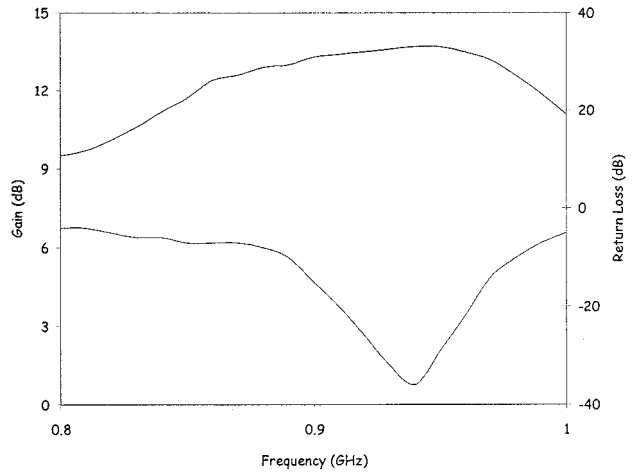

Fig. 8. Large-signal gain and return loss for the single-device amplifier.

of 29.2 dBm and a gain of 13.2 dB. The large-signal gain and return loss as a function of frequency for the extended resonance amplifier and single-device amplifier are plotted in Figs. 7 and 8, respectively. The 1-dB bandwidth for the extended resonance PA is quite comparable to the single-device amplifier, despite the fact that the four transistors are combined in "series."

V. Conclusions

An extended resonance power-combining technique has been used to demonstrate a class-E PA that is well suited for MMIC implementation because it does not require quarter-wavelength transmission lines, prematched devices, or tapered transmission lines. In this case, four transistors operating at class E have been successfully combined without sacrificing power-combining or power-added efficiency.

References

[1] K. J. Russell, "Microwave power combining techniques," *IEEE Microwave Theory Tech.*, vol. MTT-27, pp. 472–478, May 1979.

[2] G. Ferrell, L. Dickens, J. Gipprich, B. Hayes, and F. Sacks, "A high efficiency 10-watt HBT power amplifier assembly using combining techniques," in *IEEE Microwave Theory Tech. Symp. Dig.*, vol. 2, 1995, pp. 327–330.

[3] J. Gipprich, L. Dickens, and J. Faulkner, "A power amplifier yields 10 watts over 8-14 GHz using GaAs MMIC's in a LTCC serial combiner/divider network," in *IEEE Microwave Theory Tech. Symp. Dig.*, vol. 3, 1993, pp. 1369–1372.

[4] J. Gipprich, L. Dickens, R. Hayes, and M. Restivo, "A compact LTCC multilayer multiport stripline coupler network for low-loss power combining/splitting," in *IEEE 3rd Topical Meeting Elect. Performance Electron. Packag.*, 1994, pp. 167–169.

[5] I. D. Robertson, Ed., *MMIC Design*. ser. (IEE Circuits Syst. Series 7). London, U.K.: Inst. Elect. Eng., 1995.

[6] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*, New York: Wiley, 1990.

[7] A. Martin, B. C. DeLoach, and A. Mortazawi, "An eight-device extended resonance power combining amplifier," *IEEE Microwave Theory Tech.*, vol. 46, no. 6, pp. 844–850, June 1998.

[8] A. Martin, M. Mortazawi, and B. C. DeLoach, Jr., "A new lumped-element power combining amplifier based on an extended resonance technique", submitted for publication.

[9] A. L. Martin, A. Mortazawi, and B. C. DeLoach, Jr., "A power amplifier based on an extended resonance technique," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 329–331, Oct. 1995.

[10] T. Sowlati *et al.*, "Low voltage high efficiency class E GaAs power amplifiers for wireless communications," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1074–1080, Oct. 1995.

[11] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.

[12] A. Jayaraman, P. F. Chen, G. Hanington, L. Larson, and P. Asbeck, "Linear high-efficiency microwave power amplifiers using bandpass delta-sigma modulators," *IEEE Microwave Guided Wave Lett.*, vol. 8, pp. 121–123, Mar. 1998.

[13] N. Sokal and A. Sokal, "Class E—A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 168–176, June 1975.

[14] F. H. Raab, "Idealized operation of the class-E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-24, pp. 725–735, Dec. 1977.

[15] M. Kazimierczuk, "Collector amplitude modulation of the class-E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-31, pp. 543–549, June 1984.

[16] T. Mader and Z. Popovic, "The transmission-line high-efficiency class-E amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 290–292, Sept. 1995.

Adam L. Martin, photograph and biography not available at the time of publication.

Amir Mortazawi (S'87–M'90) received the B.S. degree in electrical engineering from the State University of New York at Stony Brook, in 1987, and the M.S. and Ph.D. degrees in electrical engineering from the University of Texas at Austin, in 1988 and 1990, respectively.

In 1990, he joined the University of Central Florida, Orlando, as an Assistant Professor, and became an Associate Professor in 1995. In August 1998, he joined North Carolina State University, Raleigh, as an Associate Professor of electrical engineering. His research interests include millimeter-wave power-combining oscillators and amplifiers, quasi-optical techniques, and nonlinear analysis of microwave circuits.