A Symmetrical Nonlinear HFET/MESFET Model Suitable for Intermodulation Analysis of Amplifiers and Resistive Mixers

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***Abstract*—We propose a new symmetrical heterojunction FET (HFET)/MESFET model to predict intermodulation distortion in amplifiers and resistive mixers. The model is symmetric. That is, drain and source of the intrinsic FET are interchangeable. This reflects the characteristics of most microwave FET's. The model has few fitting parameters and they are simple and straightforward to extract. The model was installed into Hewlett-Packard's harmonic-balance program microwave design system and verified by measurements. The verification shows excellent results for an MESFET and an HFET in both amplifier and resistive mixer configurations.**

***Index Terms*—MESFET'S, MODFET's, modeling.**

I. Introduction

INTERMODULATION (IM) distortion in microwave receiver front ends is mainly generated in their mixers and amplifiers. Since heterojunction FET's (HFET's) and MESFET's are common in both mixers and amplifiers, nonlinear modeling of these devices has become an important issue. An FET model capable of predicting IM distortion in both amplifiers and resistive mixers would, therefore, be attractive.

The nonlinear behavior of the FET is usually assumed to be localized to its intrinsic part and can be described by I/V and Q/V characteristics. The I/V characteristic is considered to be the more nonlinear of these two characteristics. If the reactive currents are low compared to the active ones, the reactive nonlinear contributions can be neglected. This is done by keeping the fundamental frequencies below 10 GHz. In the following, we will focus on the nonlinear I/V characteristic of the FET.

For FET's operated as amplifiers or gate mixers (where one or two signals are input at the gate) several models have been proposed [1]–[5]. These models predict gain or conversion loss (CL) and IM products very well for such applications. For FET's operated as resistive mixers (where two signals are input at different terminals of the FET), several models have also been proposed [6], [7]. All these models fit the drain-to-source current ($I_{\rm ds}$) and its derivatives with respect to the drain-to-source voltage ($V_{\rm ds}$) along the line $V_{\rm ds} = 0$. This results in very good predictions of IM levels for moderate $V_{\rm ds}$ amplitudes.

However, in [1] $I_{\rm ds}$ and its derivatives are modeled in only one bias point, whereas in [2] $I_{\rm ds}$ and its derivatives with respect to the gate-to-source voltage ($V_{\rm gs}$) are modeled for constant $V_{\rm ds}$. The models in [3]–[5] are limited to positive $V_{\rm ds}$ since they do not reflect the inherent symmetry of the intrinsic microwave FET, and [6] and [7] are restricted to moderate input amplitudes at the drain ($V_{\rm ds} \approx 0$). Consequently, none of the above models are suitable for modeling the FET in both amplifier and resistive mixer applications. Furthermore, no investigation has yet been conducted to determine which trajectory the voltages in the FET will cover for high input amplitudes at the drain in a resistive mixer.

Therefore, we propose an FET model [8] covering the region of operation for the FET in both amplifier and resistive mixer applications at high input amplitudes. The model is based on the assumption that the intrinsic FET is symmetric with respect to interchange of drain and source, reflecting the characteristics of most microwave FET's. The model has few fitting parameters and the parameter extraction is simple and straightforward. The model is verified for an HFET (NEC NE32400) and an MESFET (NEC NE76000) in both mixer and amplifier applications with excellent results. Furthermore, we propose a new concept, i.e., load area, to determine the most important region in which to model the FET when applying two signals at different terminals.

II. Modeling Approach

The nonlinear I/V characteristic of the HFET/MESFET is assumed to be localized to the intrinsic device and is symbolized by the current generator $I_{\rm ds}$ in the equivalent circuit in Fig. 1. We define the intrinsic device as the part of the FET where the gate and channel overlap.

As mentioned earlier, we neglect the nonlinear behavior of the FET's Q/V characteristic. That is, $C_{\rm gd}$, $C_{\rm gs}$, and $C_{\rm ds}$ are kept constant. This can be justified by the following. For the fundamental frequencies and the devices used in this paper, the phase of the reflection coefficient will maximally vary 12° over the entire $V_{\rm gs}$ range due to capacitance nonlinearity and the magnitude of the reflection coefficient will hardly vary at all. Hence, the variation in the voltage waveform at the gate due to capacitance nonlinearity is negligible at these frequencies. Simulations with nonlinear capacitance models indicate that the frequency has to

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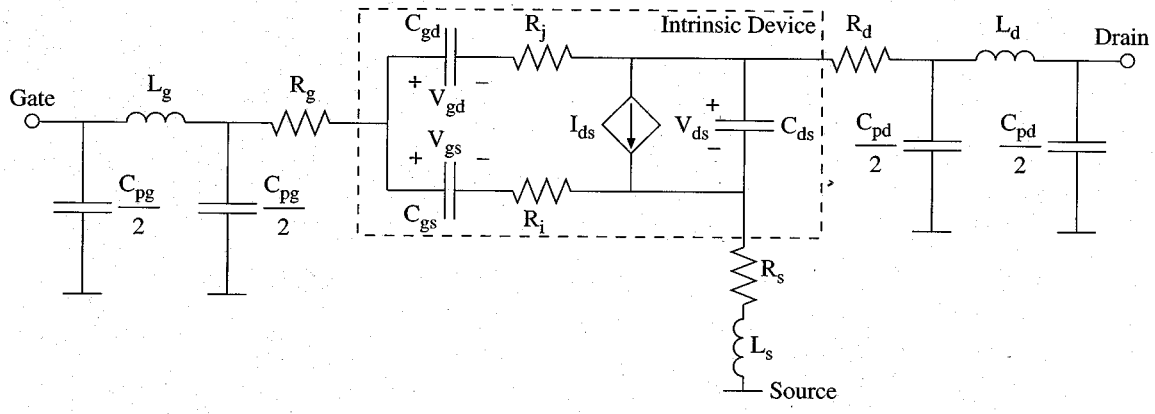

Fig. 1. Equivalent circuit of an HFET or MESFET device.

be increased to at least 15 GHz for the capacitance nonlinearities to affect the IM products measured in this paper. These results agree well with assumptions and results in [2] and [9] where similar devices are investigated.

The intrinsic part of the equivalent circuit in Fig. 1 is valid under the following two conditions. First, $V_{\rm gs}$ and the gate-to-drain voltage ($V_{\rm gd}$) should be kept between the breakdown voltage and the forward-current turn on voltage (V_f) of the gate-to-channel junction. Second, the dc power dissipation should not cause any large temperature changes.

Although the intrinsic part of most microwave FET's is symmetric, the extrinsic part is not symmetric since most FET's are designed for common source operation. For this reason, the capacitance of the source pad is usually not modeled (it is shorted to ground by L_s). However, if L_s is disconnected from ground, as in a common drain or common gate configuration, it becomes important to model the source pad capacitance. A convenient way to physically achieve a "common drain" FET without having an equivalent circuit containing a source pad capacitance is to operate the transistor in the reversed mode (i.e., invert the dc-bias current through the channel and interchange the names of the drain and the source connectors). Of course, reversing the dc bias of the FET requires a symmetric intrinsic model.

A. Selecting Independent Voltages to Make Modeling Simple

Our aim is to predict $I_{\rm ds}$ for both positive and negative $V_{\rm ds}$. Since the intrinsic FET is a symmetric device, it should be possible to select a set of independent voltages that reveal this symmetry.

Since the intrinsic FET has three terminals, gate, drain, and source, it is possible to plot $I_{\rm ds}$ as a function of any two voltages between these terminals. A common choice is $V_{\rm gs}$ and $V_{\rm ds}$. Fig. 2 shows a contour plot of $I_{\rm ds}$ versus $V_{\rm gs}$ and $V_{\rm ds}$. Obviously, this choice of a coordinate system does not make use of inherent symmetries (which makes it difficult to find a function describing $I_{\rm ds}$).

The symmetry of the intrinsic FET can be preserved by selecting $V_{\rm gd}$ and $V_{\rm gs}$ as independent variables (Fig. 3) since drain and source are inherently equivalent.

We, therefore, regard $I_{\rm ds}$ as a function of $V_{\rm gd}$ and $V_{\rm gs}$.

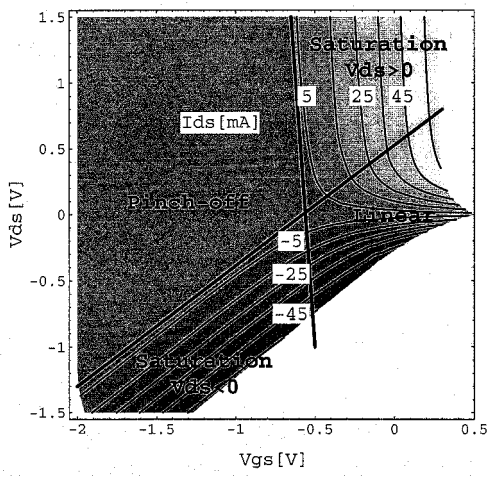

Fig. 2. Contour plot of $I_{\rm ds}$ versus $V_{\rm gs}$, and $V_{\rm ds}$ measured for the MESFET. The voltages are intrinsic.

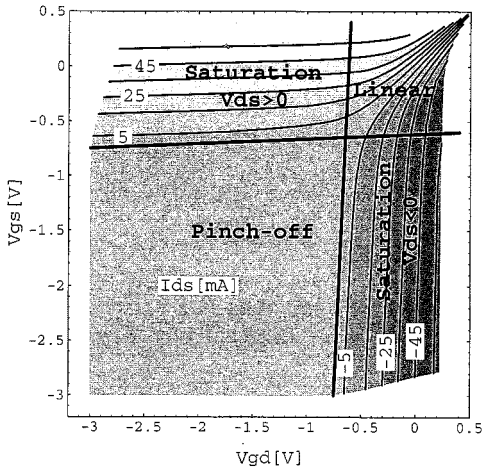

Fig. 3. Contour plot of $I_{\rm ds}$ versus $V_{\rm gd}$ and $V_{\rm gs}$ measured for the MESFET. The voltages are intrinsic.

In Fig. 3, the $V_{\rm gd}$–$V_{\rm gs}$ plane is roughly divided into four regions: one region where the device is approximately linear, two where the device is essentially saturated, and one pinchoff region. In the linear region notice that $I_{\rm ds}$ is almost proportional

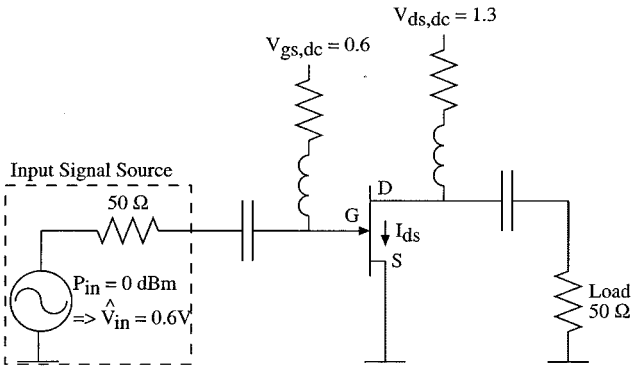

Fig. 4. FET operated as an amplifier.

to $V_{\rm ds}$. In the saturated region with $V_{\rm ds} > 0\, I_{\rm ds}$ is mainly dependent on $V_{\rm gs}$ and in the saturated region with $V_{\rm ds} < 0\, I_{\rm ds}$ is mainly dependent on $V_{\rm gd}$. The $I_{\rm ds}$ characteristic when $V_{\rm ds}$ is negative is not reflected in previous models designed for amplifier or gate mixer analysis [1]–[5].

In the following, we assume that $I_{\rm ds}$ is perfectly antisymmetric about the diagonal $V_{\rm gd} = V_{\rm gs}$ i.e., $I_{\rm ds}(V_{\rm gs}, V_{\rm gd}) = -I_{\rm ds}(V_{\rm gd}, V_{\rm gs})$. This assumption is based on the fact that most microwave FET's have a channel that is symmetric with respect to interchange of drain and source.

B. Load Line and Load Area

In this section, we roughly estimate the most important region in the $V_{\rm gd}$–$V_{\rm gs}$ plane in which to model the FET when using it in amplifiers resistive mixers, respectively. To keep the calculations simple, this is done from measured $I_{ds,\,\rm DC}$ data imported into a table driven dc simulator.

We define "load line" as the trajectory that the voltages in an amplifier will cover in the $V_{\rm gd}$–$V_{\rm gs}$ plane. Since it is most interesting to view the load line versus intrinsic voltages and since we wish to compute the load line from measured data, values for R_s and R_d have to be assumed. For the MESFET, 3.8 Ω, respectively, 4.8 Ω are used. An FET operated as an amplifier is shown in Fig. 4. In Fig. 5, the corresponding load line and dc operating point are marked in the $V_{\rm gd}$–$V_{\rm gs}$ plane.

A similar approach can be used for the resistive FET mixer. In this case, we have two input signals: LO and RF. Dual input signals yield a load area rather than a load line. An FET operated as a resistive mixer is shown in Fig. 6. The RF source impedance and IF load impedance are incorporated in the same resistor and it is not necessary to separate them to determine the load area.

The load area is determined by setting the LO (RF) voltage to its extreme values and sweeping the RF (LO) voltage between its extreme values. The asymmetry of the load area is due to the mixer topology. In a mixer like the one in [10], the load area will be symmetric. In Fig. 5, the load area boundary and the dc-operating point are marked for the MESFET with power levels and bias voltage, as in Fig. 6.

The load line in Fig. 5 shows that it is only necessary to model the FET behavior for $V_{\rm ds} > 0$ to predict amplifier performance. This confirms earlier work done on FET models for amplifiers or gate mixers [1]–[5]. On the other hand, the load area shows

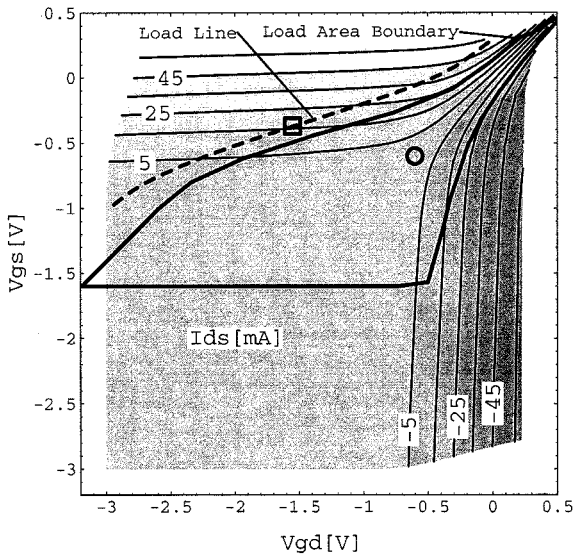

Fig. 5. Contour plot of $I_{\rm ds}$ measured for the MESFET with the amplifier load line and the mixer load area boundary marked. The square indicates the amplifier dc operating point and the circle indicates the mixer dc operating point. The voltages are intrinsic.

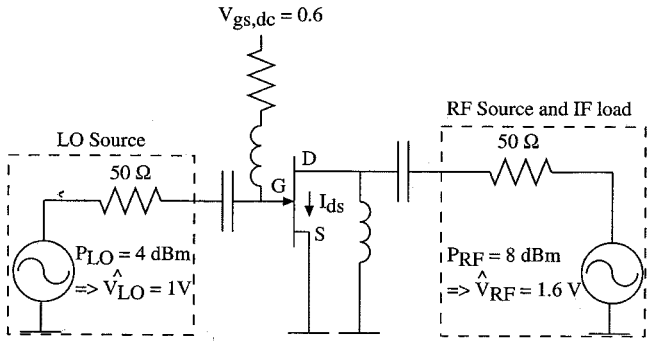

Fig. 6. FET operated as a resistive mixer.

the need for a model covering both positive and negative $V_{\rm ds}$ to predict the performance of resistive mixers. If the RF amplitude is increased further, the load area will enclose the load line. Therefore, an FET model capable to predict the performance of a resistive FET mixer at high RF amplitudes will also be suitable for amplifier analysis. However, FET models designed for amplifier analysis are not necessarily useful in the analysis of resistive mixers. Altering the source or load impedances on the amplifier or mixer harmonics will change the shape of the load line and load area. The load line and load area concepts will later be used as a simple verification of different models.

III. The Model

As pointed out earlier, $I_{\rm ds}$ is antisymmetric with respect to interchange of $V_{\rm gd}$ and $V_{\rm gs}$. Therefore, we choose to express $I_{\rm ds}$ in terms of $V_{\rm gd}$ and $V_{\rm gs}$. The $I_{\rm ds}$ model is defined by (1)–(5). The model parameters are a, b, c, d, g, and ϕ as follows:

$$I_{\rm ds} = g \cdot \Big[f_1(U_{\rm gd}^{+}, U_{\rm gs}^{+}) \cdot f_2(V_{\rm gs} - V_{\rm gd}) - f_1(U_{\rm gs}^{-}, U_{\rm gd}^{-}) \cdot f_2(V_{\rm gd} - V_{\rm gs}) \Big] \quad (1)$$

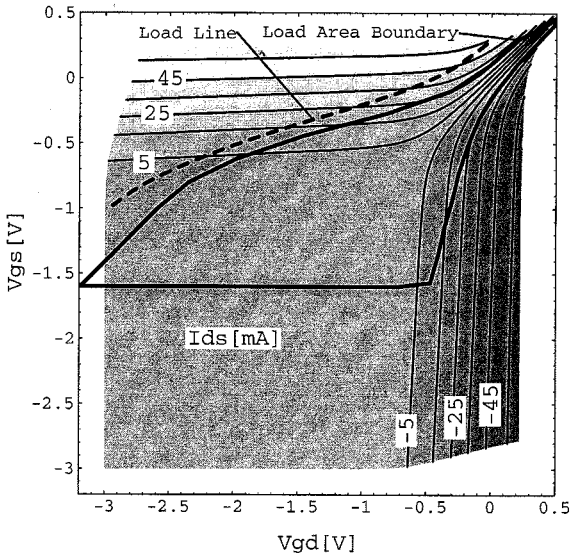

Fig. 7. Contour plot of $I_{\rm ds}$, load line, and load area boundary for the MESFET predicted with the proposed model. The voltages are intrinsic.

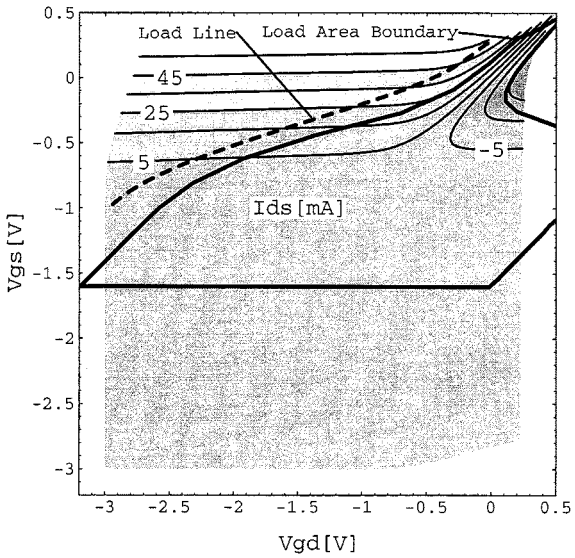

Fig. 8. Contour plot of $I_{\rm ds}$, load line, and load area boundary for the MESFET predicted with the Angelov model. The voltages are intrinsic.

where

$$f_1(x, y) = [1 + a \cdot x] \cdot \left[1 - \tanh\left(e^{-b\cdot(y+c)}\right)\right] \tag{2}$$

and

$$f_2(z) = 1 - \tanh\left(e^{-d\cdot z}\right). \tag{3}$$

The first part of (1) dominates for $V_{\rm ds} > 0$ and the second part dominates for $V_{\rm ds} < 0$. $U_{\rm gd}^{+}$ and $U_{\rm gs}^{+}$ define a coordinate system rotated by the angle ϕ counterclockwise relative to the $V_{\rm gd}$–$V_{\rm gs}$ coordinate system (4)

$$\begin{bmatrix} U_{\rm gd}^{+} \\ U_{\rm gs}^{+} \end{bmatrix} = \begin{bmatrix} \cos\phi & \sin\phi \\ -\sin\phi & \cos\phi \end{bmatrix} \cdot \begin{bmatrix} V_{\rm gd} \\ V_{\rm gs} \end{bmatrix}. \tag{4}$$

$U_{\rm gd}^{-}$ and $U_{\rm gs}^{-}$ define a coordinate system rotated by the angle ϕ clockwise relative to the $V_{\rm gd}$–$V_{\rm gs}$ coordinate system (5). In the saturated region, where $V_{\rm ds} > 0$ ($V_{\rm ds} < 0$), ϕ models the shift in pinchoff voltage with $V_{\rm gd}(V_{\rm gs})$. In the saturated region at high $I_{\rm ds}$, the parameters a and ϕ model the slight $V_{\rm gd}(V_{\rm gs})$ effect on $I_{\rm ds}$

$$\begin{bmatrix} U_{\rm gd}^{-} \\ U_{\rm gs}^{-} \end{bmatrix} = \begin{bmatrix} \cos\phi & -\sin\phi \\ \sin\phi & \cos\phi \end{bmatrix} \cdot \begin{bmatrix} V_{\rm gd} \\ V_{\rm gs} \end{bmatrix}. \tag{5}$$

The model is empirical, but it can be shown that the $V_{\rm gs}$ effect on $I_{\rm ds}(V_{\rm ds} > 0)$ is approximated by the Rohdin–Roblin model [11] and the Angelov model [4]. When $V_{\rm ds} > 0$, the transport model ($V_{\rm ds}$ effect on $I_{\rm ds}$) is also similar to the models above. As suggested in [12], we use an exponential argument for the hyperbolic tangent instead of a power series, as used in [4]. This reduces the number of fitting parameters. The model is designed to reproduce the first derivatives of $I_{\rm ds}$ correctly up to a few tenths of a volt below V_f.

Fig. 7 shows the prediction of $I_{\rm ds}$, the load line, and load area with the full proposed model. The bias voltages and signal levels are the same as in Figs. 4 and 6. The predictions agree well with measured data in Fig. 5.

Fig. 8 shows the prediction of $I_{\rm ds}$, load line, and load area with the Angelov model [4], [5]. The bias voltages and signal levels are the same as in Figs. 4 and6. Apparently this model does not predict $I_{\rm ds}$ correctly for $V_{\rm ds} < 0$. However, it models $I_{\rm ds}$ and its derivatives accurately for $V_{\rm ds} > 0$. It is, therefore, useful for amplifier and gate–mixer analysis.

The contour plot of the Maas–Neilson model [3] is not shown because of its similarity to Fig. 8. However, in this model, special attention has been paid to fit the model to the measured derivatives of $I_{\rm ds}$ with respect to $V_{\rm ds}$ for a swept $V_{\rm gs}$. Therefore, it predicts gain, CL, and IM products well for amplifiers and gate mixers. The models [1], [2], [6], and [7] predict $I_{\rm ds}$ along a strip in the $V_{\rm gd}$–$V_{\rm gs}$ plane. Therefore, it is meaningless to plot them in the entire $V_{\rm gd}$–$V_{\rm gs}$ plane.

IV. Parameter Extraction

A. Linear-Model Parameters

For the extraction of the linear parameters, we use a direct extraction method [13]–[15]. In this paper, we neglect the nonlinear contribution from the intrinsic capacitances. Therefore, we set $C_{\rm gd}$, $C_{\rm gs}$, and $C_{\rm ds}$ to small-signal values extracted at an application-relevant bias point. Due to extraction difficulties, R_i and R_j were set to a low value. Tables I and II present the extracted linear-model parameter values for the HFET and MESFET.

B. Nonlinear-Model Parameters

The model can be fit to data from either ac or dc measurements. Fitting to ac measurements is generally better since it allows fitting to the derivatives of $I_{\rm ds}$. Furthermore, ac measurements circumvent the problem with frequency dispersion caused by traps in the semiconductor material. We first describe a model parameter-extraction procedure based on small-signal ac measurements.

TABLE I
EXTRINSIC LINEAR-MODEL EXTRACTED FOR THE HFET AND MESFET

	C_{pg} [fF]	C_{pd} [fF]	L_g [pH]	L_d [pH]	L_s [pH]	R_g [Ω]	R_g [Ω]	R_d [Ω]	R_i [Ω]	R_j [Ω]
HFET	56	56	60	55	44	0.5	2.5	2.6	0.1	0.1
MESFET	65	65	54	49	45	1.0	4.8	3.8	0.1	0.1

TABLE II
INTRINSIC LINEAR-MODEL PARAMETERS EXTRACTED FOR THE HFET AND MESFET

	C_{gd} [fF]	C_{gs} [fF]	C_{ds} [fF]
HFET mixer	60	60	0
HFET amplifier	130	21	20
MESFET mixer	60	60	0
MESFET amplifier	240	24	33

We use the direct extraction method [13]–[15] to extract the first derivatives of $I_{\rm ds}$ with respect to $V_{\rm ds}$ and $V_{\rm gs}$, i.e., g_m and g_d (6), (7), from measured S-parameters

$$g_m = \left.\frac{dI_{\rm ds}}{dV_{\rm gs}}\right|_{V_{\rm ds}=\text{Constant}} \tag{6}$$

and

$$g_d = \left.\frac{dI_{\rm ds}}{dV_{\rm ds}}\right|_{V_{\rm gs}=\text{Constant}}. \tag{7}$$

We make two sets of S-parameter measurements where the dc bias is limited to $V_{\rm ds} \geq 0$. The first set covers the saturated and pinchoff regions where $I_{ds,\,\rm DC}$ and S-parameters are measured versus extrinsic $V_{\rm gs}$ with the extrinsic $V_{\rm gd}$ or $V_{\rm ds}$ as parameter. The second set covers the linear and pinchoff regions where $I_{ds,\,\rm DC}$ and S-parameters are measured versus extrinsic $V_{\rm gs}$ with $V_{\rm ds} = 0$. We choose $V_{\rm ds} = 0$ because the load area of the resistive mixer collapses to this line for low RF input levels. From the first set, g_m is extracted and, from the second set, g_d is extracted. The voltage drop over R_s and R_d is then subtracted at each bias point giving the intrinsic $V_{\rm gd}$ and $V_{\rm gs}$, which are the actual control voltages of the model. The fitting of the model is simple enough to be carried out manually. The following steps are iterated a few times.

- The parameters a, b, c, g, and ϕ are used to fit the modeled g_m to the g_m extracted from the first set of measurements above. The parameter c affects the pinchoff voltage, whereas ϕ accounts for the shift in pinchoff voltage with $V_{\rm gd}$. The parameters b and g affect the maximum g_m, whereas a accounts for the change of maximum g_m with $V_{\rm gd}$.
- The parameter d is now used to fit the modeled g_d to the g_d extracted from the second set of measurements above.

If only dc measurements are available, the following extraction method can be used. In this case, fitting to the derivatives of $I_{\rm ds}$ is difficult since these would be computed by differentiating the dc data, making them sensitive to measurement and roundoff errors.

TABLE III
NONLINEAR-MODEL PARAMETERS EXTRACTED FOR THE HFET AND MESFET

	a [V^{-1}]	b [V^{-1}]	c [V]	d [V^{-1}]	g [A]	ϕ [°]
HFET	-0.080	3.3	0.41	10	0.056	2.4
MESFET	0.040	1.9	0.22	6	0.092	1.9

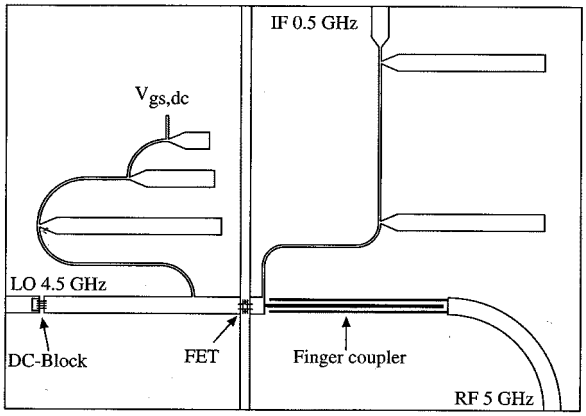

Fig. 9. Layout of the mixer used for model verification.

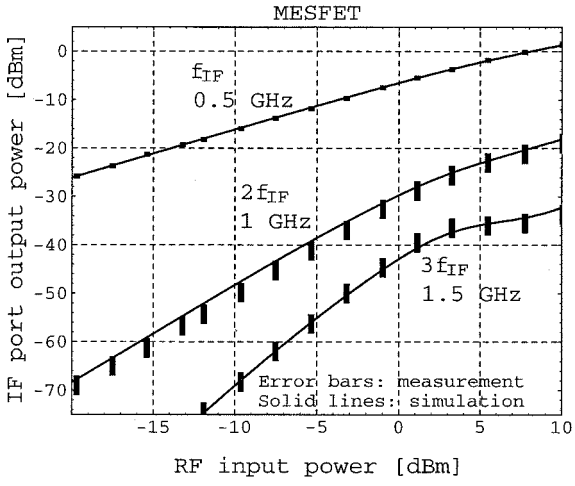

Fig. 10. Output levels at one, two, and three times the IF frequency versus RF power for the MESFET mixer. $P_{\rm LO} = 4$ dBm, $V_{\rm gs} = -0.60$ V.

We make two sets of $I_{\rm ds}$ measurements, also, in this case, we limit the dc bias to $V_{\rm ds} \geq 0$. The first set covers the saturated and pinchoff regions where $I_{\rm ds}$ is measured versus extrinsic $V_{\rm gs}$ with the extrinsic $V_{\rm gd}$ or $V_{\rm ds}$ as a parameter. The second set covers the linear and saturated region where $I_{\rm ds}$ is measured versus extrinsic $V_{\rm ds}$ with the extrinsic $V_{\rm gs}$ as a parameter. The voltage drop over R_s and R_d is then subtracted at each bias point giving the intrinsic $V_{\rm gd}$ and $V_{\rm gs}$. The following procedure is then iterated a few times.

- The parameters a, b, c, g, and ϕ are used to fit the model to the measured $I_{\rm ds}$ from the first set above.
- The parameters a, d, and g are used to fit the model to the measured $I_{\rm ds}$ from the second set above.

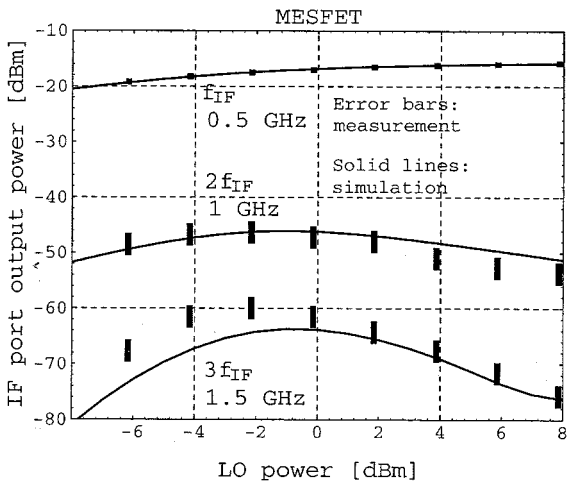

Fig. 11. Output levels at one, two, and three times the IF frequency versus LO power for the MESFET mixer. $P_{RF} = -10$ dBm, $V_{\rm gs} = -0.60$ V.

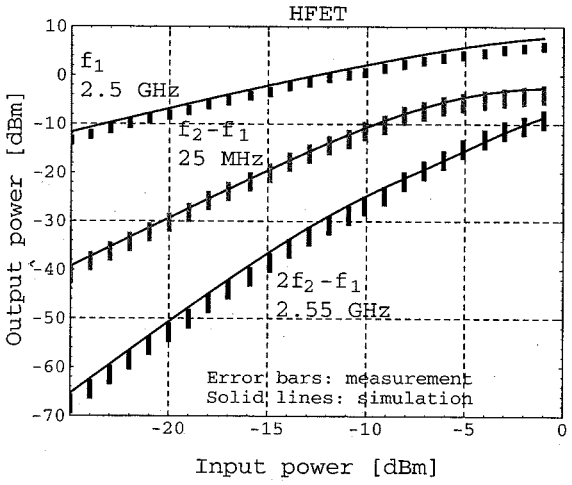

Fig. 13. Output levels at f_1, $f_2 - f_1$, and $2f_2 - f_1$ versus input power for the HFET amplifier. $V_{\rm gs} = -0.60$ V and $V_{\rm ds} = 2$ V.

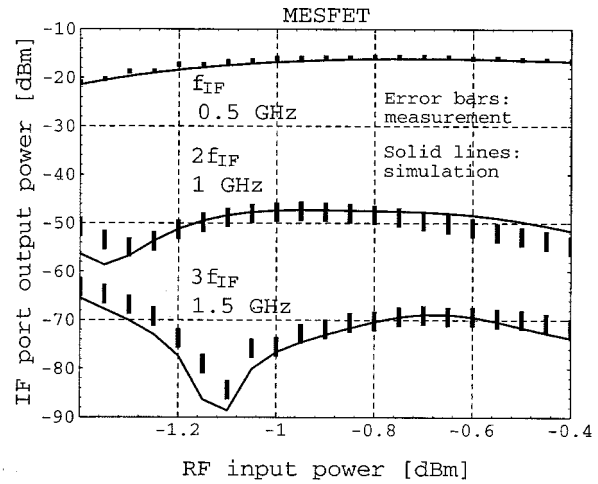

Fig. 12. Output levels at one, two, and three times the IF frequency versus gate-to-source voltage for the MESFET mixer. $P_{\rm LO} = 4$ dBm, $P_{RF} = -10$ dBm.

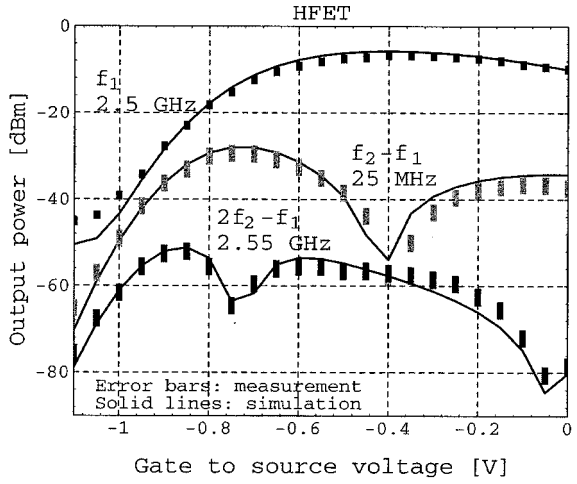

Fig. 14. Output levels at f_1, $f_2 - f_1$, and $2f_2 - f_1$ versus gate-to-source voltage for the HFET amplifier. $P_{in} = -21$ dBm and $V_{\rm ds} = 2$ V.

Fitting the model to dc measurements will, however, result in less accurate predictions of the highest order IM products shown in Section V.

Table III contains the parameter values for the HFET and the MESFET extracted from small-signal ac measurements. No tuning of the parameters has been done to fit the simulations to the verifying measurements.

V. Verification

The model was implemented in Hewlett-Packard's harmonic-balance program microwave design system (MDS) and verified by IM measurements with the MESFET and HFET in one mixer and one amplifier setup.

Mixer single-tone IM levels were measured and simulated. Single-tone IM products are easier to measure than two-tone IM products since they only require two signal generators. We believe they test the ability of the model to predict IM in mixers just as well as more complicated two-tone IM measurements. For the amplifier, two-tone second- and third-order IM levels were measured and simulated.

A. Mixer IM Measurements and Simulations

The mixer test setup consists of a resistive FET mixer realized on a microstrip substrate (RT Duroid 5870). The mixer was equipped with the MESFET and its layout is shown in Fig. 9. The input-signal frequencies were 5 GHz (f_{RF}) and 4.5 GHz ($f_{\rm LO}$) and the desired output-signal frequency (f_{IF}) was 0.5 GHz. The mixer was not optimized to meet any specific design goals since its only purpose was to verify the nonlinear model. The output levels at f_{IF}, $2f_{IF}$, and $3f_{IF}$ were measured versus RF power (P_{RF}), versus LO power ($P_{\rm LO}$), and versus $V_{\rm gs}$. $P_{\rm LO}$ was kept below 8 dBm to keep $V_{\rm gd}$ and $V_{\rm gs}$ below V_f of the MESFET.

The mixer had optimum CL of 6.1 dB at $V_{\rm gs} = -0.60$ V dc with $P_{\rm LO} = 4$ dBm. In Figs. 10–12, measured and simulated output levels at f_{IF}, $2f_{IF}$, and $3f_{IF}$ are plotted. The level at f_{IF} was measured with a power meter, while the levels at $2f_{2F}$

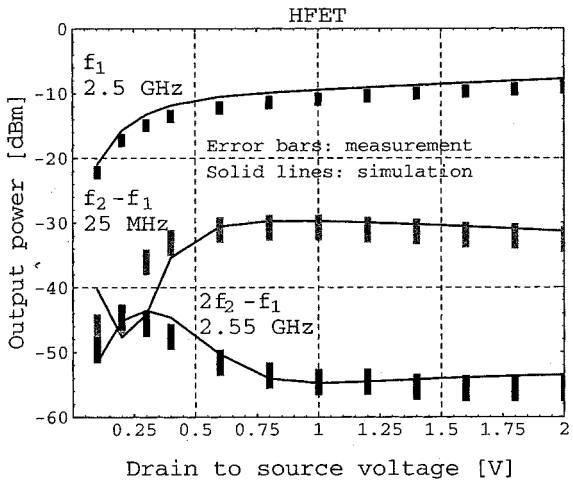

Fig. 15. Output levels at f_1, $f_2 - f_1$, and $2f_2 - f_1$ versus drain-to-source voltage for the HFET amplifier. $P_{in} = -21$ dBm and $V_{\rm gs} = -0.60$ V.

and $3f_{IF}$ were measured with a spectrum analyzer. The simulated results are plotted with lines and the measured results are plotted with error bars. We estimate the measurement error to ±0.5 dB for f_{IF} and ±2 dB for the other signals.

B. Amplifier IM Measurements and Simulations

The amplifier test setup consists of the HFET bonded to 50-Ω lines. For simplicity, no tuning of the amplifier was done. The input frequencies of the amplifier were 2.500 GHz (f_1) and 2.525 GHz (f_2). Output levels at f_1, $f_2 - f_1$, and $2f_2 - f_1$ were measured versus input power (Fig. 13), versus $V_{\rm gs}$ (Fig. 14), and versus $V_{\rm ds}$ (Fig. 15). The measurements were made with a spectrum analyzer. The simulated results are plotted with lines and the measured results are plotted with error bars. The measurement errors are estimated to be ±0.8 dB for f_1 and ±2 dB for the other signals.

VI. Conclusion

A symmetrical HFET/MESFET model suitable for predicting IM in amplifiers and resistive mixers has been derived and evaluated in this paper. The model reflects the inherent symmetry of most microwave HFET's and MESFET's. The load-line concept is generalized to a load-area concept. This is used to determine the most important region in the $V_{\rm gd}$–$V_{\rm gs}$ plane in which to model the HFET/MESFET in resistive mixer operation. The model contains few fitting parameters and the valid region is expanded compared to other models [1]–[7]. The parameter extraction is simple and straightforward. The model is verified with excellent results for both amplifiers and resistive mixers. We believe the model is also useful for predicting the performance of gate and drain mixers.

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