Balanced Monolithic Oscillators at K- and Ka-Band

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***Abstract*—A technique for generating accurate antiphase signals is presented in this paper. Monolithic oscillators at 20 and 40 GHz are realized using this technique. These oscillators have dual outputs that are mutually locked in antiphase. The inherent amplitude and phase balances between the output signals are verified. This is achieved by direct measurement using injection-locking polar diagrams, as well as low-frequency measurements of the down-converted oscillator outputs. The operation of the balanced oscillator as a multidevice power-combining oscillator is also investigated. Improvements of phase noise reduction and frequency stabilization are demonstrated at the combined oscillator output. This new oscillator topology shows significant potential in balanced circuits like mixers, multipliers, and modulators where circuit performance relies on the precise generation of the balanced signals.**

***Index Terms*—MMIC's, power combining, oscillators.**

I. Introduction

BALANCED circuit topologies are widely used to enhance circuit performance. For example, balanced mixers offer advantages of spurious response rejection, enhanced port isolations, and better power-handling capabilities. For multipliers, a balanced structure results in higher output power and rejection of undesired harmonics. The success of these circuits, however, relies on the availability of accurate antiphase signals, which is often the most difficult part of the circuit design.

Traditionally, balanced signals are obtained by the use of baluns [1]–[4]. The required antiphase is achieved through the phase-shifting characteristics of transmission lines [1] or filter structures [2], which can be narrow-band or occupy large circuit areas. Active baluns [3], [4] have also been reported, but they are often over complex, sensitive to the operating conditions, require many dc bias connections, and have poor noise and linearity performance.

Therefore, it will be very beneficial if the oscillator itself can provide antiphase outputs, eliminating the need for baluns. Several oscillator circuits have been reported [5]–[10] that have two identical oscillators operating in antiphase. In these oscillators, an external resonator that exhibits an odd-mode resonance is used to couple the two oscillators in antiphase. The resonators may be in the form of dielectric resonators [5], [6], hairpin resonators [7], [8], or microstrip patch resonators [9]. Another approach is to use 180° phase shifters between the oscillators to force the oscillators into antiphase oscillations [10]. These approaches are not suitable for monolithic microwave circuits, as the resonators required are either incompatible with monolithic-microwave integrated-circuit (MMIC) technology or they require large chip areas. In this paper, a technique for generating antiphase signals without the need for external resonators is presented. It is based on the extended resonance approach described in [11]. This results in compact monolithic oscillators, which can serve as integrated oscillators for the antiphase inputs of a balanced mixer. A simplified analysis of the balanced oscillator and measured results of two monolithic oscillators at K- and Ka-band are presented to demonstrate the technique.

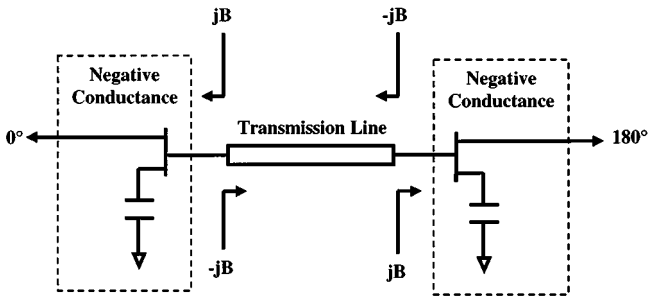

Fig. 1. Schematic diagram of the balanced oscillator.

II. The Balanced Oscillator

The schematic diagram of the balanced oscillator is shown in Fig. 1. It consists of two identical FET's whose gates are interconnected by a transmission line. Common-source capacitive feedback is applied to both FET's to develop a negative conductance at the oscillation frequency. Thus, the admittance of each device is $-G + jB$ under large-signal conditions. Using the extended resonance technique [11], the length of the transmission line is chosen such that the two devices resonate with each other. This is achieved by selecting the length so that each device's susceptance is transformed to a susceptance with the same magnitude, but opposite in sign. As illustrated in Fig. 2, this transformation creates a virtual short circuit at the midpoint of the transmission line, ensuring that the devices are injection locked out of phase. It should be noted that the transmission line serves as part of the resonant circuit instead of the coupling network or 180° phase shifter in other oscillators [5]–[9].

III. Analysis

Fig. 3 shows the equivalent circuit of the balanced oscillator. Y_{D1} and Y_{D2} represent the admittances of the two negative conductance devices and their loads, while Y_{C1} and Y_{C2} represent the admittances seen by the devices. The transmission line is

Manuscript received October 28, 1999. This work was supported by the Engineering and Physical Sciences Research Council, and by Prof. K. K. Cheng, Chinese University of Hong Kong. The work of K. S. Ang was supported by the Defence Science Organization National Laboratories.

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Publisher Item Identifier S 0018-9480(00)00856-5.

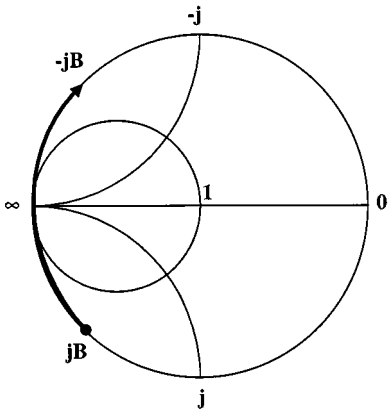

Fig. 2. Admittance chart illustrating the susceptance transformation through the transmission line.

characterized by a two-port network with its terminal voltages represented by voltage phasors, which is given by

$$\tilde{V}_1 = V_1 e^{j\phi_1}$$
$$\tilde{V}_2 = V_2 e^{j\phi_2} \tag{1}$$

where V_1, V_2, ϕ_1 and ϕ_2 are the magnitudes and phases of the voltage phasors.

The circuit equations at the transmission-line terminals can then be written as

$$\begin{pmatrix} -Y_{D1}\tilde{V}_1 \\ -Y_{D2}\tilde{V}_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} \tilde{V}_1 \\ \tilde{V}_2 \end{pmatrix}. \tag{2}$$

Any losses in the transmission line can be treated as part of the load admittances. The transmission line can then be considered lossless and its Y-parameters are given by

$$Y_{11} = Y_{22} = -jY_0 \cot\theta$$
$$Y_{12} = Y_{21} = jY_0 \csc\theta \tag{3}$$

where Y_0 is the characteristic admittance and θ is the electrical length of the transmission line. Since the oscillator consists of two identical halves, the following will be assumed:

$$V_1 = V_2 = V$$
$$Y_{D1} = Y_{D2} = Y_D$$
$$Y_{C1} = Y_{C2} = Y_C. \tag{4}$$

Substituting (4) and (1) into (2), the following relationship between ϕ_1 and ϕ_2 is obtained:

$$e^{\pm j(\phi_2 - \phi_1)} = \frac{Y_D + Y_{11}}{-Y_{12}}. \tag{5}$$

The admittance Y_D consists of the device admittance and load conductance

$$Y_D = G_L - G + jB \quad G > 0. \tag{6}$$

The admittance Y_C seen by the devices can be related to Y_D by the transmission-line equation

$$Y_C = Y_0 \frac{Y_D + jY_0 \tan\theta}{Y_0 + jY_D \tan\theta}. \tag{7}$$

Using the extended resonance technique, the length of the transmission line is chosen such that

$$\mathrm{Re}(Y_C) = G_L - G$$
$$\mathrm{Im}(Y_C) = -jB. \tag{8}$$

Solving (8) using (6) and (7) gives

$$\tan\theta = \frac{2BY_0}{B^2 - Y_0^2 + (G_L - G)^2}. \tag{9}$$

The real parts of admittances Y_C and Y_D are negative during oscillation startup. As the signal level increases, the device gain drops until the losses are exactly cancelled. Under steady-state oscillation conditions

$$G_L - G = 0. \tag{10}$$

The electrical length of the transmission line is then given by

$$\theta = \tan^{-1} \frac{2BY_0}{B^2 - Y_0^2}. \tag{11}$$

Thus, the Y-parameters in (3) are determined as

$$Y_{11} = -j\frac{B^2 - Y_0^2}{2B}$$
$$Y_{12} = j\frac{B^2 + Y_0^2}{2B}. \tag{12}$$

The phase relation in (5) can then be solved to give

$$e^{\pm j(\phi_2 - \phi_1)} = -1$$
$$\phi_2 - \phi_1 = \pm 180^\circ. \tag{13}$$

Therefore, under steady-state oscillating conditions, the outputs of the balanced oscillator are in antiphase.

IV. MMIC Realization

Based on the concept described, balanced oscillators were designed at K- and Ka-band to investigate the technique experimentally. These chips were fabricated using GEC Marconi's standard F20 and H40 processes. The F20 process employs 0.5-μm gate-length MESFET's on 200-μm-thick GaAs substrate. The H40 process employs 0.25-μm gate-length AlGaAs/InGaAs pseudomorphic high electron-mobility transistors (pHEMT's) on a 100-μm-thick GaAs substrate. The oscillator frequencies for the F20 and H40 processes were chosen to be 20 and 40 GHz, respectively, to fully exploit the capabilities of the devices and to demonstrate the technique for millimeter-wave applications.

A. K-Band Oscillator

Fig. 4 shows a photograph of the 20-GHz monolithic prototype that measures 1.2 mm × 1.6 mm. The circuit employs two 4 μm × 75 μm FET's with capacitive source feedback, laid out in rotational symmetry. Although the FET's were designed to operate under identical biasing conditions, separate biasing was catered for in this prototype. Mesa resistors of 3 kΩ were used for the gate bias, while quarter-wavelength transmission lines were used for the drain bias and source grounding. It can be

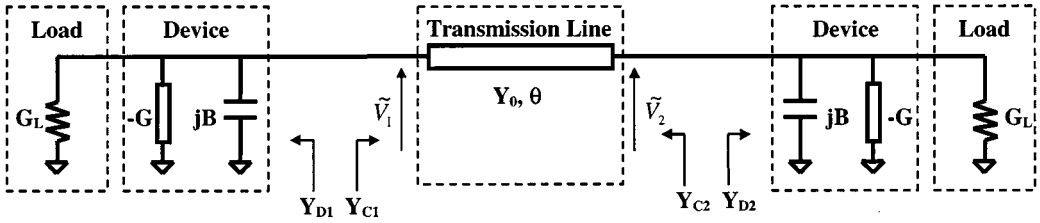

Fig. 3. Equivalent circuit of the balanced oscillator.

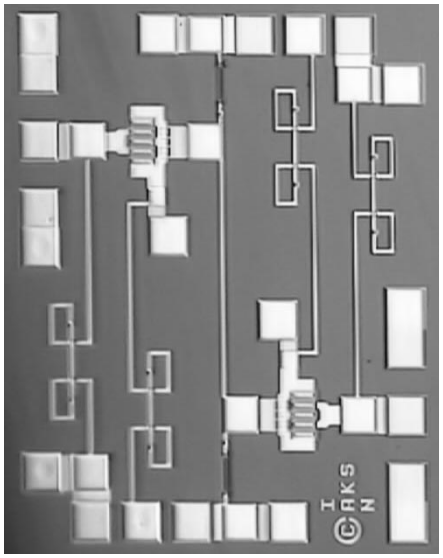

Fig. 4. Photograph of the K-band oscillator chip (1.2 mm × 1.6 mm).

noted that the length of the transmission line between the FET's is shorter than a quarter-wavelength.

B. Ka-Band Oscillators

Two chips were designed on the H40 process, as shown in Figs. 5 and 6. The chip dimensions are 0.9 mm × 1.3 mm and 1.3 mm × 2.3 mm, respectively. The first chip is analogous to the 20-GHz oscillator and employs two 2 μm × 60 μm pHEMT's. The second chip has a similar oscillator whose outputs are coupled to a pair of resistive FET mixers for down conversion. These mixers consist of two 2 μm × 60 μm pHEMT's whose gates are pumped by a common local oscillator (LO) input. By down converting the oscillator signals to low frequencies, the amplitude and phase relationships between the oscillator outputs can be readily studied as their operating conditions are varied. The mixers are included on-chip to avoid introducing additional amplitude and phase differences between the outputs by external cable connections and mixers, which will be inevitable when off-chip down conversion is performed. This ensures that the amplitude and phase relationships between the oscillator outputs are maintained in the down-converted signals.

This circuit configuration also represents a balanced mixer topology in which the antiphase signals are obtained without any baluns or hybrids. Thus, demonstrating the application of balanced oscillators as an integrated oscillator for generating antiphase signals in balanced circuits.

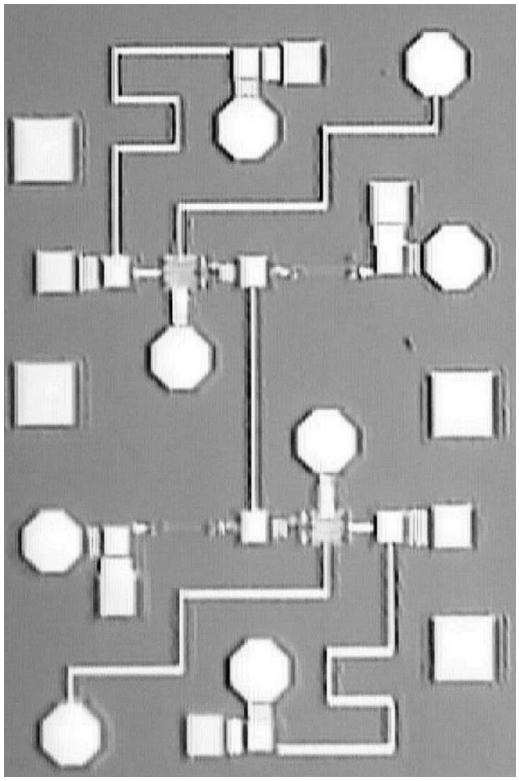

Fig. 5. Photograph of the Ka-band oscillator chip (0.9 mm × 1.3 mm).

V. Measured Performance

The fabricated chips were measured on a Cascade Microtech probestation. All RF connections to the chips were made using 200-μm-pitch coplanar probes while dc biasing was applied though probe needles.

A. K-Band Oscillator

For the K-band oscillator, stable oscillations at 19.3 GHz with 5-dBm output power were observed when the drain bias of 5 V was applied to both FET's. Fig. 7 shows the oscillation spectrum. It was found that the oscillators locked to each other even when the biasing conditions were slightly different. The variation of oscillation frequency and output power with drain bias is shown in Fig. 8. The gate bias was set at −0.5 V.

To investigate the phase relations between the oscillator outputs, a direct measurement technique using an injection-locking polar diagram is used [12]. Fig. 9 shows the measurement setup. The measurement principle is based on injection locking the oscillator with the synthesized oscillator in the vector network

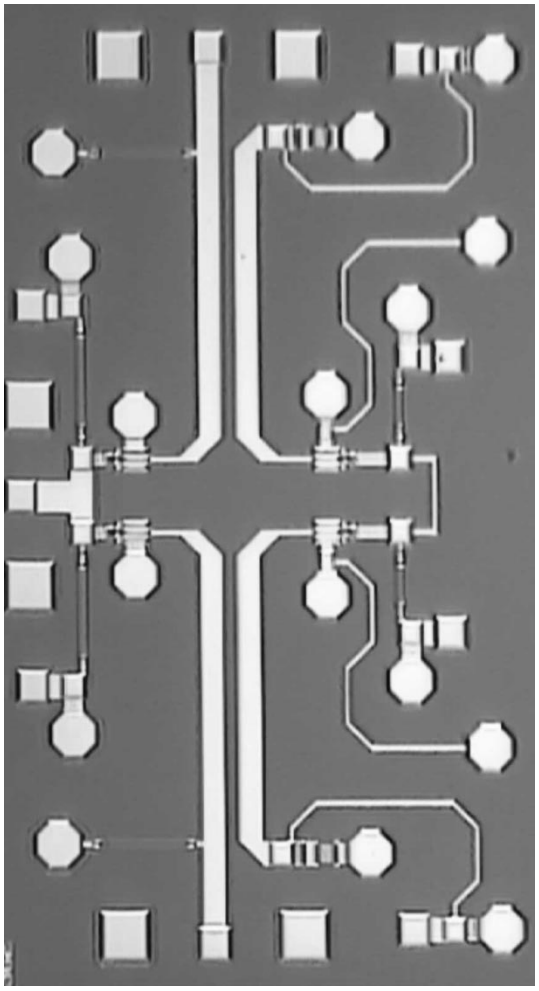

Fig. 6. Photograph of the Ka-band oscillator with integrated mixer chip (1.3 mm × 2.3 mm).

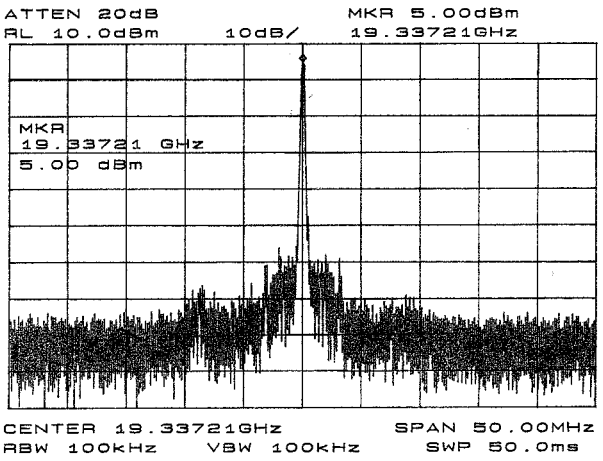

Fig. 7. Output spectrum of the K-band oscillator.

analyzer. A locking bandwidth of 10 MHz with 20-dB locking gain was observed on the spectrum analyzer. The network analyzer measures the phase of the reflection (S_{11}) and transmission (S_{21}) locking gain. Denoting the phase of the oscillator signal at the injection port and the opposite port by θ_1 and θ_2, and the phase of the injection signal by θ_3, the relationship between the two oscillator ports under locked conditions can be deduced as follow:

$$\theta_2 - \theta_1 = (\theta_2 - \theta_3) - (\theta_1 - \theta_3) = \text{phase}(S_{21}) - \text{phase}(S_{11}). \quad (14)$$

The injection-locking polar diagram obtained is shown in Fig. 10. Under locked conditions, S_{11} phase varies from 90° to –90°, while S_{21} phase varies from –90° to 90°, with increasing locking frequency. An exact antiphase relationship is maintained between the two oscillator outputs within the locking range, as shown by the phase plot in Fig. 11. This measurement also demonstrates that the balanced oscillator can be used as a form of active balun where the input signal is used for injection locking the balanced outputs.

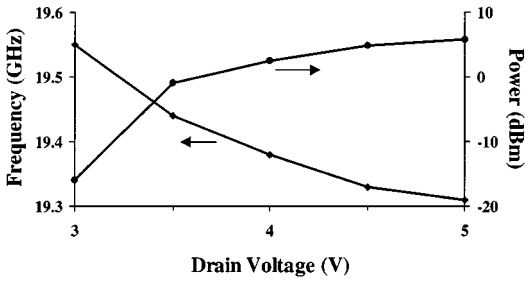

Fig. 8. K-band oscillator frequency and output power variation with drain bias. The gate bias is set at –0.5 V.

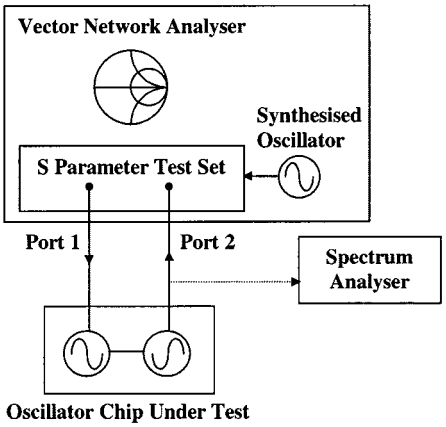

Fig. 9. Experimental setup for the phase measurement of the oscillator outputs by injection locking.

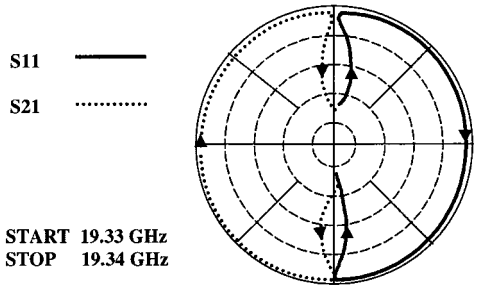

Fig. 10. Polar diagram of reflection (S_{11}) and transmission (S_{21}) injection gains of K-band oscillator. Arrows indicate direction of increasing frequency.

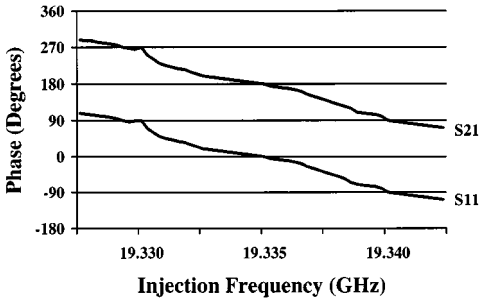

Fig. 11 Phase response of the K-band oscillator outputs relative to the injection signal at port 1.

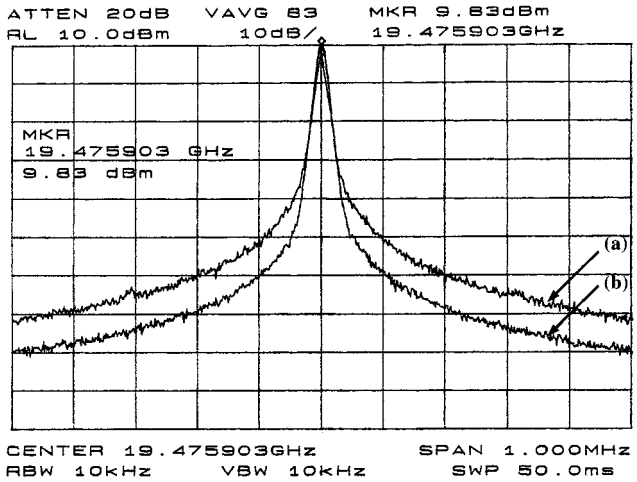

Fig. 12. Output spectrums of the K-band oscillator at $V_{\rm ds} = 5$ V, $V_{\rm gs} = 0$ V, and $V_{\rm ds} = 30$ mA. (a) When the opposite port is terminated with 50 Ω, operating at 19.30 GHz with 6.33-dBm output. (b) When the opposite port is open circuited, operating at 19.47 GHz with 9.83-dBm output.

The balanced oscillator can also operate as a power-combining oscillator when only one of the ports is loaded, leaving the other port open circuited. This can be considered as a monolithic implementation of the power-combining oscillator described in [11], with the use of FET's in place of diodes. The oscillator behavior of this configuration was investigated.

Fig. 12 shows the spectra of the power-combined output in comparison to one of the balanced oscillator outputs. For both cases, the oscillator is operating at $V_{\rm gs} = 0$ V, $V_{\rm ds} = 5$ V, and $I_{\rm ds} = 30$ mA. Besides an increase in power level by about 3 dB, a significant reduction in phase noise was also observed. At 100-kHz offset from carrier, the phase noise is about –90 dBc/Hz for the balanced outputs and –100 dBc/Hz for the combined output. This 10-dB reduction in phase noise can be attributed to the increase in the output power P_o as well as the external quality factor $Q_{\rm ext}$ of the oscillator when one of the loads is removed. Neglecting the effect of nonlinear reactances, the frequency fluctuations are inversely proportional to $P_o Q_{\rm ext}^2$ [13]. As the oscillator power is mainly dissipated in the external loads, removal of one of these loads increases both P_o and $Q_{\rm ext}$ by a factor of two. Thus, a 9-dB reduction in phase noise is expected, which is in good agreement with the observed result.

The variation of power level and frequency with the drain bias voltage of the power-combined oscillator output is measured and shown in Fig. 13. Comparing Figs. 8 and 13, the output

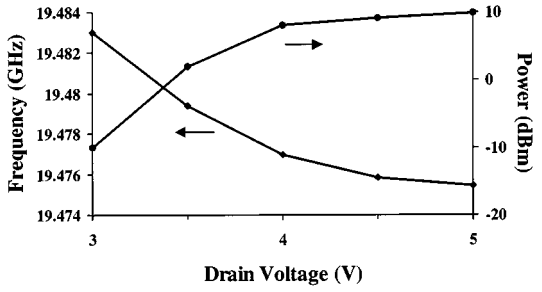

Fig. 13. K-band oscillator frequency and power variation with drain bias when the opposite port is open circuited. The gate bias is set at –0.5 V.

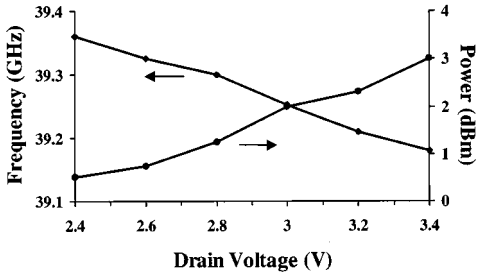

Fig. 14. Ka-band oscillator frequency and output power variation with drain bias. The gate bias is set at 0 V.

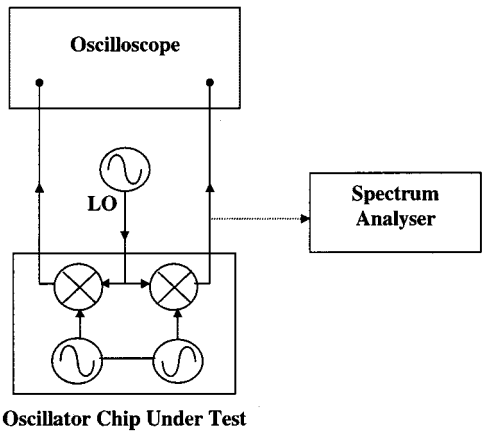

Fig. 15. Experimental setup for the low-frequency measurement of the down-converted oscillator outputs.

power is higher than the combined oscillator outputs of the balanced oscillator at low-bias voltages. The combined output frequency is also significantly less sensitive to the biasing voltage. Therefore, these measurements show that the outputs of the oscillator can be effectively combined without using any hybrids, with improvements in noise performance and frequency stability.

B. Ka-Band Oscillators

The Ka-band oscillator was measured on a spectrum analyzer using external mixers. Stable oscillations were observed around 40 GHz when the drain bias was varied from 2 to 3.8 V. The variation of frequency and power level with drain bias are shown in Fig. 14. The gate bias was set to 0 V.

Having verified the oscillation frequencies of the balanced oscillator under various biasing voltages, the oscillator chip with

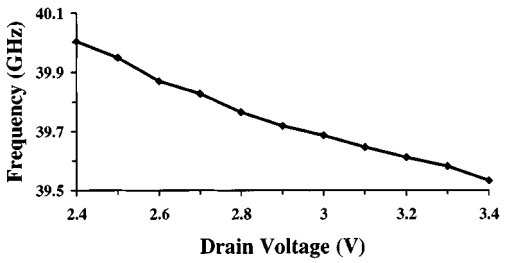

Fig. 16. Frequency variation with drain bias of the Ka-band oscillator with integrated mixer chip. The gate bias is set at 0 V.

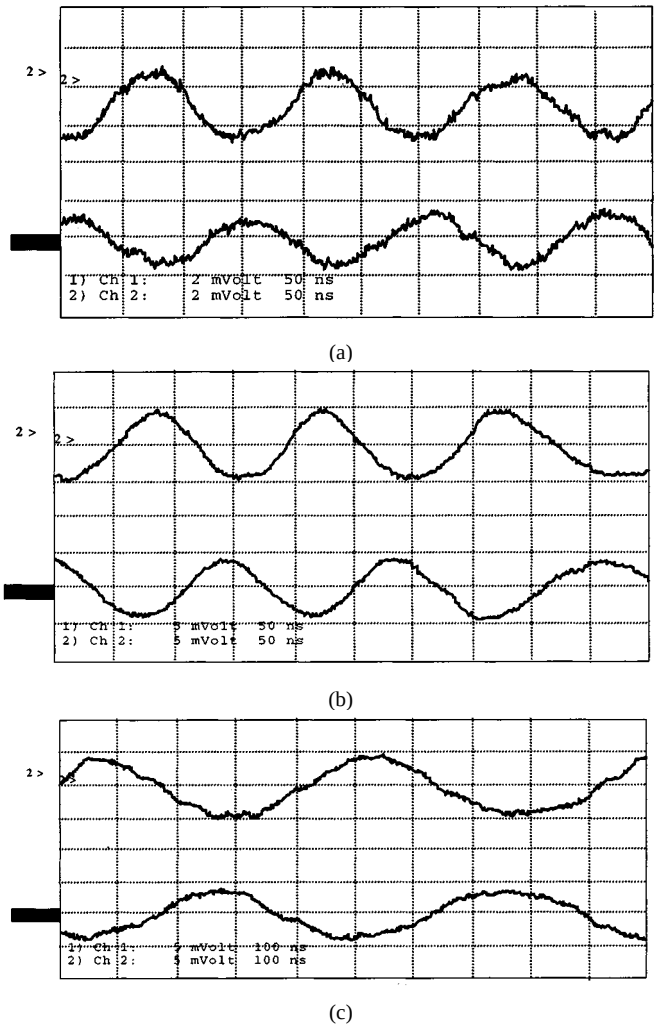

Fig. 17. Typical oscilloscope displays of the down converted Ka-band oscillator signals. (a) $V_d = 2.4$ V, LO $= 39.98$ GHz. (b) $V_d = 2.9$ V, LO $= 39.73$ GHz. (c) $V_d = 3.4$ V, LO $= 39.52$ GHz.

integrated mixers in Fig. 6 was measured under similar biasing conditions. The measurement setup is shown in Fig. 15. The LO for the down conversion is obtained from a synthesized oscillator. As the LO frequency is varied around 40 GHz, a down-converted IF signal is observed on the spectrum analyzer. By noting whether the IF increases or decreases as the LO is increased, the operating frequency of the oscillator can be deduced from the IF and LO frequencies. Fig. 16 shows the variation of the operating frequency of the oscillator when the bias is varied.

The down-converted signals are then displayed on the oscilloscope. Fig. 17 shows the typical waveform displays as the drain biased is varied. It is evident that the amplitude balance and antiphase relationship between the signals is maintained as the operating point is changed. This phase difference was always repeatable as long as the IF was low enough so that the cable lengths used in the experimental setup have negligible effect on the phase measurement. In the measurement, the LO is tuned to obtain an IF that is below 10 MHz.

VI. Conclusion

This paper has demonstrated that exact antiphase signals can be obtained directly from an oscillator without the need for external baluns or resonators. Instead, the phase and amplitude balances are obtained from the oscillator characteristics and the inherent symmetry in the circuit topology. This results in compact designs with excellent amplitude and phase balance performance, which is insensitive to process variations. The phase relationship has been verified by direct phase measurements based on injection-locking polar diagrams and with low-frequency measurements of the down-converted oscillator outputs. Measured results shows that the amplitude and phase characteristics are maintained throughout the operating frequency range of the oscillator. Therefore, this new oscillator is expected to find applications in balanced monolithic circuits where it can serve as an integrated oscillator generating accurate antiphase signals. In addition, the operation of the oscillator as a single output oscillator has also been demonstrated. Besides higher output power, the resulting oscillator also exhibits phase noise reduction and frequency stabilization. Thus, it also has significant potential in realizing multiple-device power-combining oscillators with enhanced performance.

Acknowledgment

The authors thank Prof. C. Aitchison for many valuable discussions.

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