A DC–20-GHz InP HBT Balanced Analog Multiplier for High-Data-Rate Direct-Digital Modulation and Fiber-Optic Receiver Applications

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***Abstract*—This paper reports on a dc–20-GHz InP heterojunction bipolar transistor (HBT) active mixer, which obtains the highest gain-bandwidth product (GBP) thus far reported for a direct-coupled analog mixer integrated circuit (IC). The InP HBT active mixer is based on the Gilbert transconductance multiplier cell and integrates RF, local oscillator, and IF amplifiers. High-speed 70-GHz f_T and 160-GHz $f_{\max}$ InP HBT devices along with microwave matching accounts for its record performance. Operated as a down-converter mixer, the monolithic microwave integrated circuit achieves an RF bandwidth (BW) from dc–20 GHz with 15.3-dB gain and benchmarks a factor of two improvement in GBP over state-of-the-art analog mixer IC's [1]–[9]. Operated as an up-converter, direct-digital modulation of a 2.4-Gb/s $2^{31}-1$ pseudorandom bit sequence (PRBS) onto a 20-GHz carrier frequency resulted in a carrier rejection of a 28 dB, clock suppression of 45 dBc, and less than a 50-ps demodulated eye phase jitter. The analog multiplier was also operated as a variable gain amplifier, which obtained 20-dB gain with a BW from dc–18 GHz, an third-order intercept of 12 dBm, and over 25 dB of dynamic range. A single-ended peak-to-peak output voltage of 600 mV was obtained with a ±35-mV 15 Gb/s 2^5-1 PRBS input demonstrating feasibility for OC-192 fiber-telecommunication data rates. The InP-based analog multiplier IC is an attractive building block for several wide-band communications such as those employed in satellites, local multipoint distribution systems, high-speed local area networks, and fiber-optic links.**

***Index Terms*—Fiber optics, InP HBT, limiter, mixer, multiplier, VGA.**

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I. Introduction

WIDE-BAND direct-coupled differential balanced multipliers are attractive for future communications that involve direct-digital modulation as well as wide-band reception and processing of high-data-rate digital signals. Fig. 1 illustrates the wide-band InP heterojunction bipolar transistor (HBT) multiplier monolithic microwave integrated circuit (MMIC) in these two applications. Fig. 1(a)shows a multiplier chip for direct modulation of a high data rate digital signal onto a microwave or millimeter wave carrier for subsequent line-of-sight transmission, and Fig. 1(b)shows a variable gain amplifier (VGA) (linear multiplier) for optimizing the dynamic range of a high- speed fiber-optic receiver.

In the first application, a wide-band multiplier is used for the direct modulation of high-speed data, which is transmitted at microwave or millimeter-wave carrier frequencies. Several broad-band wireless communications systems that transmit data at millimeter-wave frequencies are already established and include local multipoint distribution systems (LMDS), high-speed local area networks (LAN's), and broad-band satellite systems. In these applications, the modulation format is typically a form of spectrally shaped QPSK with symbol rates ranging from 50 Mb/s (LMDS) to several Gb/s (high-speed LAN's) with carrier frequencies up through Ka-band. This imposes a desire for wide-band operation on the RF input and output ports and high speed on the modulation $[I(t), Q(t)]$ port of the multiplier. By exploiting the high speed offered by InP HBT technology, the employment of a direct modulator can reduce modulator hardware complexity by eliminating one or more low-frequency IF stages in addition to the corresponding local oscillator (LO) sources and RF upconverter stages. This would simplify the modulator hardware and result in reduced size, weight, and cost. In the second application, given in Fig. 1(b), a wide-band analog multiplier can be used as a VGA in an automatic gain control loop of a high-speed fiber-optic receiver in order to optimize the receiver's SNR and bit error rate (BER). By applying a dc voltage on the modulation (LO) port, the MMIC can be operated as a linear multiplier or VGA in a feedback loop for automatically adjusting the signal levels introduced in the receiver. By fixing the voltage on the gain control port, the VGA can also function as a wide-band limiter amplifier. In either application, wide bandwidth (BW) is required for amplifying high data rate 10 Gb/s and above digital

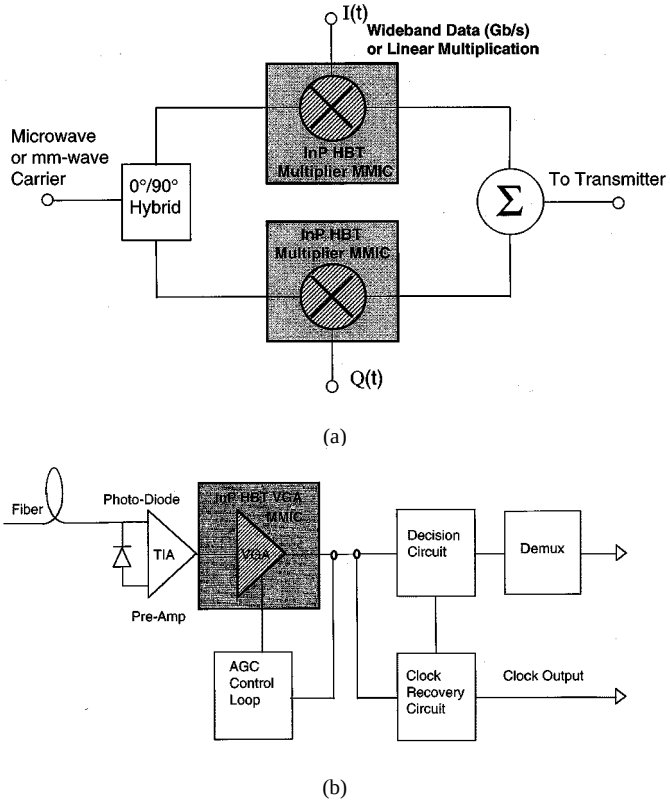


Fig. 1. Two wide-band InP HBT analog multiplier applications. (a) Direct modulation of high-speed data onto a microwave carrier. (b) Linear variable gain multiplier for high-speed fiber-optic receivers.

data streams such as those found in fiber-optic applications like SONET OC-192.

In both of these applications, the availability of a manufacturable InP HBT technology with high f_T and $f_{\max}$ enables the use of the traditional low-frequency analog design topologies at microwave frequencies. More specifically, an InP HBT-based Gilbert transconductance multiplier can provide dc coupling, differential balance, and high conversion gain performance over a multidecade microwave BW, which is preferred over the Schottky diode balanced mixer for wide-band digital communications operating in the microwave regime. In comparison, the Schottky diode balanced mixers used for microwave applications are typically limited to an octave in BW, operate single ended, and have substantial conversion losses.

Fig. 2 gives a summary of state-of-the-art wide-band analog balanced mixer integrated circuit (IC) gain-BW performance demonstrated with Si bipolar junction transistor (BJT), Si Ge BJT, CMOS, MESFET, InP high electron-mobility transistor (HEMT), GaAs HBT, and InP HBT technologies [1]–[9]. While high conversion gain can be achieved by Si CMOS and Si BJT technologies, they fall short of providing mixer BW's above 10 GHz. Also, although a record mixer RF BW was demonstrated by 0.1-μm InP HEMT technology [10], it fall short of providing the gain and GBP of the bipolar technologies. Compared to a fully self-aligned 0.6-μm silicon BJT-based analog mixer, which represents the previous best GBP of 60 GHz [8], the InP HBT-based analog mixer of this work obtains a GBP of 116.4 GHz, a factor of two improvement, and provides the best

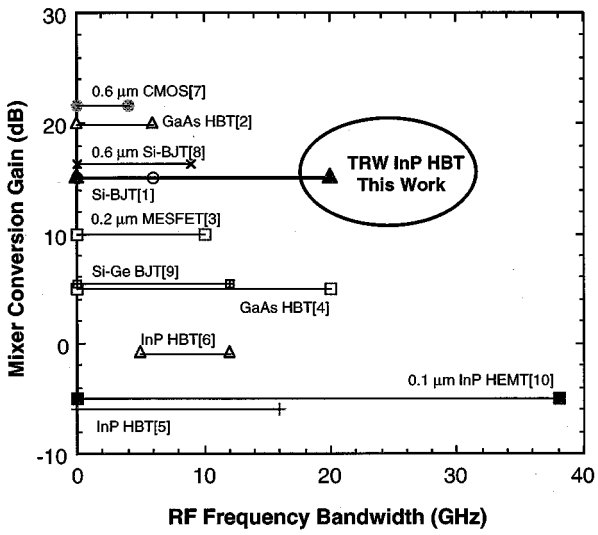


Fig. 2. Summary of state-of-the-art wide-band analog balanced mixer IC performance.

combination of gain (15.3 dB) and BW (>20 GHz) performance for the applications described above.

The following sections will describe the production InP HBT technology, detailed analog multiplier design, measured mixer and variable gain multiplier characteristics, and modulation–demodulation performance.

II. InAlAs/InGaAs-InP HBT Technology

The MMIC reported in this paper is based on an InAlAs/InGaAs-InP HBT device technology. Fig. 3 shows a cross section of TRW's InAlAs/InGaAs HBT device structure. The InAlAs/InGaAs HBT device epitaxy structure is grown by molecular beam epitaxy (MBE) on a semiinsulating 3-in InP substrate. Be and Si are used as p- and n-type dopants for the base and emitter/collector, respectively. The emitter incorporates a 750-Å InGaAs cap, which is highly doped to obtain low emitter contact resistance. The intrinsic emitter region is 1900-Å thick and doped to 5×10^{17} cm^{-3}. The base–emitter junction is compositionally graded to form manufacturable HBT's with very repeatable beta and $V_{\rm be}$ characteristics. The HBT dc current gain is typically >35 at a current density of $J_c = 40$ kA/cm^2. Fig. 4(a) illustrate the process uniformity of the intrinsic HBT $V_{\rm be}$ turn-on voltage for 100 3-in InP HBT wafers. More importantly for analog and digital circuit designs is the $V_{\rm be}$ matching characteristics illustrated in Fig. 4(b), which indicate excellent $V_{\rm be}$ match of 1.1 mV over several sampled wafers. The HBT device structure also incorporates a base–collector epitaxial with a base thickness of 800 Å uniformly doped to 3×10^{19}cm^{-3}, a 7000-Å thick n-type collector lightly doped to 1×10^{16}cm^{-3}, and an N+ sub-collector doped to 5×10^{18} cm^{-3}. The intrinsic mobility of the electrons in the InGaAs collector material allows the use of thick collector HBT's that can achieve practical breakdown voltages without significantly compromising the device f_T and $f_{\max}$. A high break down voltage $\rm BV_{ceo}$ of 8 V and $\rm BV_{cbo}$ of 13 V is obtained, which is suitable for most IC applications including cellular power amplifiers.

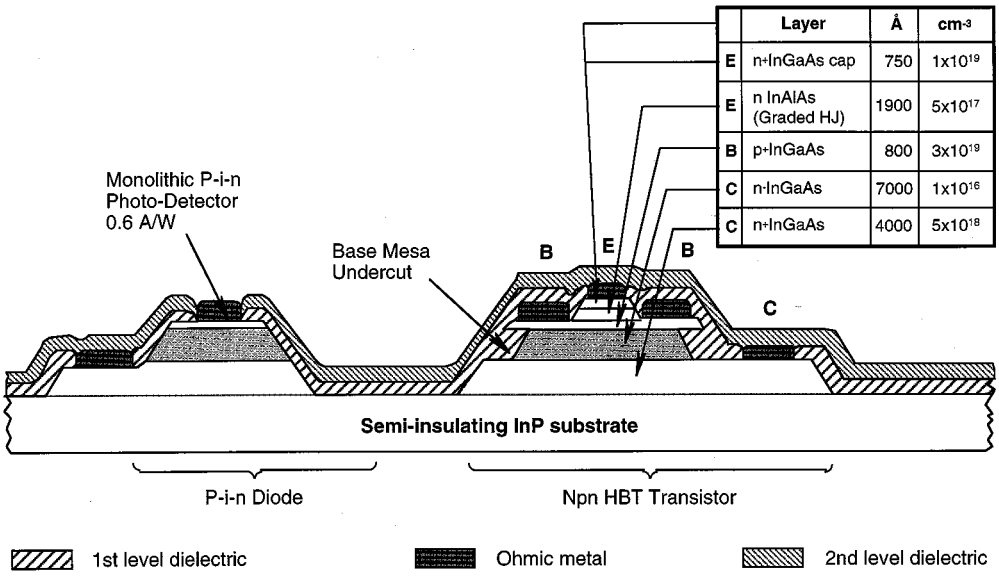
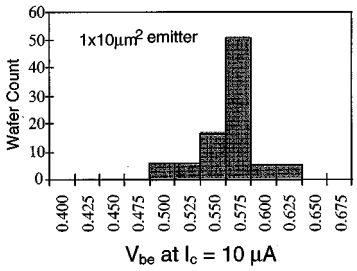
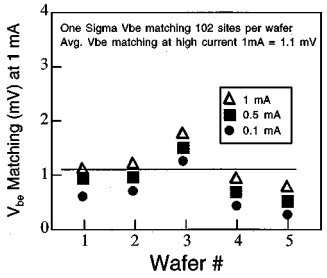


Fig. 3. Cross section of the InAlAs/InGaAs HBT device structure.



(a)



(b)

Fig. 4. (a) Process uniformity of the intrinsic HBT $V_{\rm be}$ turn-on voltage for 100 3-in InP HBT wafers. (b) HBT device $V_{\rm be}$ matching characteristics for several sampled wafers.

The manufacturable HBT fabrication technology employs a self-aligned base ohmic metal process, which is used to produce relaxed 1-μm emitter-width fingers. Due to the inherent device properties, the InP HBT's achieve peak f_T's and $f_{\max}$'s of 80 GHz and 200 GHz (from unilateral gain), respectively. These numbers are obtained from a 1×10 μm^2 quad-emitter HBT biased at a current density of $J_c = 50$–60 kA/cm^2 and a $V_{\rm ce} = 2.0$ V. Since the device frequency performance is controlled by a precision MBE growth technology high yields and uniform millimeter-wave device performance are obtained.

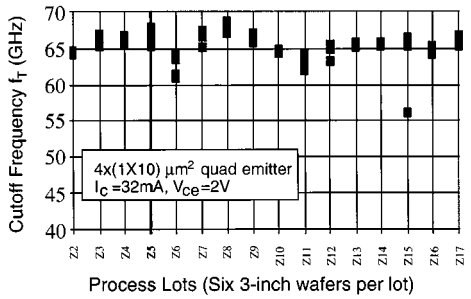


Fig. 5. Process trend chart of the InP HBT device cutoff frequency performance for 100 3-in InP wafers.

Fig. 5 illustrates the HBT device cutoff frequency performance for 100 3-in InP HBT wafers. The average f_T of a four-finger HBT is 65 GHz ±6%. The manufacturable high $f_{\max}$ and f_T of these InP HBT's make them well suited for most RF and opto-electronic applications.

III. Wide-Band Analog-Mixer Design

A block diagram schematic of the dc–20-GHz Gilbert analog mixer/VGA integrated circuit is shown in Fig. 6. The mixer integrates RF, LO, and IF amplifiers at each port of the Gilbert cell, which is differentially balanced and directly coupled at each port. The RF and LO amplifiers have dc to above 20-GHz 3-dB BW capability, while the IF output amplifier has a dc–18-GHz 3-dB BW. Compact microstrip matching networks comprised of a series microstrip line and shunt capacitor-series resistor are employed at each port to ensure flat broad-band gain and good return-loss response at the upper band edges of each amplifier. Throughout most of the design, 1×10 um^2 single-emitter HBT's are used, except for the output IF differential amplifier that employs 1×10 um^2 quad-emitter HBT's. All devices are biased at or near its optimal current density of 50–60 KA/cm^2.

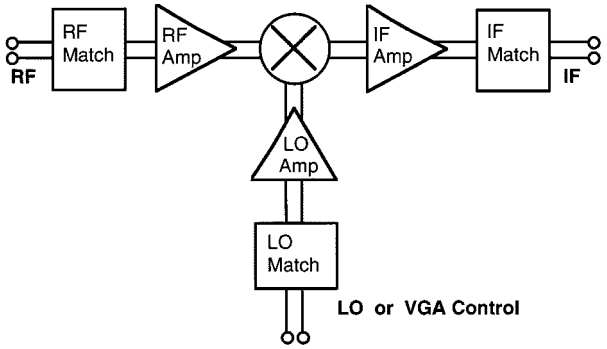


Fig. 6. Schematic of the dc–20-GHz InP HBT analog mixer/VGA circuit.

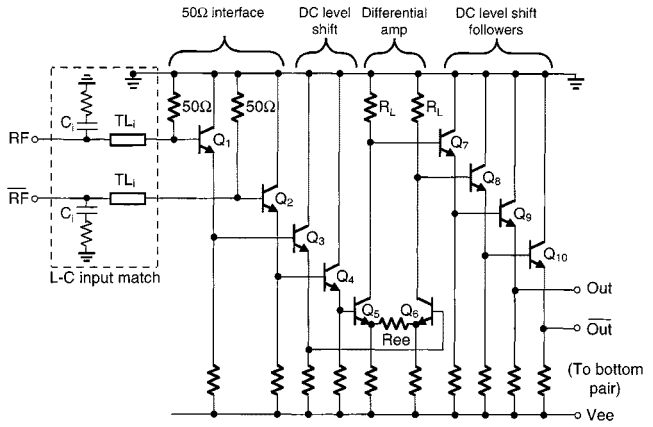


Fig. 7. Detailed schematic of the RF amplifier.

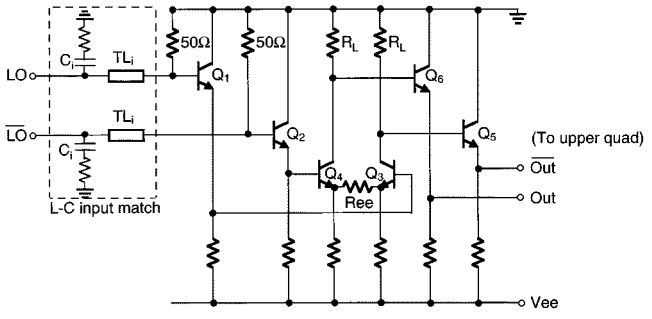


Fig. 8. Detailed schematic of the LO amplifier.

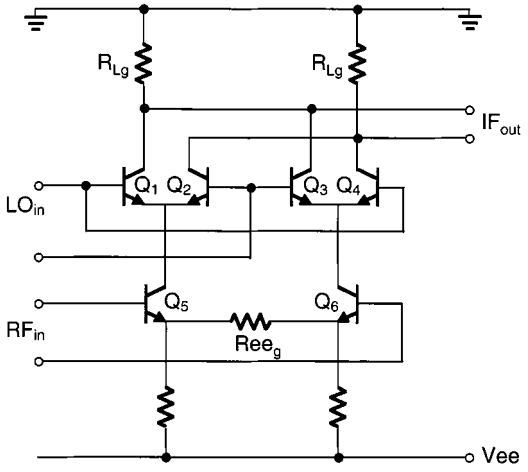


Fig. 9. Detailed schematic of the Gilbert cell multiplier core.

Fig. 7 shows the detailed schematics of the RF input amplifier stage, which is comprised of two successive emitter followers, an emitter degenerated differential amplifier, and two output followers, which feed into the bottom differential stage of the Gilbert cell mixer. The input follower has 50-Ω shunt resistors to match to the 50-Ω source. The series microstrip-line–shunt–capacitor input network is used to match to the capacitive looking impedance of the input followers at the upper band edge. The microstrip transmission line TL_i is 10 um $\times$ 250 um, while the input capacitor C_i is 0.3 pF. A 15-Ω resistor in series with the shunt capacitor is included to damp out any potential resonances that could result in excessive ringing or overshoot responses when a digital signal is applied at the input. The matching circuit results in excellent return loss >15 dB up through 20 GHz and flat broad-band gain performance beyond 20 GHz. Without the matching circuitry, the return loss becomes poorer than 10 dB at the upper band edge. The RF differential amplifier has an emitter degeneration of 5-Ω ($R_{\mathrm{ee}} = 10\,\Omega$) and a load resistance of 120 Ω.

The LO amplifier given in Fig. 8 is similar to the RF amplifier design, except the differential amplifier is followed by only one emitter follower level-shifting stage, which is fed into the top transistor quad of the Gilbert cell mixer. In addition, only one input follower stage precedes the differential amplifier, but has a similar passive *L-C* input matching network. The LO differential amplifier has a load resistor of 50 Ω and an emitter degeneration resistance of 5 Ω ($R_{\mathrm{ee}} = 10\,\Omega$). This LO amplifier operates from dc to 20 GHz and can accommodate a directly applied high-speed digital data stream for direct modulation applications. Since the input of the LO amplifier is directly coupled, a dc voltage can also be applied to either or both LO inputs in order to steer current in the Gilbert cell to obtain variable gain control from the RF input to IF output. Since the LO differential amplifier has gain, the input gain control range is only linear for an applied $\pm$75-mV dc control signal. In order to widen the linear gain control voltage characteristics for linear multiplier applications, a diode predistortion circuit can also be integrated with only a slight compromise of the LO BW response.

The mixer is comprised of the conventional Gilbert cell topology given in Fig. 9 and employs 50-Ω load resistors and 15 $\Omega$of emitter ($R_{\mathrm{eeg}} = 30\,\Omega$) degeneration resistance. A linear multiplier can easily be implemented by employing heavy emitter degeneration on the bottom differential pair instead of preceding the upper pair with a predistortion network; however, the lower pair is typically reserved as the unmodulated port in high-frequency design due to reduced Miller effect, which is a result of the low-impedance load provided by the Gilbert transistor quad $Q_{1\text{–}4}$. The output of the Gilbert cell is directly fed into the IF output differential amplifier. Fig. 10 gives a detailed schematic of the IF output buffer stage. This stage is comprised of three successive emitter followers, which provide mixer output buffering as well as a three diode level shift required to provide the proper dc voltage headroom for the output differential pair. Since the output differential amplifier must

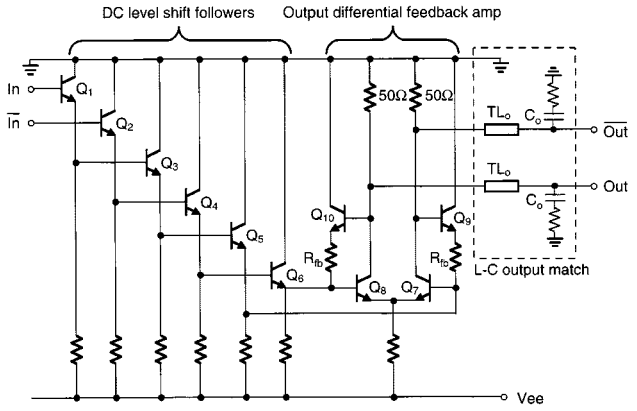


Fig. 10. Detailed schematic of the IF output buffer amplifier.

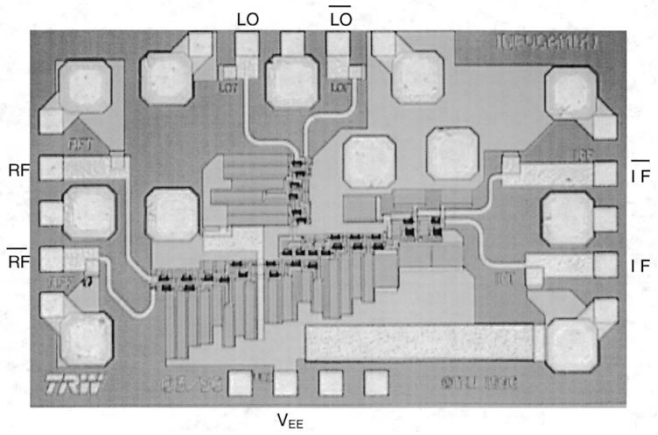


Fig. 11. Microphotograph of the InP-HBT analog mixer/VGA MMIC.

drive external 50-Ω loads and provide moderate voltage swings, large quad-emitter HBT's with a total periphery of 40 μm² are used in order to allow high current swings (20–30 mA). The capacitance due to this larger device periphery degrades the BW response of the IF output amplifier (and the RF path of the complete mixer MMIC) and, therefore, resistive feedback is employed in order to widen the gain response. The additional feedback follower transistors $Q_{9–10}$ help preserve the large signal BW as the IF amplifier goes into saturation. In addition, an output matching network comprised of a series transmission line TL_o and shunt output capacitance C_o is employed in order to improve the gain flatness and output return loss at the upper band edge. The values of these matching components are on the order of the RF and LO input matching network values. The resulting IF output stage is capable of dc–18-GHz BW response.

Fig. 11 shows a microphotograph of the InP HBT analog mixer/VGA MMIC. The complete MMIC contains 32 HBT devices, which are bias operated near their optimum $f_{\max}$ current density of 50–60 KA/cm². All HBT's are 1 × 10 μm² single emitter devices, except for two quad-emitter devices that comprise the IF output differential amplifier. The MMIC is 3-mil thick and incorporates small reactive ion etch (RIE) vias to support a microstrip matching medium and compact layout. The chip measures 1.4 × 0.9 mm² and is self-biased from a –6-V supply while consuming 190–240 mA.

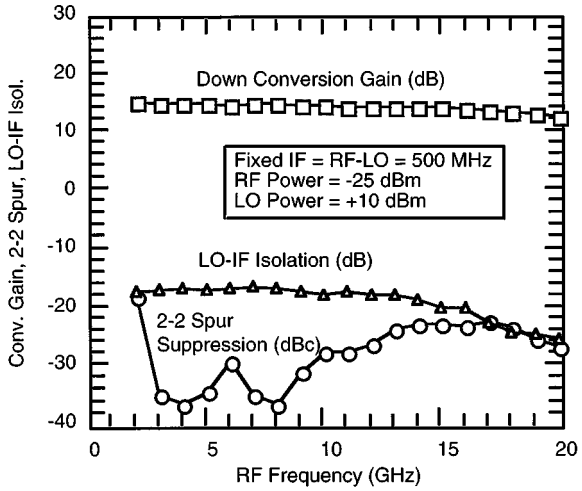


Fig. 12. Measured wide-band down-conversion mixer performance.

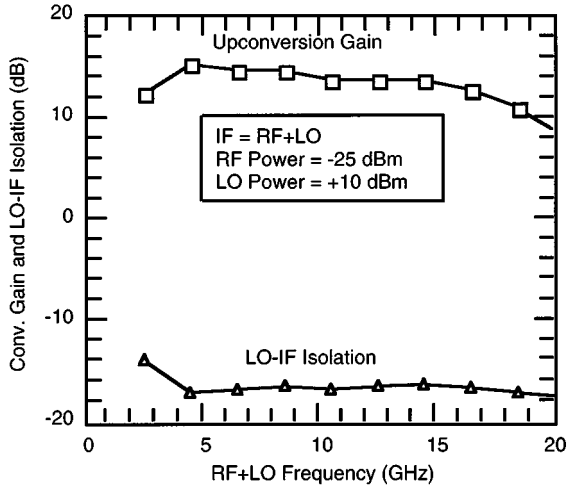


Fig. 13. Measured wide-band up-conversion mixer performance.

IV. Measured Performance

A. General RF Mixer Characteristics

The InP HBT analog multiplier was measured as both a down-converter (fixed IF) and up-converter. Fig. 12 shows the measured down-conversion mixer performance. With both RF and LO ports swept in frequency with a fixed IF frequency of 500 MHz, the mixer achieved 15.3-dB gain, and a 3-dB BW from dc to 20 GHz. With an input power near the mixer's 1-dB compression, a minimum 2-2 spur suppression of 20 dBc was obtained across the band. The LO–IF isolation is >17 dB with the integrated LO and IF amplifiers, which comprise over 20 dB of combined gain. The back-calculated LO–IF isolation of the Gilbert cell core is >32 dB up to 20 GHz and is indicative of good differential balanced operation that is dependent on the HBT's threshold matching performance. The up-conversion response in which both RF and LO are swept simultaneously is given in Fig. 13. This figures illustrates an up-conversion gain of 15 dB and a 3-dB BW of 16 GHz. The BW of the IF output amplifier determines the upper limit of the upconversion BW performance since the BW capability of both RF and LO ports

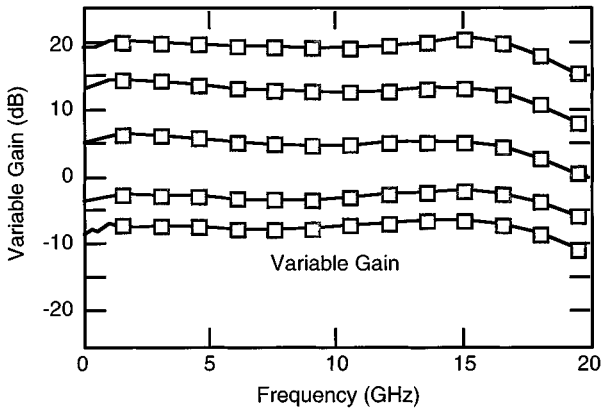


Fig. 14. Broad-band VGA response.

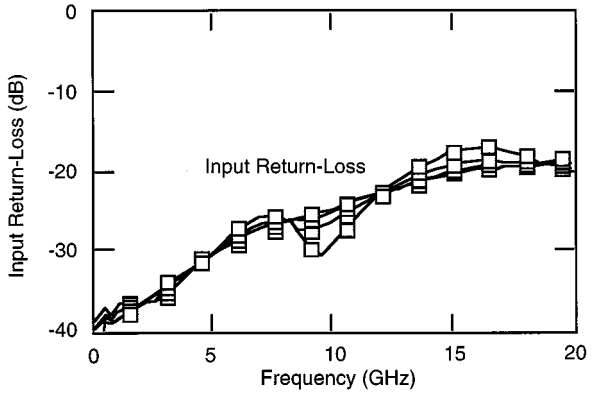


Fig. 15. Broad-band input return-loss performance over gain control.

extend beyond 20 GHz. Again, an LO–IF isolation on the order of 18 dB is achieved through most of the band.

B. General VGA Characteristics

The analog multiplier was also operated as a VGA by applying a dc voltage control signal to the LO port. Fig. 14 gives the dc–20-GHz variable gain response for various dc control voltages. The amplifier obtains flat gain control response from dc to 16 GHz with a 3-dB BW of 18 GHz. Over this BW a maximum gain of 20 dB and a dynamic range of 27 dB is obtained. The corresponding linear input control voltage is ± 75 mV. Since the variable gain port is high speed with a BW from dc to 20 GHz, this port can be used as a linear control port of a high speed complex modulator applications. With the employment of a predistortion circuit on this port, the linear gain control voltage can be extended to ± 500 mV. Fig. 15 shows the broad-band input return-loss performance over gain control. This figures shows the effectiveness of using microwave microstrip matching at the input port of the mixer. Greater than 15-dB return loss is achieved from dc to 20 GHz and is not sensitive to gain control. Without the input matching network, the return loss becomes poorer than 10 dB at the upper band edge. Fig. 16 gives the broad-band output characteristics of the VGA at maximum gain setting. The VGA obtains 20-dB associated gain from dc to 16 GHz, an third-order intercept (IP3) as high as 12 dBm, $P_{\rm sat}$ of 3.5 dBm, and $P_{1\,\rm dB}$ of > –1 dBm.

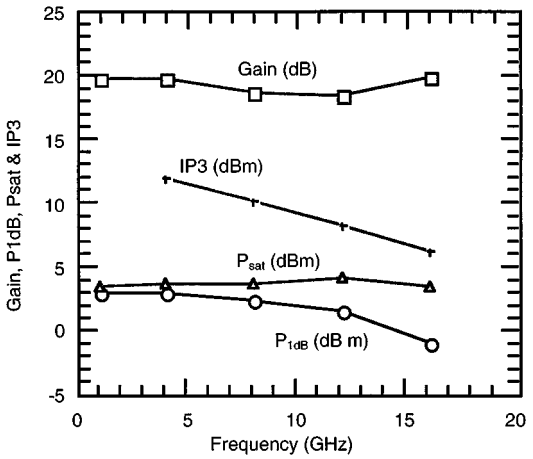


Fig. 16. Broad-band output characteristics of the VGA at maximum gain setting.

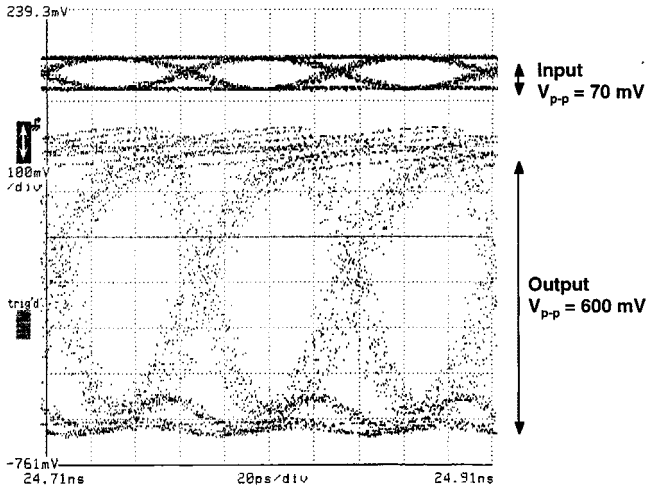


Fig. 17. Single-ended driven VGA eye diagram response to a ± 35-mV 15-Gb/s $2^5 - 1$ PRBS input signal.

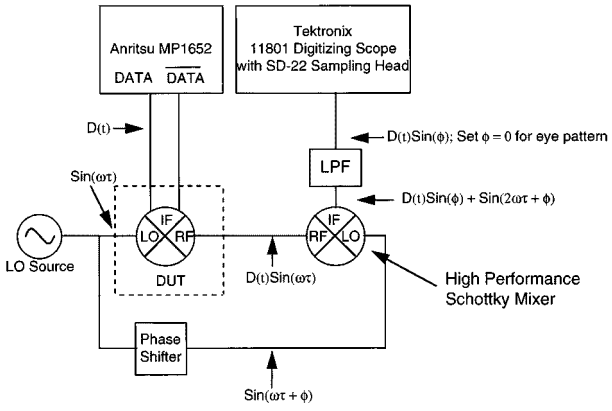


Fig. 18. Block diagram of the modulator–demodulator test measurement system used to evaluate the InP HBT multiplier.

To demonstrate its feasibility for high data rate limiting and detecting applications, the eye diagrams of the single-ended driven VGA at maximum gain setting was obtained (see Fig. 17). This figure illustrates good eye opening in response

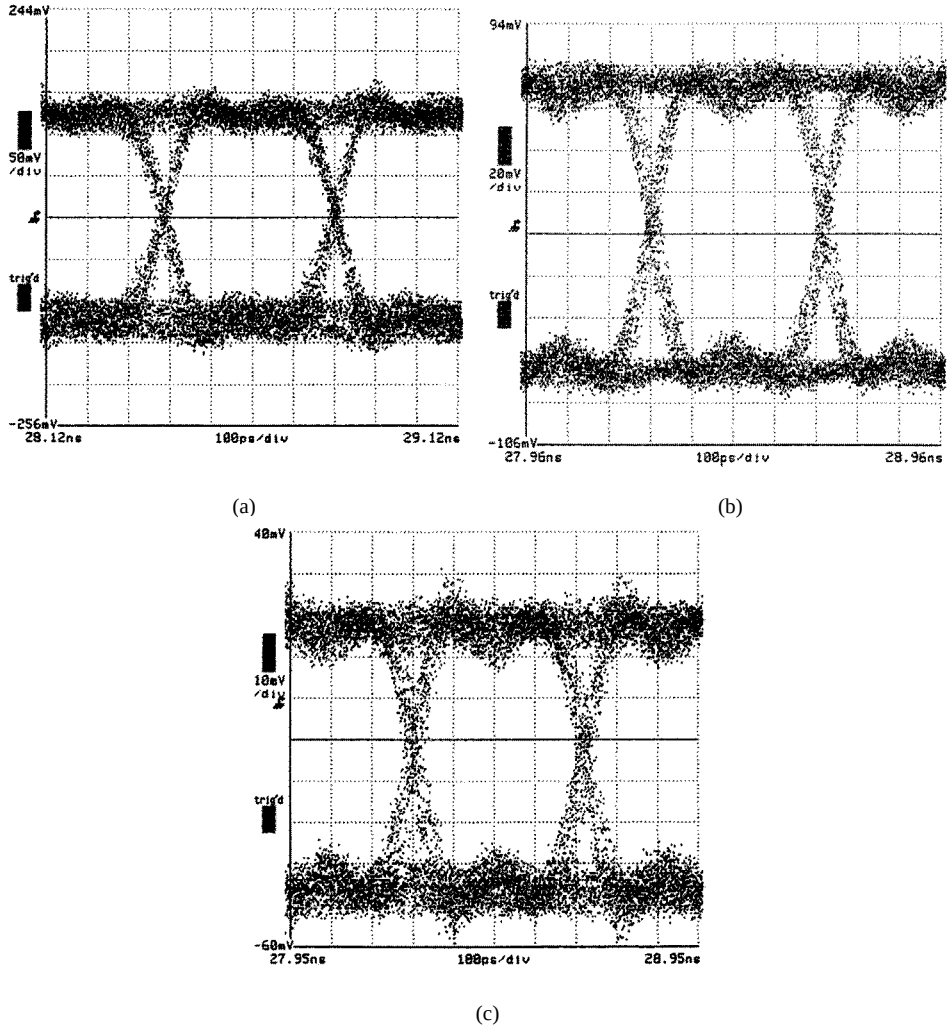


Fig. 19. 2.4-Gb/s demodulated eye diagrams for carrier frequencies of (a) 10, (b) 16, and (c) 20 GHz.

to a ±35-mV 15-Gb/s pseudorandom bit sequence (PRBS) input signal. The singled ended output signal was 600 mV peak-to-peak with a gain of 18.7 dB.

C. High-Speed Direct Digital-Modulator–Demodulator Demonstration at Microwave Frequencies

In order to demonstrate the analog mixer's direct-modulation capability, the MMIC was measured in a modulator–demodulator test measurement system, shown in Fig. 18. The device-under-test (DUT) is the InP HBT analog multiplier, which is fed differentially into the IF (labeled LO on the MMIC schematics) modulating port by an Anritsu MP1652 signal generator. The Anritsu produced a $2^{31}-1$ PRBS, which was fixed at a data rate of 2.4 Gb/s to demonstrate the high-speed direct-modulation capability. This modulation was superimposed onto 10-, 16-, and 20-GHz carriers provided by the LO signal source generator fed into the LO port (labeled RF on the MMIC schematics). This modulated carrier is then demodulated using a high-performance Schottky diode mixer, low-pass filtered, and then displayed on a Tektronix 11 801 Digitizing Scope with a SD-22 sampling head. A low-pass filter is used to filter out the carrier signal before being displayed. A variable phase shifter is employed on the LO port of the demodulator mixer and is adjusted to maximize the amplitude of the demodulated eye response. Fig. 19 illustrates the demodulated eye diagrams for 10-, 16-, and 20-GHz carrier frequencies. Each of the eye diagrams have very well-defined eye diagrams, indicative of excellent modulator performance. The observable overshoot is believed to be due to the pattern generator's interaction with the RF cables at the harmonic frequencies. This was verified by connecting the Anritsu directly to the Tektronics scope through an RF cable and observing the ringing response. The overshoot ringing was subdued by employing the low-pass filter, but did not completely eliminate the subtle overshoot characteristics. Table I

TABLE I
2.4-Gb/s DEMODULATED EYE CHARACTERISTICS

Carrier Frequency (GHz)	Phase Jitter (pS)	DC Output Offset Voltage (mV)
10	30	0
16	50	0
20	50	12

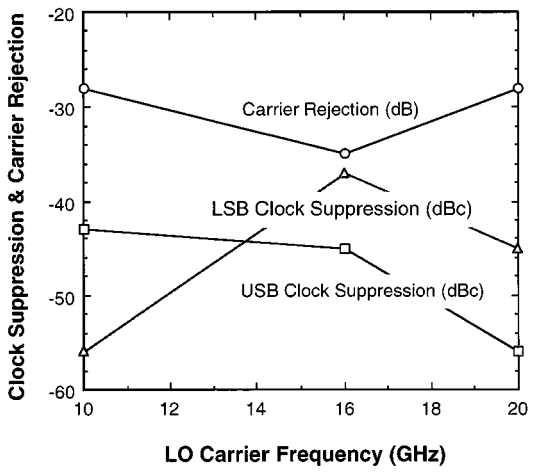


Fig. 20. Carrier rejection and clock suppression performance as a function of carrier frequency.

summarizes the demodulated eye phase jitter and dc offset of the multiplier as a function of carrier frequency. A demodulated phase jitter of 30 ps was obtained for a 10 GHz carrier while 50 ps was obtained for 16- and 20-GHz carrier performance. The corresponding dc offset voltage is immeasurable for the 10- and 16-GHz carriers, and only 12 mV was measured for the 20-GHz carrier. Note that the demodulated eye diagram characteristics reflect both modulator DUT and demodulator characteristics. Thus, these measured characteristics may be interpreted as the conservative performance of the InP HBT direct-modulator DUT. Finally, carrier rejection and clock suppression were directly measured at the output of the DUT using a spectrum analyzer and is shown in Fig. 20. For the 2.4-Gb/s modulated 20-GHz carrier, a carrier rejection of 28 dB was obtained, while lower side-band and upper side-band clock suppressions of 45 and 56 dBc, respectively, were also obtained. These measurements indicate that excellent direct-modulation performance can be achieved up to the mixer's conversion-gain band edge of 20 GHz.

V. Conclusion

This paper demonstrates an InP HBT analog Gilbert cell mixer/VGA, which achieves the widest conversion-gain–BW product reported for an analog IC mixer. The availability of the high-speed InP HBT technology enabled the analog multiplier to demonstrate 2.4-Gb/s direct modulation at 20 GHz and 15-Gb/s VGA-limiter amplifier performance for high —data-rate wide-band digital communications systems. In order to pursue higher output voltage limiter amplifier, optical mod-driver, and power amplifier applications for wide-band millimeter-wave frequency operation, InP collector epitaxy double heterojunction bipolar transistors (DHBT's) are being developed for the next iteration of these circuit designs. Combined with a manufacturable high-speed InP HBT technology, the analog mixer/VGA MMIC can become an enabling building block for future high-data-rate systems employing direct-digital modulation–demodulation, and fiber-optic communication links for satellite, millimeter-wave digital radio, and fiber-optic telecommunications.

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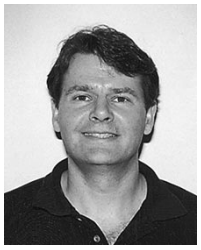

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