Short Papers

A Single-Chip SI-Bipolar 1.6-GHz VCO with Integrated-Bias Network

M. Zannoth, J. Fenk, A. Springer, and R. Weigel

***Abstract*—A single-chip 2.7-V voltage-controlled oscillator (VCO) with an integrated-bias network has been implemented in an Si-bipolar process with an f_T of 25 GHz. With an on-chip resonator consisting of vertically coupled inductors and varactor diodes, an oscillation frequency of 1.56 GHz was measured. A careful design of the oscillator and bias network was necessary to achieve a phase noise performance of –139 dBc/Hz at 4.7 MHz off carrier. The tuning sensitivity was 100 MHz/V, which is sufficient to compensate for production tolerances. The VCO can be used as a building block for single-chip transceivers in digital European cordless telephone or global system for mobile communication systems.**

***Index Terms*—Analog integrated circuits, bias networks, bipolar RF, RF oscillators.**

I. Introduction

Since cost is of major concern for all wireless communication products, a large research effort is put into the task of a complete integration of RF and IF oscillators. Up to now, these are one of the remaining building blocks that are difficult to integrate into a single chip transceiver. At present, discrete modules or external *LC* tanks are used because of the poor phase noise performance and high sensitivity to production tolerances integrated components suffer from. With a given maximum power consumption, the phase noise is limited by the quality factor of the integrated inductor. With external elements, the quality factor of the resonator is about two orders larger than that of an integrated type and the tolerances are much less. With integrated capacitors, a tolerance of ±10% is typical. This leads to large variations of the center frequency, thus, a large tuning range is recommended to be able to achieve the desired frequency. As supply voltages of battery-driven circuits are very low (about 3 V), large tuning constants are required, which make the system sensitive to noise injected by bias networks. Especially when considering the noise performance of an oscillator, the bias network has to be included in the design process. We present a single-chip voltage-controlled oscillator (VCO) with an integrated-bias network, which was optimized with respect to the noise behavior. The oscillator covers a wide frequency range and is, therefore, suitable for various wireless communication systems.

II. Integrated Oscillator

The oscillator core consists of a differential amplifier with positive feedback (Fig. 1), which is realized with vertically coupled inductors [1].

For attaining a good phase noise performance, the voltage swing at the resonator must be maximized [2]. In the described topology, the upper and lower limits for the voltage swing are given by the conditions that forward biasing of the base–collector diode has to be avoided and that a minimum value of collector–emitter voltage of the current source (and, therefore, a minimum base voltage $V_{\rm Bias}$) has to be kept to prevent the current source from saturating. The saturation would cause a current injection into the substrate, resulting in crosstalk in other building blocks on the same substrate.

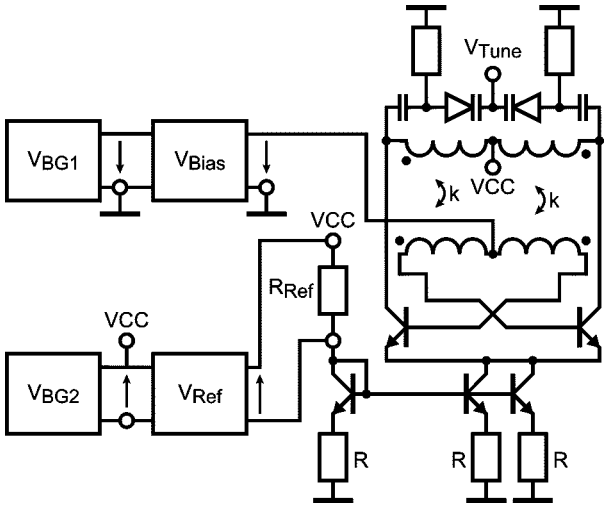

Fig. 1. Schematic of the biased oscillator.

To prevent the base–collector diode from getting forward biased, a maximum bias voltage of 1.7 V is calculated from

$$V_{\max} = (V_{CC} - V_{\rm res}/2) + V_D - V_{\rm res}/2 \qquad (1)$$

where the maximum allowed base–collector diode voltage is $V_D = 0.6$ V, $V_{CC} = 2.7$ V, and the maximum amplitude at the resonator is $V_{\rm res} = 1.6\,V_{\rm pp}$. If $V_{\max}$ is exceeded ($V_{\rm Bias} > V_{\max}$), the amplitude of the resonator voltage would be limited by the base–collector diode and additional damping would be applied to the resonator. This would cause a reduction of the quality factor and a rise of phase noise. We choose a bias voltage$V_{\rm Bias}$ of 1.6 V, which leads to an emitter voltage of 0.75 V ($V_{\rm BE} = 0.85$ V). When accounting for a minimum collector–emitter voltage of 450 mV at the current source, a negative feedback (resistor R in Fig. 1) of 300 mV can, therefore, be applied, which helps to reduce noise coupling from the reference voltage.

III. Integrated Resonator

The capacitance of the tank is built up by two varactor diodes with series capacitances. These capacitors are introduced to decouple the anode of the tuning diode from the supply voltage and to reduce the voltage swing at the diode to avoid forward biasing. They also linearize the tuning characteristic (Fig. 2).

Three metal layers are used to build the vertically coupled inductors. To maximize the quality factor of the inductor, hollow inductors are used, as shown in [3]. The spacing between the conductors is minimized to the lowest value possible to maximize the inductance [5], [4]. The width of the inductor is optimized for minimum series resistor. A compromise between dc resistance, which decreases with growing width, and substrate losses and skin effect, which increase with the width, has to be found [5]. The quality factor of the primary inductor

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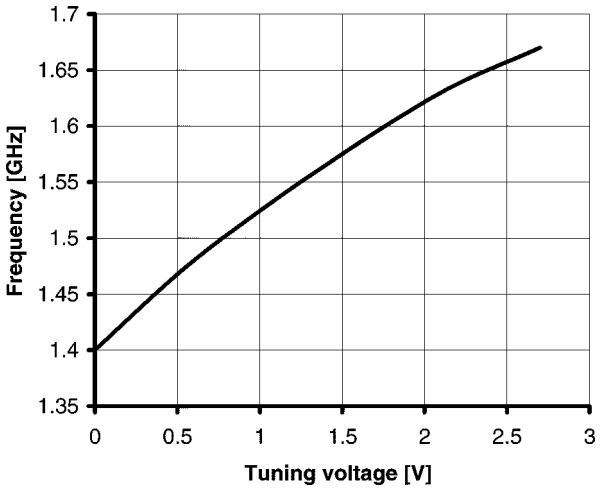

Fig. 2. Tuning characteristic.

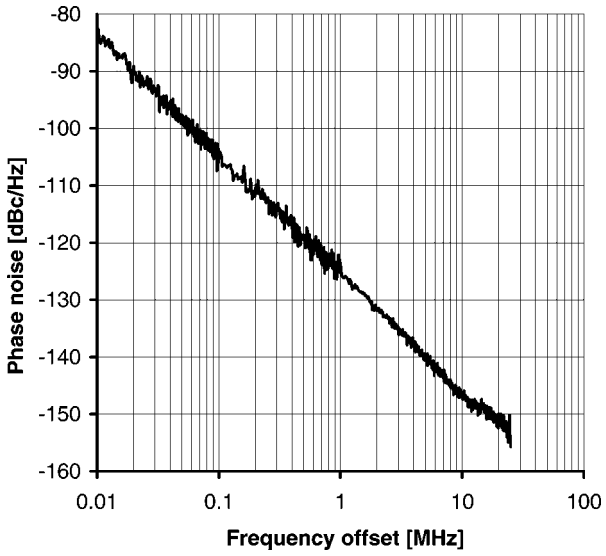

Fig. 3. Measured phase noise.

TABLE I
NOISE CONTRIBUTORS OF THE BIASED OSCILLATOR

Noise contributor	noise fraction
Oscillator transistors	34 %
Resonator elements	28 %
Bandgap with current generation	20 %
ESD-protection resistor	15 %
Bandgap with levelshift for V_{Bias}	3 %

TABLE II
SUMMARY OF THE VCO CHARACTERISTICS

Current of oscillator core	11 mA
Current of amplifier	5 mA
Current of bias network	6 mA
Output power	−11 dBm
Center frequency	1.56 GHz
Tuning constant (KVCO)	100 MHz/V
Tuning range (0, ⋯, 2.7 V)	270 MHz
Phase noise @100 kHz	−105 dBc/Hz
Phase noise @4.7 MHz	−139 dBc/Hz
Size of one inductor	300 μm × 300 μm

was estimated from the equivalent circuit to be about five at a frequency of 1.5 GHz.

IV. BIASING NETWORK

The noise performance of an oscillator is determined by the energy stored in the resonator, the quality factor of the resonator, and the noise of the bias network. For minimum noise, we used inductive feedback, as described in [1]. With this kind of coupling, the bases of the transistors can be applied to a voltage source for biasing. Blocking capacitors can be applied to reduce noise and spurious signals generated by the source. Since inductive coupling is used, most of the noise generated by the source is suppressed as a common-mode signal. However, when the output voltage reaches its maximum, one of the transistors is nearly in saturation and the other is blocked. In this case, the disturbances are not common-mode ones anymore, and a voltage source with minimum noise must be used. In our design, a Widlar Cell [6] in combination with a level shifter is used to realize a temperature-stabilized voltage source for generating the 1.6-V bias voltage where the oscillator has its optimum bias point. This voltage has the same constant temperature dependence as the bandgap reference. The current of this biasing block is about 2 mA. A simulated noise voltage of 25 nV/$\sqrt{\text{Hz}}$ can be achieved, which makes up only 3% of the total oscillator noise corresponding to Table I, in which a list of noise contributors from simulation results is shown. The simulations are carried out by means of a nonlinear analysis in the time domain [7] with the use of a commercial simulator.

To generate the current for the differential pair of the oscillator, a current mirror is used (Fig. 1). A tradeoff between noise performance and power consumption in the design of the current mirror had to be found as the mirror factor influences both quantities conversely. With the used value of six, a good performance with respect to noise and power consumption could be achieved. The reference current is generated by applying a reference voltage [6] to an external resistor. Due to the production tolerances of about ±15%, an internal resistor cannot be used. Current mirror and the reference resistor are stacked for minimum power consumption (Fig. 1).

In the presented design, two reference generation blocks are used to prevent spurious coupling across the substrate from the oscillator current to the bias voltage and vice versa. With the described concepts, the noise contributions of the bias blocks are reduced to a level where they do not dominate the oscillator performance. From simulation, we see that the highest noise contribution (about 34%) is generated by the transistors of the differential pair. The elements in the resonator follow with about 28% and the biasing blocks contribute to about 23% of the total noise. The necessary electrostatic discharge (ESD)-protection resistor at the tuning input makes up about 15% noise, as the white noise generated by this resistor is directly modulated to the oscillator frequency, where it can be seen as additional phase noise.

V. EXPERIMENTAL RESULTS

The realized integrated VCO includes a complete internal biasing network with only one external resistor for adjusting the current. It was produced in an Si-bipolar technology with a transit frequency of 25 GHz. The described optimized chip design with respect to phase noise minimization resulted in a performance of −139 dBc/Hz at a frequency offset of 4.7 MHz (see Fig. 3 and Table II). That meets the digital European cordless telephone (DECT) specification for transmitters and receivers with a sufficient margin for production tolerances and, thus, the VCO can be also used as an IF oscillator in global system

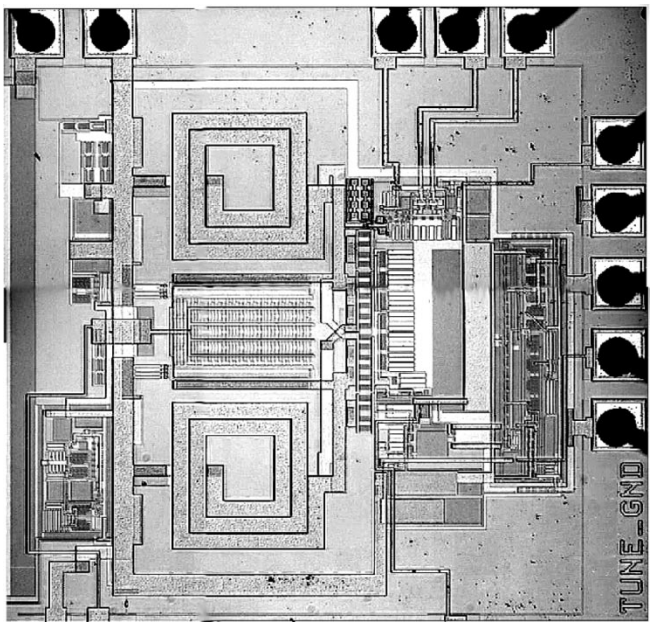

Fig. 4. Die photograph.

for mobile communication (GSM) systems. The variation of the phase noise versus tuning voltage is about 4 dB. Variations of the supply voltage from 2.4 to 3 V result in a phase noise variation of about 2 dB. Minimum phase noise is achieved at 2.7 V, the value for which the circuit was designed. For using this VCO in different systems, the center frequency can be adjusted to the required value by changing the size of the varactor diodes. An oscillation frequency range from 1.3 to 2 GHz can be realized without changing the inductor. The tolerances due to production in the center frequency result from the variations of the capacitance ($\pm 10\%$) of the resonator. The printed inductor has negligible variations of its inductivity. These tolerances lead to a variation of ±5% in frequency that has to be compensated for by the tuning range of the oscillator. At a center frequency of 1.56 GHz, the VCO has a tuning constant of 100 MHz/V, as shown in Fig. 2, thus, tolerances of $\pm 5\%$ in frequency can be compensated for with a tuning voltage in the range from 0.4 to 2.4 V. With an integrated buffer amplifier, which is only applied for the characterization of the circuit, the oscillator has an output power of −10 dBm at 50 Ω and a total current consumption of 22 mA. Without the amplifier for the 50-Ω output, 5-mA current can be saved. The oscillator core requires about 11 mA at a supply voltage of 2.7 V. A die photograph is shown in Fig. 4.

VI. Conclusion

In this paper, a single-chip 2.7-V VCO with an integrated-bias network was presented. The circuit was fabricated in Si-bipolar technology with an f_T of 25 GHz. The VCO has a phase noise performance of −139 dBc/Hz at 4.7-MHz frequency offset from the carrier at 1.56 GHz. With its tuning constant of 100 MHz/V, it can be used for mass production, as frequency variations due to production can be compensated for. As the bias network for the circuit is also integrated, the presented VCO can be used in truly single-chip transceivers for DECT and GSM systems.

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A Low-Power 15-GHz Frequency Divider in a 0.8-μm Silicon Bipolar Technology

Herbert Knapp, Wilhelm Wilhelm, and Martin Wurzer

***Abstract*—In this paper, we present a low-power static frequency divider with a divide ratio of eight. It operates up to 15 GHz, consuming only 22 mA from a 3.6-V supply. The chip is manufactured in a 0.8-μm silicon bipolar production technology with a cutoff frequency of 25 GHz. The circuit has a single-ended input and output and is mounted in a six-pin SOT363 plastic package.**

***Index Terms*—Frequency conversion, microwave bipolar integrated circuits.**

I. Introduction

The fast-growing mobile communications market has led to the introduction of numerous integrated circuits operating in the range of 0.9–2.5 GHz. Frequency dividers, dual-modulus prescalers, and single-chip phased-locked loops (PLL's) operating at these frequencies are available from many manufacturers. These devices are mostly manufactured in inexpensive silicon bipolar or BiCMOS technologies. With these devices, frequency synthesizers can be realized at low cost and low parts count.

For applications requiring a synthesizer operating at frequencies of 10 GHz or more, no single-chip PLL's are available and more complex solutions are needed. Higher frequencies can be generated by using a phase-locked oscillator at low frequencies, followed by one or several multiplier stages. This solution requires the use of filters to remove the fundamental frequency and undesired harmonics.

Another common solution is shown in Fig. 1. In this circuit, the frequency range of a single-chip PLL is extended by a fixed-modulus divider or prescaler. Since the voltage-controlled oscillator (VCO) operates at the desired output frequency, no filters are required.

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The output frequency of the circuit shown in Fig . 1 is

$$f_{\mathrm{VCO}} = f_{\mathrm{REF}} \cdot N \cdot K = \frac{f_{\mathrm{XTAL}}}{R} \cdot N \cdot K. \tag{1}$$

The frequency step size at the output of the synthesizer is

$$f_{\mathrm{STEP}} = K \cdot f_{\mathrm{REF}} \tag{2}$$

compared to

$$f_{\mathrm{STEP}} = f_{\mathrm{REF}} \tag{3}$$

if no prescaler is used. For a given channel spacing this means that the reference frequency of the PLL has to be decreased by a factor of K. This leads to a longer settling time of the PLL and it is, therefore, desirable to keep K as small as possible. A low overall divide ratio of the PLL is also important for achieving low phase noise of the output signal. The lower limit for K is given by the maximum input frequency of the divide-by-N circuit.

Frequency dividers operating at 10 GHz or more are commercially available and dividers operating at much higher frequencies have been presented [1]. These circuits are mostly fabricated in compound semiconductor technologies. For low-cost applications, however, the use of mainstream silicon bipolar technologies is preferable. Today's silicon bipolar technologies reach cutoff frequencies in the range of 20–50 GHz, making them an attractive choice for multigigahertz circuits. Silicon bipolar frequency dividers operating up to 35 GHz (measured on wafer) have been published [2], and an 18-GHz divider mounted in a surface-mount package has also been reported [3].

It was the aim of this work to develop a low-power fixed-modulus divider with a guaranteed operating frequency of at least 12 GHz using a silicon bipolar production process with a cutoff frequency f_T of 25 GHz. Important design goals were lowest possible power consumption and operation over a wide range of supply voltages. A divide ratio of eight was selected for the divider because this leads to an output frequency below 2 GHz, which can be handled by inexpensive components designed for mobile communications. The main challenge of the design was to achieve low power consumption although the circuit has to operate close to the cutoff frequency of the transistors. The choice of an SOT363 plastic package poses severe restrictions on the chip size. Due to the limited number of pins, only a single-ended input and output are possible.

II. Fabrication

The circuit was fabricated through Infineon Technologies B6HF silicon bipolar production technology [5]. This double-polysilicon self-aligned technology uses 0.8-µm lithography and is compatible to the standard 0.8-µm CMOS processing environment. It achieves a cutoff frequency f_T of 25 GHz and a ring oscillator gate delay of 25 ps. Apart from high-speed n-p-n transistors, the technology provides lateral p-n-p transistors, linear capacitors with a specific capacitance of 2 fF/µm^2, and a three-layer metallization.

The layout of the frequency divider was carefully optimized to keep critical paths short and to reduce parasitic capacitances. Only two of the three available metallization layers are used to reduce manufacturing cost. Due to the use of a very small SMD package, the overall chip size is restricted. The chip measures only 536 µm × 476 µm (Fig. 4).

III. Circuit Design

The frequency divider consists of three asynchronous divide-by-two stages to achieve the desired overall divide ratio of eight (Fig. 2). Each of these stages consists of a master–slave D-type flip-flop with feedback from the inverted output to the data input.

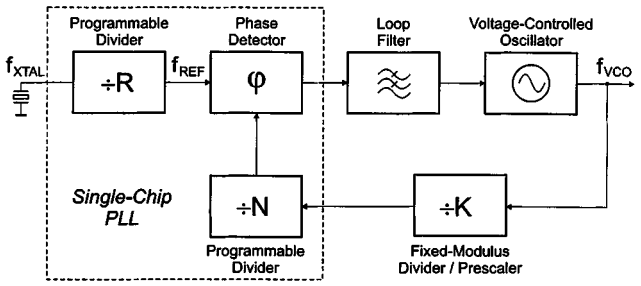

Fig. 1. Frequency-synthesizer block diagram.

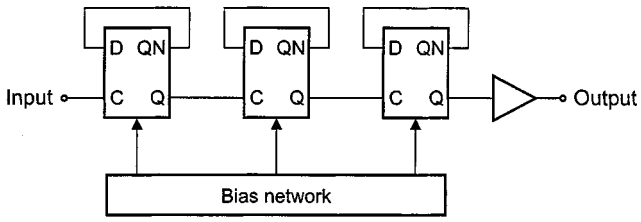

Fig. 2. Divider block diagram.

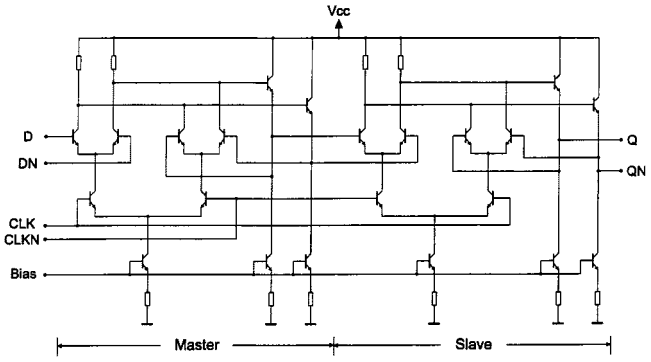

Fig. 3. Master–slave flip-flop.

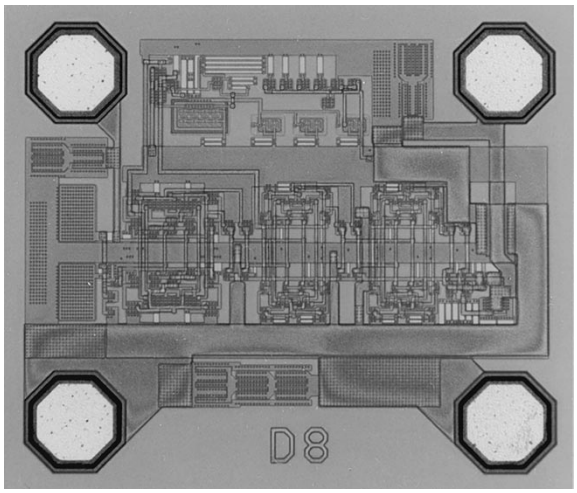

Fig. 4. Chip photograph.

The flip-flops are realized in emitter-coupled logic (ECL) using series gating between clock and data inputs (Fig . 3). This poses a lower limit on the supply voltage. Although the use of cascaded emitter followers would result in a higher speed of operation [4], only single emitter followers are used to allow operation at supply voltages down

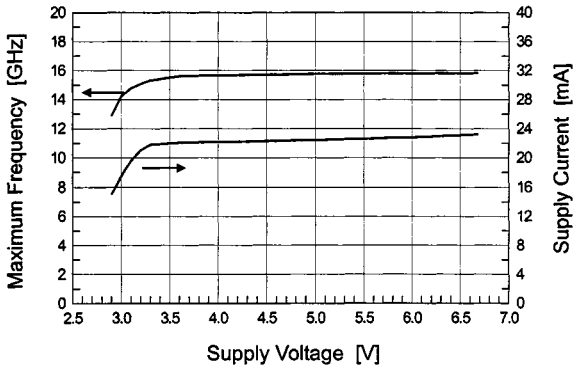

Fig. 5. Maximum operation frequency and supply current versus supply voltage.

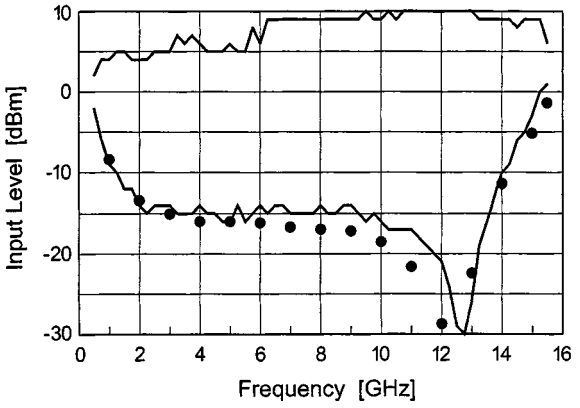

Fig. 6. Input sensitivity; solid line, top: measured maximum input level; solid line, bottom: measured minimum input level; dots: simulated minimum input level.

to 3.6 V. The use of current-mode logic (CML), which omits the emitter followers, would permit operation down to 2.7 V, but would reduce the speed of the flip-flops unacceptably.

To achieve a high operation frequency, the transistors of the first flip-flop operate at the optimum current density at which the peak cutoff frequency is found. Since the input frequencies of the second and third flip-flops are already reduced, these stages can operate at lower currents and use transistors with a smaller emitter area. Great care was taken during the simulation of the circuit to achieve the lowest possible power consumption without degrading the maximum frequency of operation.

The quiescent current of the differential pairs and emitter followers used in the flip-flops is determined by current sources. While this leads to an increased complexity of the circuits compared to the use of resistors alone, current sources are essential to keep the supply current constant when the supply voltage varies.

The entire chip uses differential signals; only the input and output are single-ended. Since no preamplifier is necessary to achieve the desired input sensitivity of the divider, the input signal can be applied directly to the clock input of the first flip-flop. The complementary clock input is decoupled by an on-chip bypassing capacitor. This capacitor has a value of 4 pF, which results in a lower cutoff frequency of 250 MHz. An output buffer converts the differential output signal of the last divider stage to a single-ended signal and is capable of driving a 50-Ω load. The output power is limited to a value sufficient for driving typical single-chip PLL's in order to keep the current consumption low.

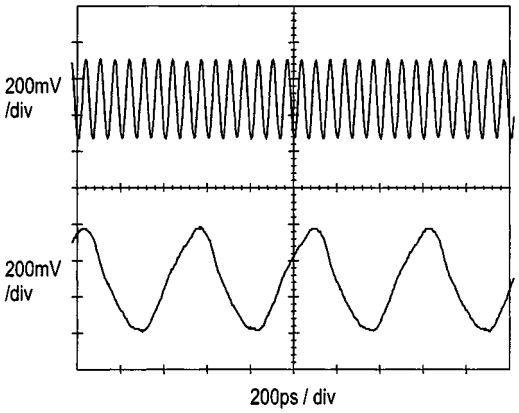

Fig. 7. Input and output waveforms at 15-GHz input frequency.

A bias network provides a reference voltage for the current sources used throughout the chip. The supply current is maintained almost constant over a wide range of supply voltages.

IV. Experimental Results

The divider chips were mounted in six-pin SOT363 packages. Measurements were performed with packaged chips soldered on microstrip test boards.

The maximum operating frequency obtained at a supply of 3.6 V/22.1 mA is 15.6 GHz. The current consumption and maximum frequency remain almost unchanged over the nominal 3.6–6-V supply range, as can be seen in Fig. 5. At room temperature, operation at 15 GHz is possible with a supply voltage as low as 3.2 V and a power consumption of only 67 mW. To evaluate the effect of the plastic package, additional measurements were performed on-wafer. The maximum input frequency measured on wafer is 16.2 GHz. The required input signal is 2 dB lower than for the packaged chips at the frequency of 15 GHz. These measurements indicate that the package has only a slight influence on the performance of the circuit.

Fig. 6 shows the input sensitivity of the frequency divider. The solid lines indicate the minimum and maximum input power for correct operation. The dots show simulation results for the minimum input power. In these simulations, bond-wire inductance and pad capacitance were included to account for the effect of the package. Simulation and measurement show good agreement.

The dynamic range of the frequency divider is 20 dB or more over a wide frequency range. The lowest operating frequency of the divider is 500 MHz. At frequencies below 2 GHz, however, higher input levels are needed. The flip-flop forming the first divider stage requires a minimum slew rate of its clock signal. When applying a low-frequency sinusoidal input signal, this slew rate has to be achieved by increasing the amplitude.

The input sensitivity reaches a maximum around 12 GHz. This is the frequency at which self-oscillation of the divider occurs in the absence of an input signal. This self-oscillation is a common phenomenon in ECL dividers and is caused by the first divider stage acting as a ring oscillator. As Fig. 2 shows, this stage consists of a D-type flip-flop with feedback from the inverted output to the input, corresponding to the feedback from the output to the input of an inverter chain in a ring oscillator. The flip-flops used in the divider are of the master–slave type. This means that, depending on the state at the clock input, either the master or slave section is transparent, while the other stage is latched. This latched condition breaks the feedback loop and, thus, prevents oscillation. In the absence of an input signal, however, the

TABLE I
TECHNICAL DATA

Supply voltage	3.6 V – 6 V
Supply current ($Vcc = 3.6\,V$)	22.1 mA
Maximum frequency ($Vcc = 3.6\,V$)	15.6 GHz
Output power ($f_{IN} = 12\,GHz$)	-7 dBm
Phase noise ($f_{offset} = 1\,kHz$)	-137 dBc/Hz
Chip size	536 x 476 μm^2
Technology	0.8 μm silicon bipolar
Package	SOT363

differential input voltage of the complementary click inputs (CLK and CLKN) of the flip-flop (Fig. 3) is zero. This corresponds to an invalid logic level between *HIGH* and *LOW*, which causes both master and slave to become transparent. The flip-flop, therefore, acts as inverter, and ring oscillator operation sets in. This behavior is also responsible for the minimum slew rate requirement mentioned above. The clock transitions have to be fast enough to prevent self-oscillation during the zero crossings.

If the divider is used as prescaler in a frequency synthesizer, this self-oscillation poses no problem since the VCO always provides an input signal. There are other applications of this divider, however, where self-oscillation is undesirable, e.g., in frequency counters. Since the oscillation is caused by an invalid logic level at the clock input of the flip-flop, it can be prevented by forcing this input into a well-defined state in the absence of a signal. This can be done by introducing an offset of approximately 40 mV between the complementary CLK and CLKN inputs of the first flip-flop. The generation of this offset could easily be included on chip into the network providing the bias for the clock input. However, this offset causes a decrease in sensitivity of the divider since the input signal has to become larger than the offset to have any effect. In our design, which does not include a preamplifier, the higher input sensitivity was preferred over the suppression of self-oscillation. In those cases where it is desired, the offset can easily be achieved by connecting one external resistor of 1.5 kΩ from the input pin of the chip to ground.

Fig. 7 shows the input and output waveforms at an input frequency of 15 GHz. The output power is –7 dBm with a 50-Ω load. This is sufficient to drive dual-modulus prescalers or single-chip PLL's following this divider in typical applications.

In a frequency synthesizer, great care is taken to keep the phase noise of the output signal to a minimum. It is important to note that not only the VCO, but also all other components inside the PLL (i.e., frequency dividers, phase detector, and loop filter) contribute to the phase noise. For this reason, it is desirable to keep the phase noise of frequency dividers as small as possible. In our design, low-current consumption was of the highest importance. This demand tends to be conflicting with low phase noise. We, therefore, measured the phase noise at the divider output to verify that the optimization for low power has not compromised the phase noise performance. A measurement setup similar to the one proposed in [6] was used. At an input frequency of 12 GHz and an offset of 1 kHz, a phase noise of –137 dBc/Hz is achieved. This is in good agreement with values reported for other ECL dividers [7] and shows that the optimization for low power has not impaired the phase noise performance of the divider.

Table I gives a summary of the technical data of the frequency divider.

V. CONCLUSION

We have designed a static frequency divider operating up to over 15 GHz. It was optimized for low-power dissipation and consumes only 22 mA with supply voltages ranging from 3.6 to 6 V. This shows that mature silicon bipolar production technologies can be used to manufacture high-speed and low-power components for frequencies well above 10 GHz. In combination with an inexpensive plastic package, this results in significant cost reduction.

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A Plastic Package GaAs MESFET 5.8-GHz Receiver Front-End with On-Chip Matching for ETC System

Eng Chuan Low, Kelvin Yan, H. Nakamura, and Hiroki I. Fujishiro

***Abstract*—A plastic package GaAs MESFET receiver front-end monolithic microwave integrated circuit operating at 5.8 GHz is presented in this paper. It has a two-stage low-noise amplifier followed by a dual-gate mixer. Operating at 3 V and 8.3 mA, a conversion gain of 20.4 dB, noise figure of 4.1 dB, and high port-to-port isolations have been achieved. Total chip size of 1.0 × 0.9 mm^2 has been achieved through on-chip matching for both RF and local-oscillator ports and the use of simple two-element matching networks for all interstage matching. The 3-dB bandwidth of conversion gain is 1 GHz.**

***Index Terms*—Cascaded LNA, dual-gate mixer, ETC system, 5.8 GHz, GaAs, on-chip matching, plastic package, receiver front-end.**

I. Introduction

Recently, the electronic toll collection system (ETC) in Japan has attracted much attention. The system operates at 5.8 GHz, a frequency that is not easy to design using discrete components. Some transmitter performance results using monolithic mircowave integrated circuits (MMIC's) have just been reported [1], [2]. Receiver front-end (RFE) performance has also been reported using an self-aligned gate (SAG) GaAs MESFET process in a ceramic package [3].

In this paper, the design and the performance of the RFE MMIC using a plastic package for the ETC system are presented.

II. Circuit Design

The MMIC reported in this paper is based on the 0.5-μm gate ion-implantation GaAs MESFET process technology with 4-μm-thick Au-plated film for spiral inductors. The key feature of this RFE MMIC is that the whole circuit has been designed and realized in a plastic package rather than the typical expensive ceramic package. This is a rather attractive cost-effective MMIC to realize. In addition to this, the small chip size (1.0 × 0.9 mm^2) drives down the overall cost even further. The achieved chip size is made possible through the use of simple two-element matching network for all the interstage matching. Also, both the RF and local oscillator (LO) ports have been matched on-chip. Based on all these considerations, the achieved conversion gain and noise figure (NF) fit well with simulation results.

To achieve good performance at 5.8 GHz by using a plastic package, accurate models are necessary and taken into consideration from the early design stage. Models have been extracted internally for the package, signal bonding wire, and ground bonding wire. The package lead and signal bonding wire have been grouped as a single entity. Model parameters are extracted by a data-fitting technique that fit the simulated S-parameter to the measured S-parameter. Fig. 1 shows the model for the package lead and signal bonding wire. The model has been developed in such a way that the loop height has been included into the model, and only the distance from the bonding tip of the package lead to the bonding pad of the designed chip need to be considered. This model has been tested and verified within the 0.1–10.1-GHz range. As for the MESFET device model, the model to simulate its behavior is the EEFET3, a model that was proposed by the Hewlett-Packard (HP) Company, Santa Rosa, CA. This model is basically an empirical model. The elements in the equivalent circuit approximate some aspects of the device physics that are expressed by some empirical formulas. The coefficients in the empirical formulas

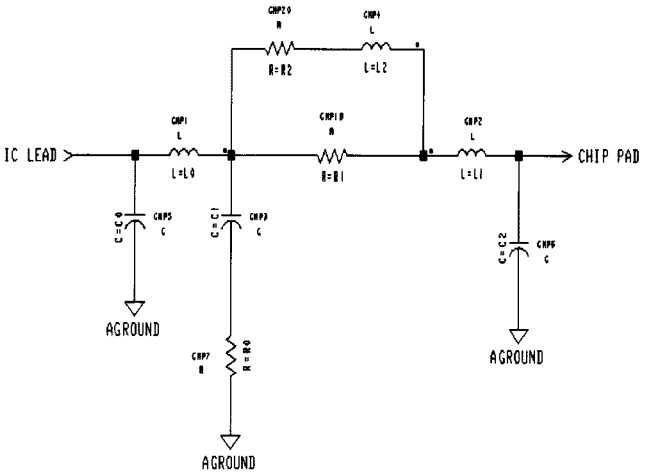

Fig. 1. Package and signal bonding wire model.

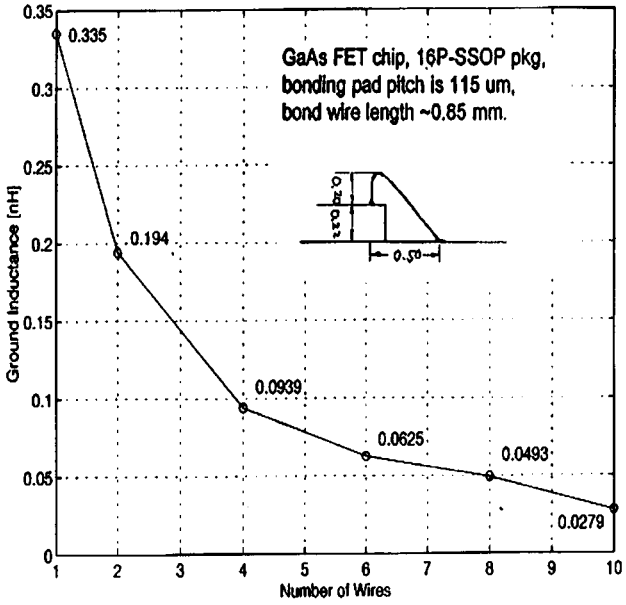

Fig. 2. Inductance versus number of common ground bonding wires.

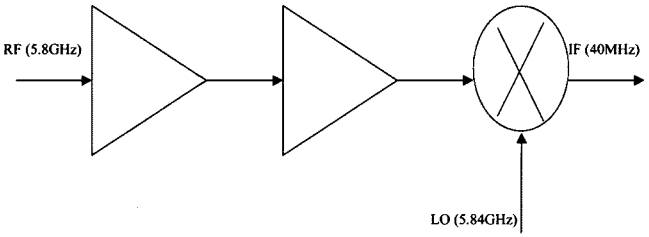

Fig. 3. Block diagram of the RFE MMIC.

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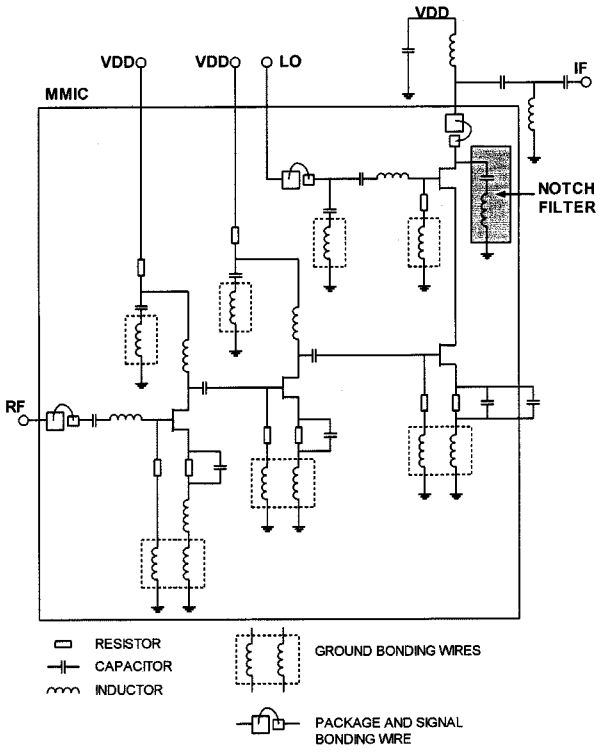

Fig. 4. Circuit schematic of the RFE MMIC.

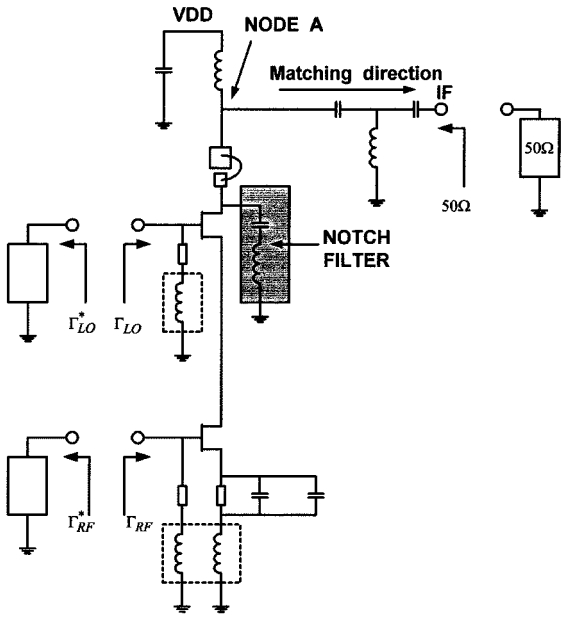

Fig. 5. IF port matching.

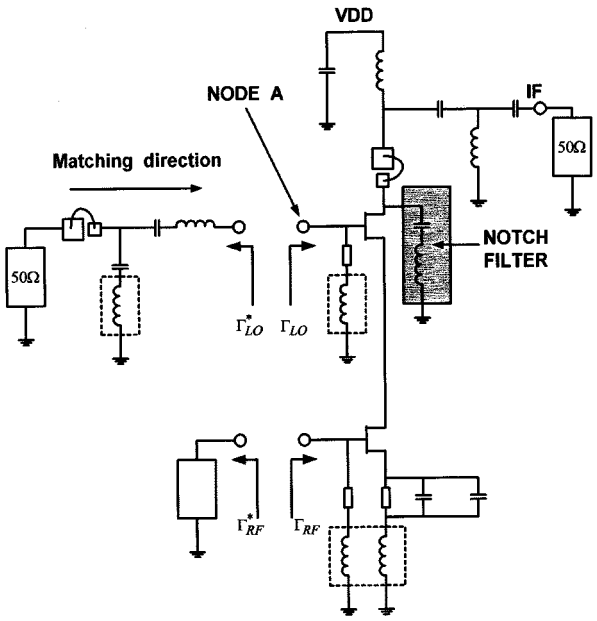

Fig. 6. LO port matching.

can be determined by data-fitting techniques through comparison of the measured and simulated dc characteristic and multibias points S-parameters. Based on the EEFET3 model, 48 model parameters are extracted for one MESFET device. These parameters describe the drain current, frequency dispersion effect, thermal effect, gate current, charge distribution, NF, and parasitic in the device.

Fig. 2 shows the inductance value of the common ground bonding wire. The inductance value approximately halved whenever the number of wires doubled. All these have been used throughout the design and have proven to be successful for a 5.8-GHz design application.

The block diagram of the MMIC RFE for the ETC system is shown in Fig. 3. This system basically consists of a cascaded two-stage low-noise amplifier (LNA) followed by an active dual-gate mixer. Each block has been designed to deliver some gain. In this design, the LO and IF frequencies are chosen to be at 5.84 GHz and 40 MHz, respectively. With such a large step in frequency conversion, image frequency rejection will be a problem without a sharp attenuation filter between the LNA and mixer. However, in the actual application environment, the image frequency band has been blocked out. Hence, the circuit has been designed without any image-rejection filter.

The complete circuit diagram of the RFE is shown in Fig. 4. The LO signal is injected into the upper FET of the dual-gate mixer. The RF signal from the cascaded LNA output is injected into the lower FET of the mixer. A notch filter that resonates at 5.8 GHz has also been integrated into the circuit at the IF output.

From the circuit-design topology, some key features are noted. Firstly, the cascaded LNA's and the dual-gate mixer together with the careful layout ensure good LO–RF isolation, sufficiently preventing the LO signal from being radiated out of the antenna. Secondly, the RF and LO power leakage into the IF port is minimized by the notch filter whose resonance frequency is 5.8 GHz. Thirdly, self-biasing is used in all stages, enabling a single voltage supply. Fourthly, to minimize the area required and, hence, the cost of the MMIC, a simple L-matching network has been employed for interstage matching. Even though this gives less degree of freedom, the results show that it is still a viable matching technique for 5.8-GHz application. Fifthly, both the RF and LO ports have been matched on-chip. The package lead and signal bonding wires are used as part of the matching elements. The technique of matching these two ports will be described later.

In the design of this MMIC, the matching design was done progressively, starting from the IF port and ending at the RF port. Compared to the conventional method of designing an LNA and mixer independently and then putting them together, this method of matching the RFE interstage removes the nonunilateral effects of the MESFET devices.

All the input ports of the MMIC are connected to 50-Ω system. The technique of matching the signal ports depends on whether the ports are matched on- or off-chip. The key idea is to include the package

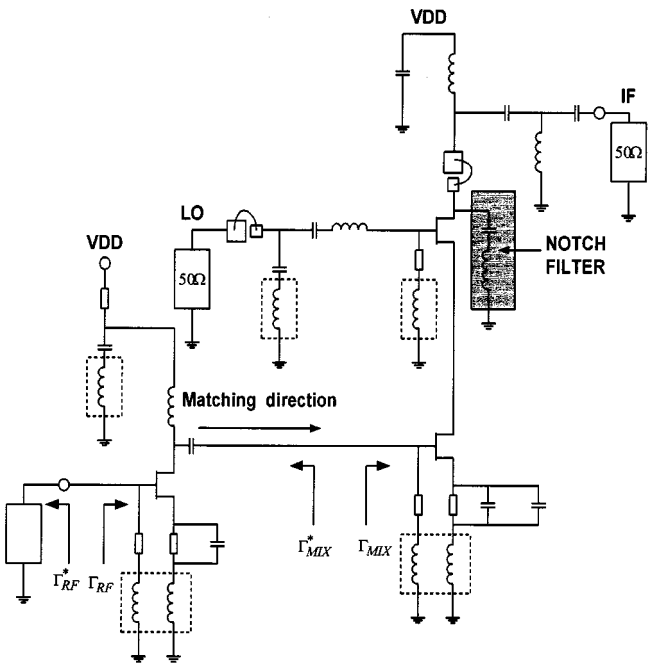

Fig. 7. Mixer interstage matching.

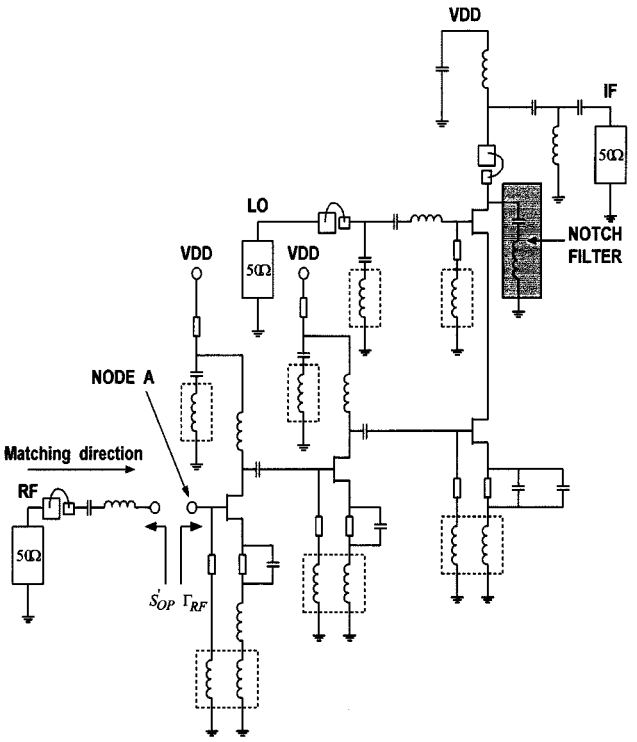

Fig. 8. RF port matching.

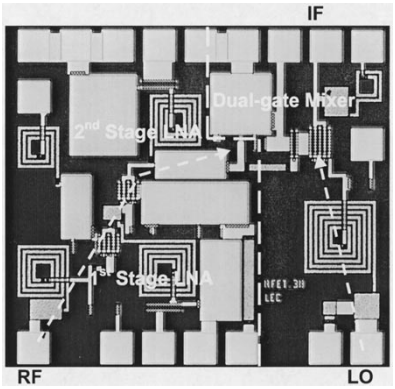

Fig. 9. Microphotograph of the RFE MMIC layout (1.0 mm × 0.9 mm).

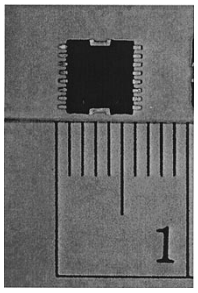

Fig. 10. Photograph of the 16-p-i-n SSOP plastic package.

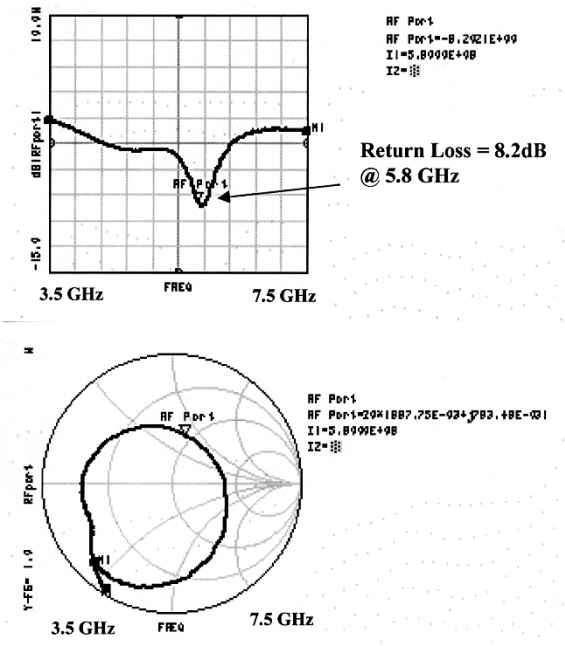

Fig. 11. Measured S-parameter of the RF port.

lead and signal bonding wire at the earliest as possible as part of the matching network.

The IF matching network is realized outside the MMIC due to the frequency at which the matching must be carried out. Fig. 5 shows the IF port matching flow and the termination of the RF and LO ports. Measured S-parameter data of the passive components have been used. Since the package lead and signal bonding wire follow immediately after the IF output, the method of matching follows the conventional way, that is to match outward toward the 50-Ω IF port starting from node A. The series capacitors are used for blocking the dc current. Since the LO and RF ports have not been matched, both ports are terminated by their respective conjugate impedance when matching the IF port.

Fig. 6 shows the LO port matching flow. In this case, the on-chip matching network is located between the package lead and the gate of the mixer MESFET. In order to include the package lead and bonding wire of the LO port as early as possible, the matching cannot be done as per the IF port. Instead, the matching starts from the input of the LO port, and moves progressively toward the gate (node A) of the

TABLE I
SUMMARY OF RFE MEASURED PERFORMANCE

No	Parameters	Unit	Test Conditions	Measured Results
1	Total Current	mA	-	8.3
2	Conversion Gain	dB	RF Pin = -30dBm LO Pin = 0 dBm	20.4
3	Noise Figure	dB	LO Pin = 0 dBm	4.1
4	LO-RF Isolation	dB	LO Pin = +2 dBm	39.3
5	LO-IF Isolation	dB	LO Pin = +2 dBm	53.6
6	RF-IF Isolation	dB	RF Pin = -30dBm	48.2
7	Input P1dB Compression	dBm	-	-31
8	RF port Return Loss	dB	-	8.2
9	LO port Return Loss	dB	-	15.8
10	IF port Return Loss	dB	-	35.8

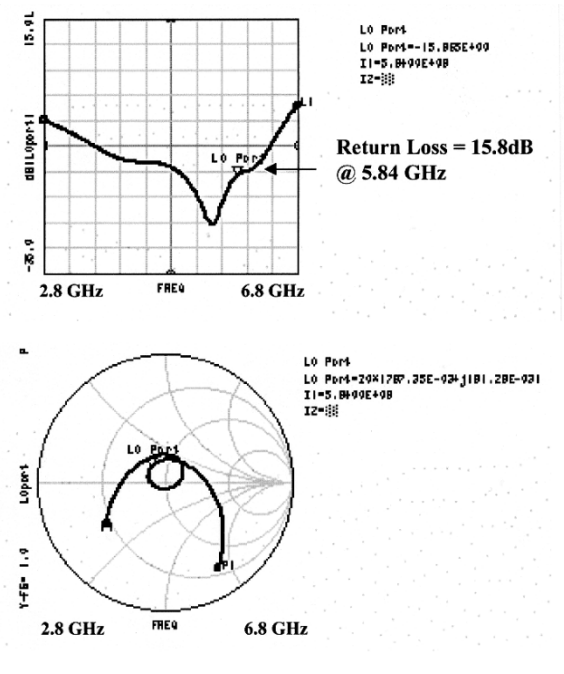

Fig. 12. Measured S-parameter of the LO port.

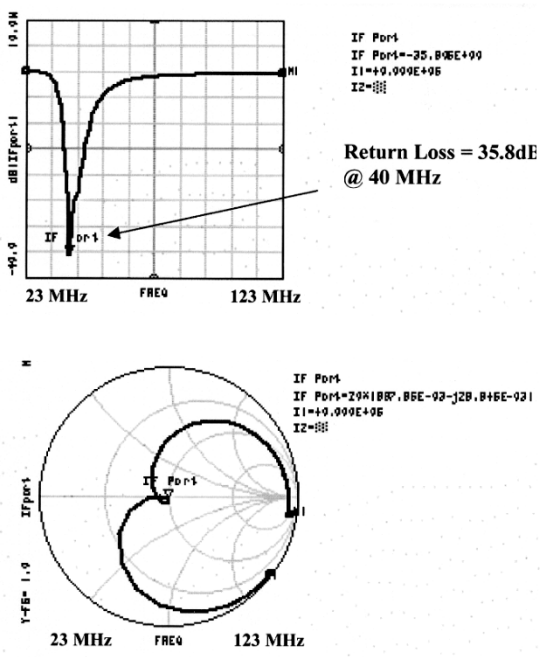

Fig. 13. Measured S-parameter of the IF port.

MESFET. To achieve maximum power transfer to the gate of the MESFET, a conjugate match at node A has been done. The matching circuit also includes a dc blocking capacitor to prevent any dc current flow from the LO input port. Again, since the RF port has not been matched, it is terminated with its conjugate impedance. The IF port is terminated with its matching circuit done earlier.

Fig. 7 shows the interstage matching for the mixer input. A simple L-network is used to conjugately match the LNA output to the input of the mixer to ensure maximum power transfer to the mixer. The RF port impedance is set to the conjugate impedance of the input impedance. The same approach is used for the interstage matching of the two-stage LNA's.

For the input to RF port case, the matching technique is similar to the LO port case. An inductor is inserted into the source of the FET for the purpose of stabilizing the FET at low frequency and bringing the NF matching closer to the gain matching point. This will improve the RF input return loss without sacrificing too much on the NF performance. As in any LNA design, a compromise is necessary between minimum noise performance and good return loss. Fig. 8 shows the matching direction of the RF port. The diagram also shows that the LNA is not

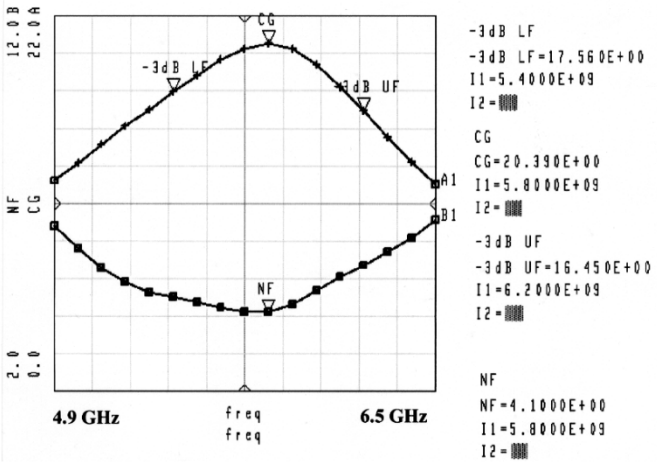

Fig. 14. Measured frequency response of conversion gain and noise figure.

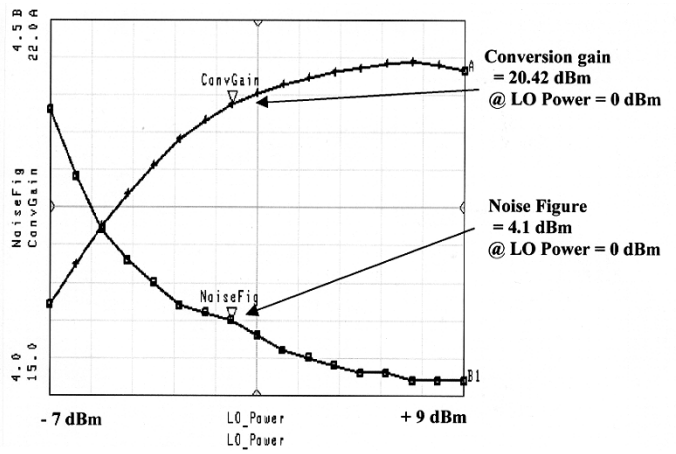

Fig. 15. Measured conversion gain and noise figure versus LO power.

conjugately matched to achieve maximum power transfer. It is matched to obtain good NF performance. Both the IF and LO ports are terminated in their respective 50 Ω preceded by their matching networks.

All common ground bonding wires have been included in the matching process above.

III. MMIC Layout

A microphotograph of the fabricated RFE MMIC chip is shown in Fig. 9. The arrowheads show the signal flow of the RF and LO signal in the MMIC. These signal paths have been layout diagonally so as to maximize the physical separation of these paths. Inductors in the RFE have been placed far apart from each other as much as possible to minimize the coupling effects and, hence, signal leakage. The inductors are realized using Metal3 layer with the center connected by Metal2. The capacitors are realized using the metal–insulator–metal (MIM) and Metal2–Gate layers. Both Metal2 and Metal3 are also used as transmission lines. The chip size (pad to pad) is 1.0×0.9 mm^2. A photograph of the RFE die as packaged into a 16-p-i-n shrinked small outline package (SSOP) plastic package with heat sink is shown in Fig. 10.

IV. Circuit Performance

All the critical performance parameters are summarized in Table I. This is the typical performance of the RFE MMIC chip. For a conversion gain of 20.4 dB, the total current of 8.3 mA is quite low for an RFE. Good LO–RF isolation is achieved by a combination of careful physical layout of the MMIC, physical separation of the RF and LO signals bonding wires, and the overall circuit topology adopted. High LO–IF and RF–IF isolations are also achieved through the implementation of the grounded series resonant circuit at the IF port.

The measured S-parameter of the RF, LO, and IF pots are shown in Figs. 11–13, respectively. The measured frequency response of the conversion gain and noise figure is shown in Fig. 14. As shown, both these parameters are optimized at the nominal frequency of 5.8 GHz. Also shown in Fig. 14, the 3-dB bandwidth of conversion gain is approximately 1 GHz. Fig. 15 shows the measured conversion gain and noise figure of the RFE as the LO power is swept from -7 to 9 dBm. The lowest achievable NF when the LO power is set at 9 dBm is approximately 4.02 dB. This shows there is not much improvement on the NF performance even when the LO power is increased to 9 dBm.

V. Conclusion

We have shown that a plastic packaged RFE can achieve good performance at 5.8 GHz in terms of conversion gain, NF, port-to-port isolations, and frequency response through early involvement in the design stage of accurate models for the package, signal bonding wire, and ground bonding wire. This is even more remarkable when it is operated from a 3-V supply with just 8.3 mA. To achieve small chip size (1.0×0.9 mm^2), simple L-networks have been used for all interstage matchings. Also, on-chip matchings have been realized for both the RF and LO ports.

Acknowledgment

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