A Simplified Broad-Band Large-Signal Nonquasi-Static Table-Based FET Model

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***Abstract*—In this paper, a simplified nonquasi-static table-based approach is developed for high-frequency broad-band large-signal field-effect-transistor modeling. As well as low-frequency dispersion, the quadratic frequency dependency of the y-parameters at high frequencies is taken into account through the use of linear delays. This model is suitable for applications related with nonlinear microwave computer-aided design and can be both easily extracted from dc and s-parameter measurements and implemented in commercially available simulation tools. Model formulation, small-signal, and large-signal validation will be described in this paper. Excellent results are obtained from dc up to the device f_T frequencies, even when f_T is as high as 100 GHz.**

***Index Terms*—FET's, modeling.**

I. Introduction

TABLE-BASED empirical nonlinear semiconductor device models [1]–[10] have been developed as an alternative approach to nonlinear analytical models. They are able to accurately reproduce the complex nonlinear behavior of semiconductor devices from measured data tables. In most cases, they can predict device operation under dc, small-signal, and large-signal excitations, and have been applied to MESFET's, MODFET's, and MISFET's fabricated from different technologies. From a practical point of view, they require an accurate and intensive experimental device characterization [11]. To decrease the measurements required, the extraction of a dense grid of measured points only where nonlinearities are stronger has been proposed [4]. An alternative is to use single-frequency s-parameter bias scans instead of the common single-bias s-parameter frequency scans [12]. In this paper, we will exploit this latter approach because it is an efficient way of extracting our model. Recently, table-based models have also been extracted from large-signal RF data, as suggested in [13], [14]. Most issues outlined in this work will still have to be taken into account when considering such an extraction.

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On the other hand, the extracted-model large-signal relations may not be integral path independent, thus making it difficult to quantify an unique RF model [15], [16]. This issue is more significant when low-frequency dispersion and nonisothermal data collection play a major role. In this study, only GaAs-based devices with relatively small low-frequency dispersion and thermal related effects were considered. In this case, it is possible to extract a viable RF model and account for these effects through the use of different current sources for dc and RF operation [4].

Empirical circuit-based models have been successfully used to predict device behavior in the microwave and millimeter-wave frequency ranges [17], [18]. For increasing the bandwidth of table-based models into the millimeter-wave range, several nonquasi-static charge approaches have been suggested [5], [7], which make use of nonlinear delay functions. In these cases, the increase in model bandwidth is achieved at the expense of an increased number of measurements along with more complex model generation and implementation procedures.

Our goal was to extend the usefulness of basic table-based models into the millimeter-wave range, without sacrificing the good reported behavior at low frequencies, and with two important requirements: simplified model extraction (reduced time) and easy implementation in available computer-aided design (CAD) tools.

II. Modeling Approach—Mathematical Description

Underlying most large-signal models is the quasi-static assumption, i.e., the large-signal model relations are considered to be only functions of their instantaneous controlling voltages [19]. Usually, table-based models assume for the intrinsic device a black-box model in which the current at each terminal is characterized by at least two large-signal functions, current and charge constitutive relations, accounting for both conductive and displacement effects [1], [3]. Displacement currents are often modeled using nonlinear charges (charge-based approaches), thus assuring both current and charge conservation in these models [20], [21].

The quasi-static assumption is a good first-order approximation in device modeling [19], but does not hold in the whole range of different device operation conditions. For instance,

due to thermal and trapping processes, the device conductive behavior is not the same under dc and RF excitations. Low-frequency dispersion modeling is often avoided in many large-signal models, but it must be included to obtain a precise model. Different table-based approaches have also incorporated this type of modeling [4], [6], [8]. Root's approach [4], for example, assumes a single-pole transition between dc and RF behavior through the use of two different drain current state functions, thus perturbing the initially assumed drain conductive quasi-static behavior. With that approach, model bandwidth (frequency range in which model predictions are valid) has been extended from microwaves down to dc. The use of quasi-static-charge large-signal relations in [1]–[4], however, restricts the upper bandwidth end of these models since they cannot predict the higher order frequency behavior of the device y-parameters, especially y_{11}, at high frequencies.

Model bandwidth can be increased with more complex intrinsic circuit topologies. In the case of linear models, an eight-element intrinsic topology [see Fig. 1(a)] is sufficient to predict high-frequency device behavior, at least up to f_T [18]. R_i in this topology accounts for quadratic frequency dependences of the small-signal y-parameters. In the case of nonlinear models, besides considering the bias dependency of these elements, e.g., g_m, $C_{\rm gs}$, etc, it is necessary to add the nonlinear diodes conductances to account for forward and breakdown behavior [see Fig. 1(b)] [17]. There are table-based approaches whose large-signal topology has explicit [10] or "implicit" [5], [7] R_i terms. Daniels's proposal [5], [22] (similar to [7]) is a charge-based approach able to model higher order frequency effects through the use of *nonquasi-static* charges. These charges are described by means of nonlinear delay functions and quasi-static charge functions at each terminal. However, model extraction and/or implementation in these cases is complex and appropriate simplifications could be desirable.

The starting point in this study is a model combining both Daniels' nonquasi-static charge definition and Root's low-frequency dispersion modeling, with the latter applied, for model completeness, to the input and output of the device. In this case, current at ith terminal can be expressed in the time domain as follows [16], [23]:

$$I_i(t) = \left[1+\tau_x\frac{d}{dt}\right]^{-1} I_i^{\rm low} + \left[1+\tau_x\frac{d}{dt}\right]^{-1} \tau_x\frac{d}{dt} I_i^{\rm high} + \frac{dQ_i^{nq}(t)}{dt}. \quad (1)$$

In (1), we are using a similar notation as in [24], in which $I_i^{\rm low}$ and $I_i^{\rm high}$ are two-dimensional functions of node voltages $V_{\rm gs}$ and $V_{\rm ds}$, $[1+\tau_x\ d/dt]$ represents a (pseudo) differential operator that is applied to the large-signal current relations, τ_x is a relaxation time modeling thermal and traps time constants, and $i = g, d$. As a consequence of this formulation, $I_i^{\rm low}$ and $I_i^{\rm high}$ are the low- and the high-pass filtered components, respectively. τ_x is related with the cutoff frequency of the filtering process and is in the kilohertz-megahertz range. In most applications, an accurate estimation of τ_x or the need for a more complex (multipole) function to model traps and thermal influence in the device frequency response is not necessary. We are interested in applications in which harmonic generation at microwaves and millimeter waves plays a major role in circuit behavior, as in the case of power amplifiers, frequency multipliers, etc, thus, this formulation along with an approximate τ_x value is all that is required.

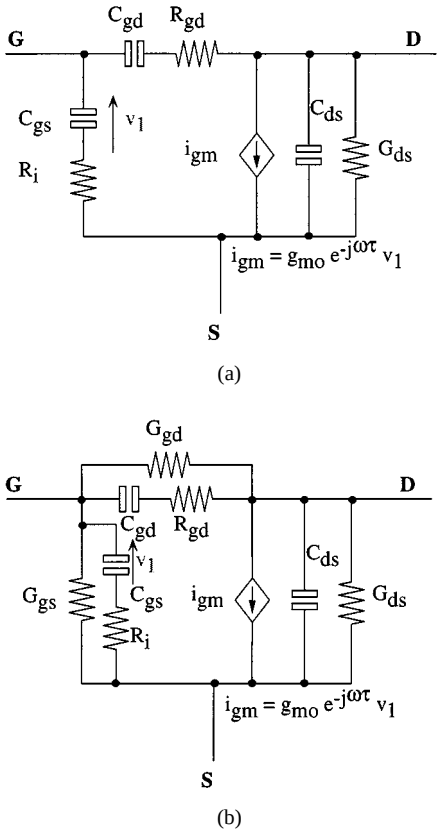


Fig. 1. Conventional intrinsic FET topologies. (a) Eight elements. (b) Ten elements. The dependent current source i_{gm} is usually controlled by the voltage drop across $C_{\rm gs}$.

The nonquasi-static charges Q_i^{nq} are expressed as [5]

$$Q_i^{nq}(t) = Q_i^q(V_{\rm gs}, V_{\rm ds}) - \tau_i(V_{\rm gs}, V_{\rm ds})\frac{dQ_i^{nq}(t)}{dt} \quad (2)$$

where Q_i^q (charge relation) and τ_i (delay relation) are quasi-static functions of nodal voltages. τ_i represents a time for redistribution of charge at ith terminal. A nonquasi-static model based on substituting (2) into (1) will be addressed as model 1.

After linearizating model 1 around a given bias point (small-signal conditions), the resulting (common source) y-parameters are [23]

$$Y_{ik} = \frac{i_i}{v_k} = g_{ik}^{\rm dc} + \frac{j\omega\tau_x}{1+j\omega\tau_x}(g_{ik}^{\rm ac} - g_{ik}^{\rm dc}) + \frac{j\omega c_{ik}}{1+j\omega\tau_i} \quad (3)$$

where

$$g_{ik}^{\rm dc} = \partial I_i^{\rm low}/\partial V_k$$
$$g_{ik}^{\rm ac} = \partial I_i^{\rm high}/\partial V_k$$
$$c_{ik} = \partial Q_i^q/\partial V_k$$
$$V_k = V_{\rm gs}, V_{\rm ds}$$

$v_k = v_{\rm gs}, v_{\rm ds}$ (small-signal voltages), i_i (small-signal currents), and $k = gs, ds$.

As an alternative, consider an approximation of (2), as suggested in [9], [16] (following partly [25])

$$Q_i^{nq}(t) \approx Q_i^q(V_{\rm gs}, V_{\rm ds}) - \tau_i(V_{\rm gs}, V_{\rm ds}) \frac{dQ_i^q(V_{\rm gs}, V_{\rm ds})}{dt}. \quad (4)$$

A nonquasi-static model based on substituting (4) into (1) will be addressed as model 2.

In this case, we obtain the following y-parameters [23]:

$$Y_{ik} = g_{ik}^{\rm dc} + \frac{j\omega\tau_x}{1+j\omega\tau_x}(g_{ik}^{\rm ac} - g_{ik}^{\rm dc}) + j\omega(1-j\omega\tau_i)c_{ik}. \quad (5)$$

These models can be applied to the extrinsic field-effect transistor (FET), but because of the reduction in useful bandwidth that would result, we will apply these models only to the intrinsic device. Fig. 2(a) shows the basic extrinsic circuit topology used in this work (completed with extra cells when required by the device). An approximate intrinsic topology corresponding to models 1 and 2 when $\omega\tau_x \gg 1$ is shown in Fig. 2(b).

Equations (3) and (5) can be analyzed in the following three different cases.

$\omega \to 0$ (dc case): in both approaches

$$Y_{ik} \approx g_{ik}^{\rm dc}. \quad (6)$$

$\omega\tau_x \gg 1$:

nonquasi-static model 1:

$$Y_{ik} \approx g_{ik}^{\rm ac} + \frac{j\omega c_{ik}}{1+j\omega\tau_i}. \quad (7)$$

nonquasi-static model 2:

$$Y_{ik} \approx g_{ik}^{\rm ac} + j\omega(1-j\omega\tau_i)c_{ik} = g_{ik}^{\rm ac} + \omega^2\tau_i c_{ik} + j\omega c_{ik}. \quad (8)$$

$\omega\tau_x \gg 1$ and $\omega\tau_i \ll 1$:

In both models

$$Y_{ik} \approx g_{ik}^{\rm ac} + j\omega c_{ik}. \quad (9)$$

Equation (9) is a quasi-static charge formulation (as in [4]) when $\omega\tau_x \gg 1$.

Equation (8) is just a truncation of (7) when $\omega^2\tau_i^2 \ll 1$. In both cases [i.e., (7) and (8)], higher order frequency dependencies can be modeled, and are good enough for predicting excellent results up to f_T.

If we compare the nonquasi-static model 2 with a quasi-static charge model [given in (9)], the only difference is just one term: the real part of the y-parameters shows a quadratic frequency dependence. That implies that both models will have approximately the same displacement currents, but they will differ in the real currents. Hence, model 2 will be able to model high-frequency quadratic dependencies of the y-parameters, as given by (8), while the quasi-static charge approach will model only linear dependencies.

In the formulation of models 1 and 2, the delay functions are also two-dimensional functions of voltage, thus requiring the processing of bias- and frequency-dependent data to extract all the nonlinear tabled functions versus voltages. As a consequence, there is a great increase in the amount of data required over quasi-static charge approaches, in which single-frequency bias dependent RF data is required. Besides model extraction, implementation is also not straightforward. For this reason, we investigated the use of linear delay functions, as a compromise between accuracy in the high-frequency regime and ease in extraction and implementation (which will also affect simulation time and memory requirements).

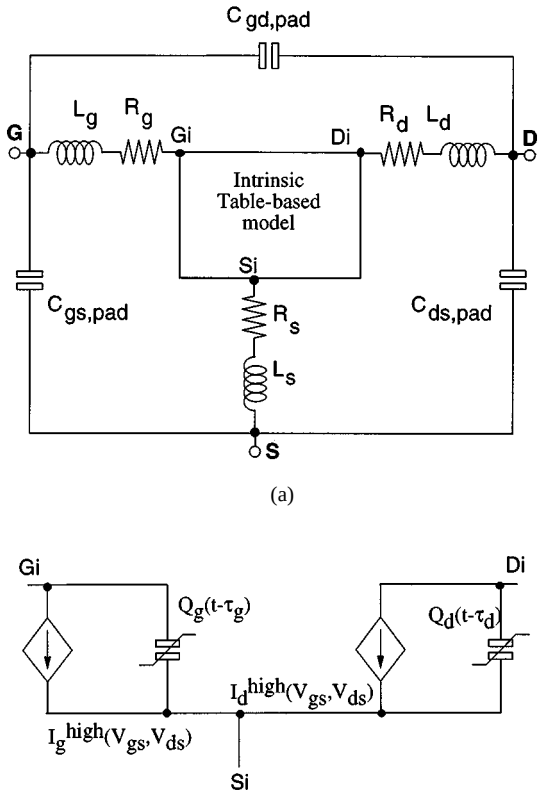


Fig. 2. (a) Model structure including a simplified parasitic network. (b) Approximate intrinsic topology when $\omega\tau_x \gg 1$.

III. Model Generation—Small-Signal Device Characterization

The extraction of a table-based model for large-signal applications requires measurements covering as much of the operational voltage range of the device as possible. For this reason, besides the linear and saturation regions of the *I–V* curves, we performed measurements in the pinchoff and forward regimes. Breakdown modeling is also very important, but unfortunately special measurements (e.g., pulsed measurements) are required to feed the model with data covering that region. An alternative we have investigated is to extend the model conductive behavior with some analytical functions (e.g., exponential behavior for soft breakdown, as in [26]) only in those regions with lack of data and when required by the application.

The extraction of the parasitic network was performed following the well-known procedure based on cold-FET measurements [27], [28]. To obtain accurate parasitic capacitances, we have measured FET's with different gatewidths to remove the

undesired intrinsic contribution to the overall extracted capacitances. Channel resistance has also been taken into account under forward bias conditions [16], [27], [28]. Once parasitics were known, parasitic cells were deembedded to get the intrinsic y-parameters (as in [29]) required to directly fit the small-signal nonlinear model equations [(7)–(9), depending on the model or the frequency range]. It was also necessary to shift the voltage reference planes to the intrinsic level [24], taking into account dc voltage drops in parasitic resistances and measurement system bias tees.

The current relations I_i^{low} were directly obtained from the measured dc *I–V*'s of the device. The high-frequency current and charge relations I_i^{high} and Q_i^q were determined from the small-signal conductances g_{ik}^{ac} and capacitances c_{ik} by a contour integration process [see (10) and (11)] [4], [5], [16], [23]. Provided that some relations are held (integrability conditions [16]), uniqueness in the model is assured.

$$\begin{aligned}\vec{\nabla} I_i^{\text{high}} &= g_{i\text{gs}}^{\text{ac}} \hat{V}_{\text{gs}} + g_{i\text{ds}}^{\text{ac}} \hat{V}_{\text{ds}} \\ \vec{\nabla} Q_i^q &= c_{i\text{gs}} \hat{V}_{\text{gs}} + c_{i\text{ds}} \hat{V}_{\text{ds}}\end{aligned} \tag{10}$$

$$\begin{aligned}I_i^{\text{high}} &= \int \vec{\nabla} I_i^{\text{high}} \cdot d\vec{V} \\ Q_i^q &= \int \vec{\nabla} Q_i^q \cdot d\vec{V}.\end{aligned} \tag{11}$$

If we consider for a moment the use of nonlinear delay functions, g_{ik}^{ac}, c_{ik}, and τ_i could be determined at each bias point by relating the right-hand side of (7) or (8) to the y-parameters extracted from measurements in the frequency range where $\omega\tau_x \gg 1$. We have performed this curve fitting using robust estimation, in order to minimize the contributions of noisy data to the generation process. Once these parameters were obtained versus bias, it is possible to generate I_i^{high} and Q_i^q through the integration process. This extraction procedure, however, requires multifrequency s-parameter measurements in a fine mesh of bias points; this is a very time-consuming process. To avoid this, a constant τ_i function is proposed [23], which allows for simplified model extraction, generation, and implementation. If τ_i is considered as a constant, we can directly extract g_{ik}^{ac} and c_{ik} from single-frequency measurements, in the range for which $\omega\tau_x \gg 1$ and $\omega\tau_i \ll 1$ hold, using (9) in both models (as in a quasi-static charge approach). These measurements can be quickly performed using single-frequency bias scans [12], [29]. In addition, for extracting an effective value for τ_i, it is only necessary to perform a reduced set of measurements over frequency at various bias points, fitting (7) or (8) (for models 1 and 2, respectively) by using robust estimation. Therefore, the use of linear delay reduces considerably the amount of measurements required.

In this case, I_i^{high} and Q_i^q are directly extracted from the y-parameters, and there is not an intermediate step to fit the intrinsic model to a conventional small-signal circuit topology, as in other large-signal models. The only fitting process required (through (7) or (8)) is to extract the constant τ_i values, and it has to be performed only at a few bias points to get an effective value.

As a first test to the validity of the linear delay assumption, Fig. 3 shows the measured bias dependence of these delays

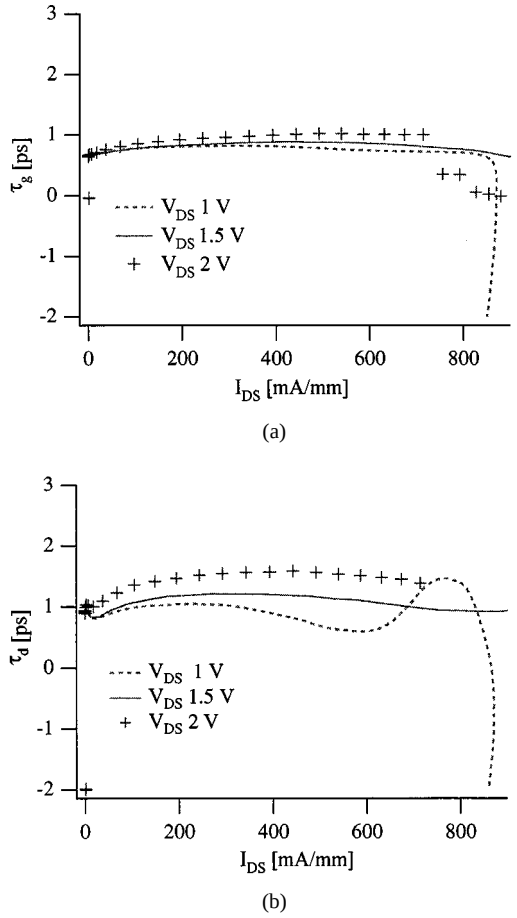


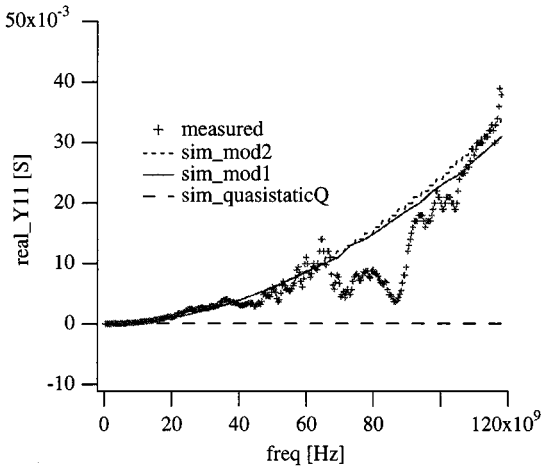
Fig. 3. Delay functions versus I_{DS} at three fixed values of V_{DS} for a 4 × 60 μm width pHEMT with a 0.15-μm gate length. (a) τ_g. (b) τ_d.

for a GaAs pseudomorphic high electron-mobility transistor (pHEMT) device. In most of the *I–V* range, the extracted delay functions are approximately constant, thus consistent with the assumption. A more exhaustive test is performed in the following section.

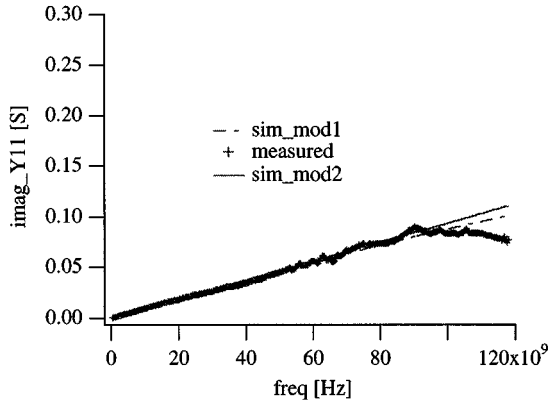
IV. Model Validation Under DC and Small Signal up to 120 GHz

The linear delay nonquasi-static models 1 and 2 have been implemented in MDS (HP-EEsof) using symbolically defined devices (SDD's). The linear delay assumption allows for a very simple implementation of both approaches. In fact, the translation of each model from the time to frequency domain is straightforward, and only simple frequency transformations are required. During simulation time, table-formatted large-signal relations are interpolated using the standard spline routines available in MDS.

Model extraction and validation have been performed using single- and double-delta-doped AlGaAs/InGaAs/GaAs pHEMT devices fabricated at the Fraunhofer Institut für Angewandte Festkörperphysik (Fraunhofer IAF), Freiburg, Germany. We have chosen devices from different wafer designs, with f_T values of approximately 30 and 100 GHz. S-parameter measurements in the 0.5–118.5-GHz range have been performed to extract the parasitics values, and for model

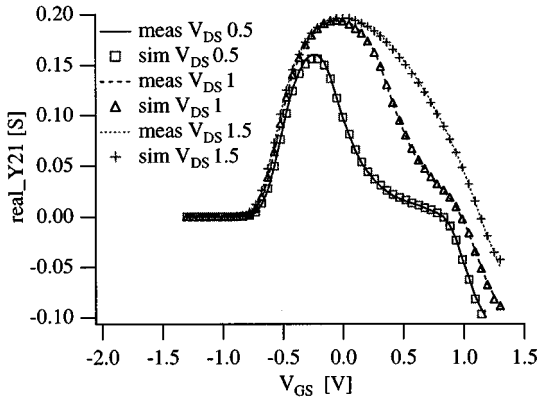


(a)

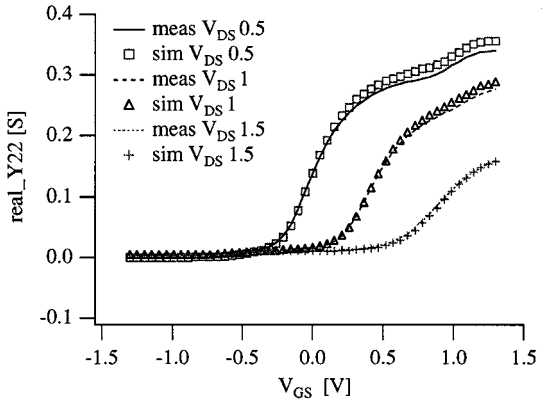


(b)

Fig. 4. Measured and simulated intrinsic Y_{11} for a $2 \times 60\ \mu$m width pHEMT with a 0.15-μm gate length. (a) Real part. (b) Imaginary part. $V_{\rm GS} = 0.3$ V, and $V_{\rm DS} = 1.5$ V.



(a)



(b)

Fig. 5. Measured and simulated y-parameters real parts for a $4 \times 60\ \mu$m width pHEMT with a 0.15-μm gate length. (a) Y_{21}. (b) Y_{22}. Frequency: 2 GHz. Note the good predicted behavior at this low frequency.

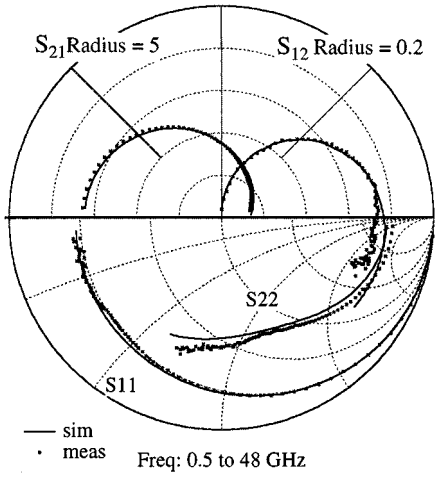
validation purposes, of the 100-GHz f_T devices, using the system described in [18]. In the case of the 30-GHz f_T devices, these measurements were performed in the range of 0.5–50 GHz. In both approaches, models 1 and 2, and for all devices, single-frequency s-parameter measurements at 2 GHz were used to extract $I_i^{\rm high}$ and Q_i^q. For extracting τ_i values, measurements were performed in the 0.5 range to approximately 40 GHz (for all devices) at several bias points. Those delays could be also used as fitting parameters and be optimized to fit the measured s-parameters.

Small-signal validation involves checking the ability of these models to predict the proper y- or s-parameters at each bias point and at those frequencies in the desired bandwidth. If we consider, for instance, the frequency dependence of the measured real part of Y_{11}, $\rm real\_Y_{11}$ [see Fig. 4(a)], an approximate quadratic behavior with the frequency can be observed. The simplified approaches proposed in this paper present a mathematical formulation which, in theory, can model such behavior. On the other hand, Fig. 4(b) shows a nearly linear behavior with frequency for the imaginary part of Y_{11}, $\rm imag\_Y_{11}$, as extracted from measured s-parameters. Assuming the use of the same delays τ_i in both nonquasi-static models, Fig. 4 also shows the intrinsic $\rm real\_Y_{11}$ and $\rm imag\_Y_{11}$ versus frequency modeled using these approaches. As can be seen, they predict the quadratic behavior observed in $\rm real\_Y_{11}$ and the linear one observed in $\rm imag\_Y_{11}$. Only small differences between both models can be observed at very high frequencies, confirming that model 2 is a valid simplification of model 1, even at these high frequencies. The behavior of a pure quasi-static charge approach extracted at 2 GHz is also shown in Fig. 4(a), confirming its erroneous prediction of the measured $\rm real\_Y_{11}$ frequency response.

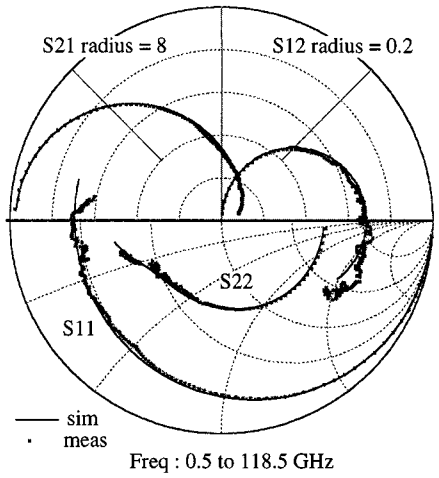
In addition, the ability of these models to predict device behavior at different bias points is clearly shown in Fig. 5, which plots the measured and simulated at 2 GHz $\rm real\_Y_{21}$ and $\rm real\_Y_{22}$ versus gate bias for different drain voltages.

These models, therefore, account for both the necessary frequency- and bias-dependent behavior required to predict the small-signal s-parameters at the different bias points.

Fig. 6(a) shows the good agreement obtained comparing measured and simulated, using model 1, s-parameters in the range of 0.5–48 GHz for a device with a f_T of 30 GHz. To demonstrate that this good agreement holds even in the case of devices suitable for applications in the millimeter-wave range, Figs. 6(b), 7, and 8 show a similar plot, but in the 0.5-118.5-GHz range for two different devices. Excellent agreement can be observed up to 118.5 GHz, being important to note that the devices f_T in this case is 100 GHz. On the other hand, using model 1 [see Fig. 7(a)] or model 2 [see Fig. 6(b)] for simulating the same de-

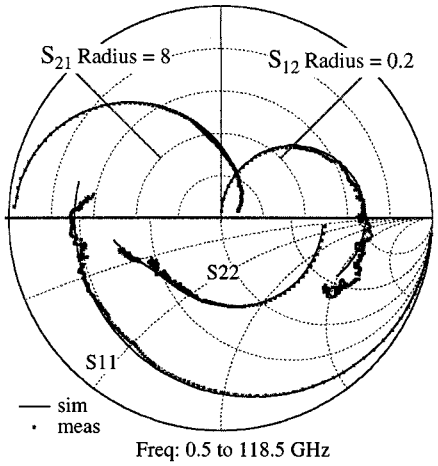


(a)

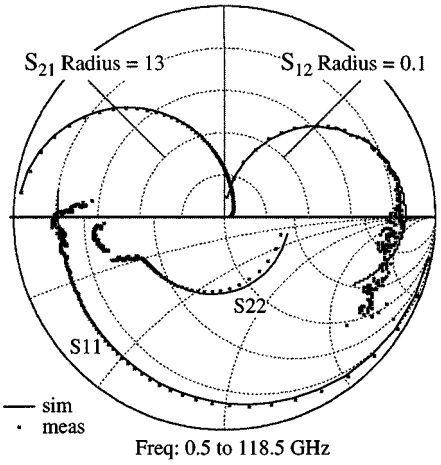


(b)

Fig. 6. Measured and simulated s-parameters. (a) For a 2×50 μm width pHEMT with a 0.6-μm gate length, $V_{\rm GS} = -0.5$ V and $V_{\rm DS} = 2$ V, simulated using model 1. (b) For a 2×60 μm width pHEMT with 0.15-μm gate length, $V_{\rm GS} = 0.3$ V and $V_{\rm DS} = 1.5$ V, simulated using model 2.



(a)



(b)

Fig. 7. Measured and simulated using model 1 s-parameters. (a) For a 2×60 μm width pHEMT with a 0.15-μm gate length, $V_{\rm GS} = 0.3$ V and $V_{\rm DS} = 1.5$ V. (b) For a 4×60 μm width pHEMT with a 0.15-μm gate length, $V_{\rm GS} = 0.0$ V and $V_{\rm DS} = 1.5$ V.

vice does not make any important difference in bandwidth, thus, from this point, it will not be addressed the specific model used in each figure, both give similar predictions. It is also important to note that these models were extracted in these cases at 2 GHz, and the bandwidth is achieved by the nonquasi-static charge formulation based on linear delays.

We have also observed that a proper selection of the integration path can enhance the accuracy over a given region of operation. We have used this knowledge to improve model behavior for special applications, like class-B amplifier operation (see Fig. 8).

V. Model Validation Under Large-Signal Conditions

Large-signal FET operation can be characterized using the conventional harmonic output power versus input power, gain, and efficiency versus input power or impedance terminations. Recently, it has also been addressed the necessity of characterizing the large-signal device dynamic behavior [30]: input and output waveforms, dynamic loadline, dynamic transfer characteristics, input dynamic trajectory, etc. With this information, we get a better knowledge of device behavior: *I–V* regions where power saturation takes place, optimum terminations for max-

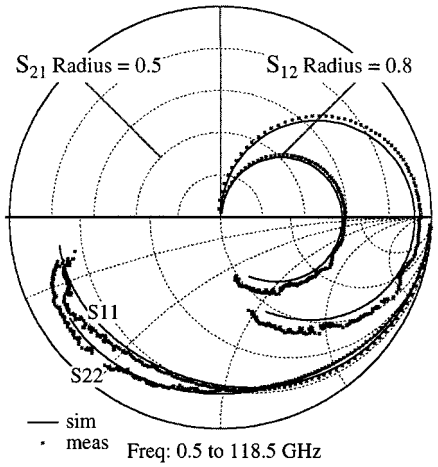


Fig. 8. Measured and simulated s-parameters for a 4×60 μm width pHEMT with a 0.15-μm gate length. $V_{\rm GS} = -1$ V and $V_{\rm DS} = 1.5$ V (class B).

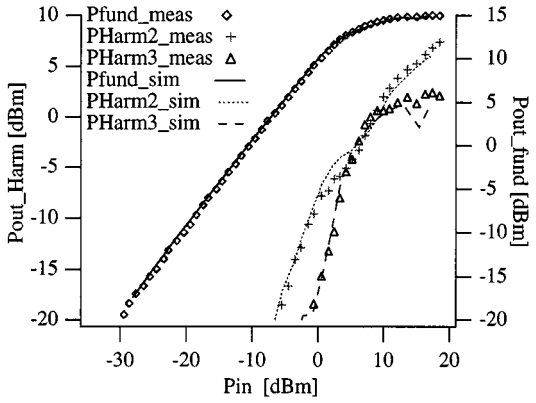


Fig. 9. Measured and simulated fundamental (16 GHz), second (32 GHz) and third (48 GHz) harmonic output power for a $4 \times 60\ \mu$m width pHEMT with a 0.15-μm gate length. $V_{\rm GS} = -0.5$ V and $V_{\rm DS} = 1.5$ V (class AB).

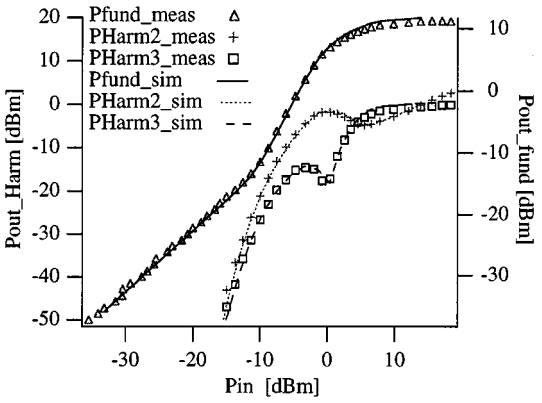
imum output power [31], etc. This characterization can be performed with the Microwave Transition Analyzer (MTA)-based systems [32]–[34].

In this study, large-signal measurements have been done using an on-wafer vector-calibrated large-signal measurement system based on the MTA [33]. Fig. 9 compares measured and simulated output power levels versus input power for the fundamental (16 GHz), second (32 GHz), and third harmonics (48 GHz, out of the system guaranteed bandwidth). Figs. 10 and 11 show similar plots for the same device, but at different fundamental frequencies and bias points. In general, excellent results have been obtained with different devices in the range of fundamental frequencies checked (from 2 to 20 GHz).

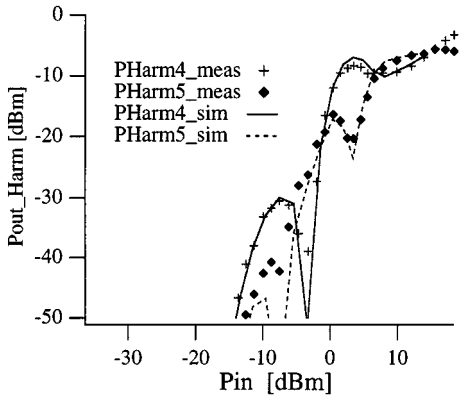
Fig. 12 shows the measured and simulated input and output dc currents versus input power in a class-B bias point and at a fundamental frequency of 8 GHz. As can be seen, the device self-biasing behavior is accurately predicted.

Fig. 13 shows a comparison between measured and simulated large-signal input and output waveforms, measured and simulated dynamic loadline and transfer characteristics at a fundamental frequency of 8 GHz (five harmonics have been used for waveform construction). Not only the RF global behavior can be perfectly predicted using both models, but also the RF dynamic behavior and the static dc bias point (due to the inclusion of the low-frequency dispersion modeling, as discussed above). It is important to note the shape of the measured loadline. Clearly, even if the measurement system is nominally a 50-Ω-load system, the load presented at the device also has reactive components. To account for this fact, we have used the information obtained from the calibration coefficients to get the actual impedance values presented at device terminals at each harmonic frequency. These values were, therefore, applied to the device terminals in the simulations under large-signal conditions [16].

It is important to note that, when comparing measurements and simulations under large-signal conditions, the effect of the uncertainties (calibration differences, bias tees resistances uncertainties, probe tips position, etc.) associated with the use of two different measurement systems, to extract and validate these models, must be considered. To get a more accurate comparison in which these uncertainties can be avoided, we have ex-



(a)



(b)

Fig. 10. Measured and simulated harmonic output power for a $4 \times 60\ \mu$m width pHEMT with 0.15-μm gate length. $V_{\rm GS} = -1$ V and $V_{\rm DS} = 1$ V (class B). (a) Fundamental (8 GHz), second and third. (b) Fourth and fifth.

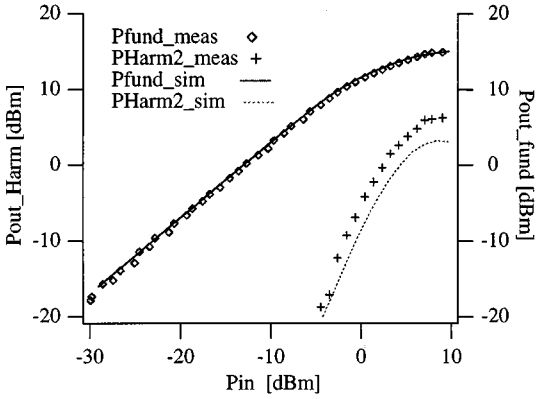


Fig. 11. Measured and simulated fundamental (20 GHz) and second harmonic (40 GHz) output power levels for a $4 \times 60\ \mu$m width pHEMT with 0.15-μm gate length. $V_{\rm GS} = 0$ V and $V_{\rm DS} = 1.5$ V (class A).

tracted and validated these modeling approaches in the same measurement system [32], [35]. Excellent results have been obtained under different load conditions and class-B device operation [32], [35].

VI. Scalability

Scaling of the nonlinear models with gatewidth is also an important issue. To achieve this, we must first be sure

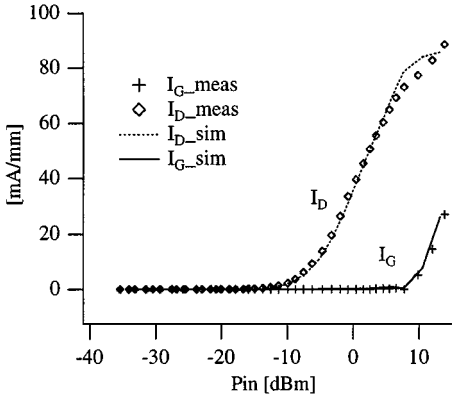


Fig. 12. Measured and simulated input and output dc currents versus input power for a 4 × 60 μm width pHEMT with 0.15-μm gate length. Fundamental frequency: 8 GHz. $V_{\rm GS} = -1$ V and $V_{\rm DS} = 1.0$ V (class B).

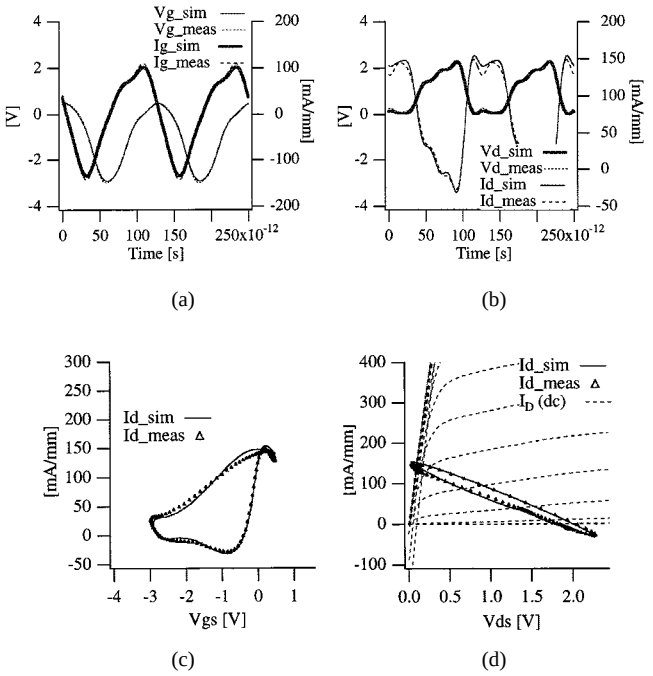


Fig. 13. Measured and simulated waveforms for a 4 × 60 μm width pHEMT with 0.15-μm gate length. (a) Input voltage and current. (b) Output voltage and current. (c) Measured and simulated dynamic transfer characteristic (I_d versus $V_{\rm gs}$). (d) Measured and simulated dynamic loadline (I_d versus $V_{\rm ds}$). $V_{\rm GS} = -1$ V and $V_{\rm DS} = 1.0$ V (class B). Fundamental frequency 8 GHz. $P_{\rm in} = 6$ dBm and $P_{\rm out}$ (fundamental) $= 10$ dBm.

that technology is experimentally scalable (e.g., comparing gatewidth-normalized dc *I–V* curves from devices having different widths), and that the proper scaling rules for device parasitics are used (e.g., check parasitics with linear models for different gatewidths). The scalability of the models developed in this work has been checked previously by the authors by comparing gatewidth-normalized current and charge large-signal relations from devices having different gatewidths [15]. Also, the ability of the scaled model to predict the small-signal s-parameters of devices with different gatewidths has been confirmed [15]. The scaling of the parasitics have been performed following first-order generally accepted scaling rules.

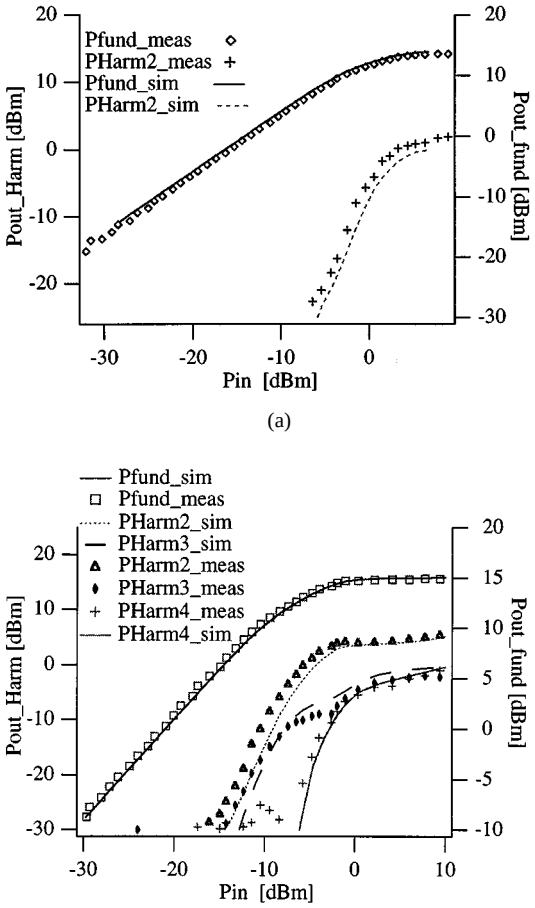


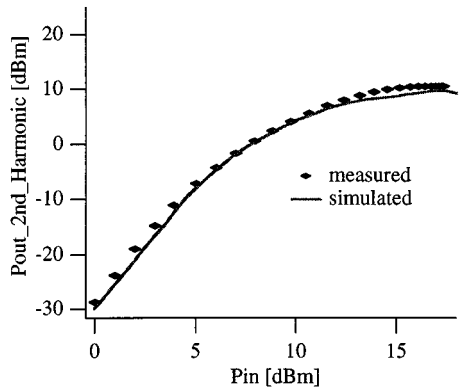
Fig. 14. Measured and simulated output power levels. Simulations performed using a simplified nonquasi-static scalable model extracted from a 4 × 60 μm width pHEMT with 0.15-μm gate length. $V_{\rm GS} = 0$ V and $V_{\rm DS} = 1.5$ V (class A). (a) 2 × 60 μm device, fundamental frequency: 20 GHz. (b) 4 × 45 μm device, fundamental frequency: 8 GHz.

In this study, we have checked the scalability of the model under large-signal conditions. For that purpose, we extracted a scalable model from a 4 × 60 μm width device (four fingers, and 60-μm unit finger width) and scaled it to different device geometries. In Fig. 14, the results of the simulations using this model scaled to 2 μm × 60 μm [see Fig. 14(a)] and 4 × 45 μm [see Fig. 14(b)] devices are compared with the measurements of such devices.

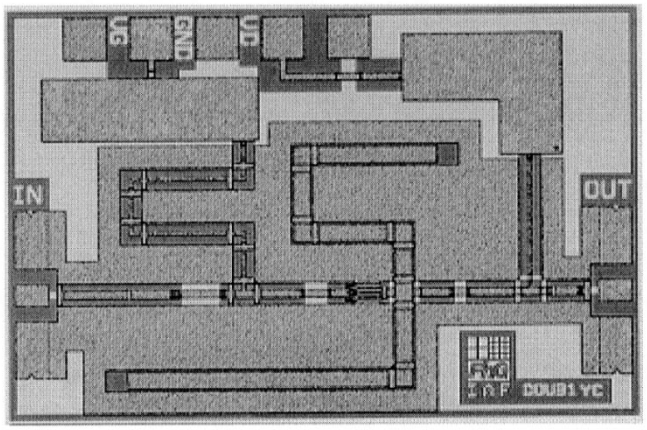
VII. Application to Monolithic-Microwave Integrated-Circuit Design

The simplified nonquasi-static models discussed in this paper have been successfully used for monolithic-microwave integrated-circuit (MMIC) designs for applications in the millimeter-wave region. As an example, different configurations (single-ended and balanced) GaAs pHEMT frequency doublers operating at 76 GHz have been designed with MDS and realized in coplanar technology demonstrating state-of-the-art performance [36].

Fig. 15(a) shows the good agreement obtained between the measured and simulated second harmonic (76 GHz) output power versus the input power (38 GHz) for a frequency doubler



(a)



(b)

Fig. 15. (a) Measured and simulated second harmonic (76 GHz) output power versus input power of a single-ended doubler. $V_{GS} = -0.8$ V and $V_{DS} = 2.2$ V. (b) Photograph of the circuit in coplanar technology (fabricated at the Fraunhofer IAF). The chip size is 1×1.5 mm^2.

operating at 76 GHz. At an input frequency of 38 GHz, the circuit achieves a maximum conversion gain of -4 dB and an output power in saturation of 10 dBm with a fundamental suppression of 17.5 dBc.

VIII. Conclusions

In this paper, we have studied different table-based FET approaches using nonquasi-static current and charge large-signal relations. In all cases, we have considered the low-frequency dispersion modeling as suggested by Root (and applied also to the device input) and proposed the use of bias scans for device characterization from dc and small-signal experimental data. We have also suggested a simplified extraction process for the nonquasi-static charge approaches through the use of linear delays, as a means to decrease characterization time and simplify model extraction, and implementation in commercially available simulators. They have been validated with pseudomorphic GaAs-based HEMT devices under dc, small-, and large-signal conditions. The simplified nonquasi-static charge approaches proposed in this paper have shown excellent results from dc up to approximately the device f_T frequencies, even when f_T is as high as 100 GHz. It has been also proven that these models can be scaled with gatewidth and successfully used in MMIC design.

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Dr. Schlechtweg was the recipient of the 1993 Fraunhofer Prize.