A Semianalytical Parameter Extraction of a SPICE BSIM3v3 for RF MOSFET's Using S-Parameters

Seonghearn Lee, *Member, IEEE,* and Hyun Kyu Yu, *Member, IEEE*

***Abstract*—In this paper, we present a new parameter-extraction method combining analytical and optimization approaches for the RF large-signal Berkeley Short-Channel IGFET Model 3, Version 3.0. Using S-parameters of MOSFET's with different channel lengths and widths at zero gate bias, all overlap capacitances are accurately determined in the high-frequency range. The junction-capacitance model parameters are extracted using S-parameters of devices with different perimeter-to-area ratios at two different biases of zero and high voltages. A robust technique utilizing simple Z-parameter equations is also used to extract resistances (R_g and R_d) and inductances. The source and substrate resistances are initially determined using the zero-bias optimization, and their uncertainties are subsequently eliminated in the normal-bias optimization. Good agreements between measured and modeled S-parameters from 0.5 to 12 GHz demonstrate the validity of this semianalytical method.**

***Index Terms*—MOSFET's, parameter extraction, scattering parameters, SPICE.**

I. Introduction

DUE TO mature and low-cost Si technologies, MOSFET's are currently recognized as promising core devices for RF/microwave circuit applications such as highly integrated communication systems [1]. For accurate circuit simulation using SPICE, the Berkeley Short-Channel IGFET Model 3, Version 3.0 (BSIM3v3) has been widely recognized as an accurate and scalable *I–V* model [2], [3], and has recently been modified to predict RF characteristics [4], [5]. Together with this development, intense research of the accurate parameter extraction of SPICE BSIM3v3 should be carried out as an essential step in RF MOSFET modeling. However, for the RF BSIM3v3, the parameter-extraction procedure suited for high frequencies has not yet been firmly established.

Generally, the sum of source and drain resistance is usually determined from dc channel conductance measurements [6], but the separate extraction remains a difficult task. The gate resistance is roughly estimated from the sheet resistance of gate material, but this estimation contains the errors due to the transmission-line effect. In particular, conventional CV measurements in the frequency range of megahertz are less sensitive to extract low capacitance values in submicrometer RF MOSFET's. In order to avoid these problems associated with dc or CV measurements without special test structures, it is beneficial to use S-parameter data measured in the high-frequency range of gigahertz. Due to this reason, the iterative optimization technique [7] using an HSPICE circuit simulator has been developed to fit a modified Level 3 SPICE model to the measured S-parameters for RF lateral diffused (LD) MOSFET. Also, a global optimization technique for the BSIM3v3 is employed for fitting S-parameters in a commercial extraction program such as Silvaco's UTMOST III [8]. However, these optimization techniques may be unable to obtain physically meaningful parameters depending on the initial value and numerical algorithm. Therefore, it is essential to reduce the number of unknown parameters to prevent the optimization from trapping into a local minimum. An efficient way to decrease parameter space dimension is to develop an independent extraction method, as in this paper, which determines model elements using S-parameter measurements separately.

Recently, direct extraction methods from measured S-parameters without the optimization have been reported for the small-signal modeling of MOSFET's [9]–[11], but its capability has been limited to small-signal parameter extraction. In addition, another extraction scheme has been introduced for a simple SPICE large-signal model with less than 20 parameters [12], but this extraction approach cannot be applied for the large-signal SPICE BSIM3v3 with much larger parameters. Thus, a new kind of BSIM3v3 extraction method should be developed for the large-signal modeling of high-frequency MOSFET's.

In this paper, a novel extraction approach utilizing S-parameter data of MOSFET's with different geometries measured at zero and normal bias values is described to obtain capacitance model parameters, resistances, and inductances of the modified RF BSIM3v3 without CV measurements. In this approach, SPICE model parameters are independently extracted from a semianalytical procedure combining analytical and optimization techniques.

II. Parameter Extraction

A novel extraction technique is applied to determine BSIM3v3 parameters of N-MOSFET's fabricated on p-type 2-k$\Omega \cdot$ cm high-resistivity (100) Si wafers using a standard twin-well CMOS process [13]. S-parameters are measured in the common source-bulk configuration using "on-wafer" RF probes and an HP8510B Network Analyzer, and probe pad parasitics are subsequently eliminated from these measured data using an open-pad pattern without a MOSFET [9].

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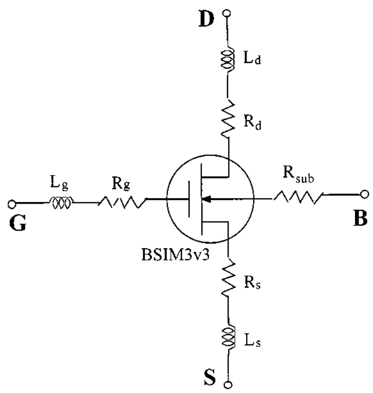

Fig. 1. Modified BSIM3v3 model ($\mathrm{RDSW} = 0$) used for an RF Si MOSFET.

Fig. 1 shows a modified MOSFET RF model suited for high-frequency circuit applications, where additional parasitic elements are added to an original BSIM3v3 model. In this model, the lumped substrate resistance (R_{sub}) that affects both drain and source junctions is included for considering the high-frequency distributed bulk effect. This bulk model with only one element of R_{sub} has already been proven to be accurate in the high-frequency region [14], [15], and is much simpler for parameter extraction than a complicated network of four bulk resistances [5]. The lumped gate resistance (R_{g}) accounting for the transmission-line effect of gate material is also added [5], [7]. In order to consider the asymmetry between drain and source resistances, the width coefficient of parasitic resistance (RDSW) is set as zero and discrete elements (R_{d} and R_{s}) are then included [4], [5]. In this high-frequency model, the parasitic inductances (L_{g}, L_{d}, and L_{s}) associated with their finger and interconnection lines are additionally inserted [9]–[11].

MOSFET model parameters in the BSIM3v3 are divided into dc parameters for modeling dc characteristics and ac parameters for ac and transient analysis. First, the dc parameters are determined by utilizing a conventional extraction routine installed in UTMOST III [8]. These extracted dc parameters are held constant during the subsequent ac extraction combining analytical equations and the HSPICE optimization.

A. Extraction of Resistances and Inductances

The accurate values of parasitic resistances and inductances in the high-frequency range are obtained by finding constant terms through the simple curve fitting of the following analytical equations [9]–[11] at normal bias over the wide range of frequency:

$$\mathrm{Re}(Z_{22} - Z_{12}) = R_{\mathrm{d}} + \frac{Ad}{\omega^2 + B} \tag{1}$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = R_{\mathrm{g}} + \frac{Ag}{\omega^2 + B} \tag{2}$$

$$\frac{1}{\omega}\mathrm{Im}(Z_{12}) = L_{\mathrm{s}} - \frac{Es}{\omega^2 + B} \tag{3}$$

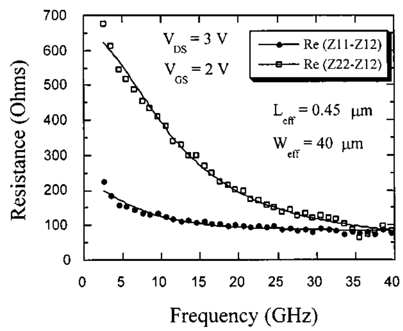

Fig. 2. Measured data (symbols) and fitted curves (lines) versus frequency for (1) and (2). The fitted values are R_{d} of 35 and R_{g} of 80 Ω.

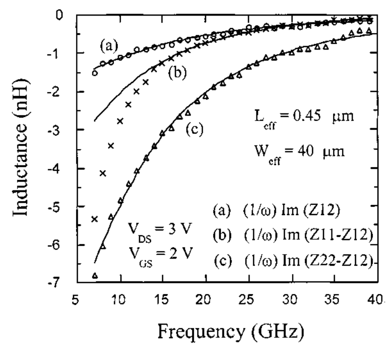

Fig. 3. Measured data (symbols) and fitted curves (lines) versus frequency for (3)–(5). The fitted values are L_{s} of 53 pH, L_{d} of 204 pH, and L_{g} of 205 pH.

$$\frac{1}{\omega}\,\mathrm{Im}(Z_{22} - Z_{12}) = L_{\mathrm{d}} - \frac{Ed}{\omega^2 + B} \tag{4}$$

$$\frac{1}{\omega}\,\mathrm{Im}(Z_{11} - Z_{12}) = L_{\mathrm{g}} - \frac{E_{\mathrm{g}}}{\omega^2 + B} - \frac{Fg}{\omega^2(\omega^2 + B)} \tag{5}$$

where B, A_{d}, A_{g}, E_{s}, E_{d}, E_{g}, and F_{g} are constant values at fixed bias.

The cold-field-effect-transistor (FET) method utilizing measured S-parameters of devices with forward-biased gate at $V_{\mathrm{DS}} = 0$ has been widely used to extract inductances and resistances for GaAs MESFET's and high electron-mobility transistors (HEMT's) [16]. However, this cold-FET method is not applicable to extract these parasitics of Si MOSFET's because dc gate current cannot flow into the rest of the device. To overcome this serious problem, the Z-parameter-extraction method using (1)–(5) was used to apply for MOSFET's, and is superior to the zero-bias method [17] for extracting resistances of the MOSFET because there are no extra measurements.

Figs. 2 and 3 show measured data and fitted curves of (1)–(5) as a function of frequencies up to 40 GHz. From these curves, R_{g} of 80 Ω, R_{d} of 35 Ω, L_{s} of 53 pH, L_{d} of 204 pH, and L_{g} of 205 pH are extracted. Excellent correlation between measured and fitted curves in the wide range of frequency is observed. The gate inductance is extracted from measured data in the higher frequency region where the third term in (5) can be neglected.

B. Extraction of Overlap Capacitances

At zero gate bias ($V_{\mathrm{GS}} = 0$), overlap capacitances (C_{GBO} between gate and bulk, C_{GSO} between gate and source, and

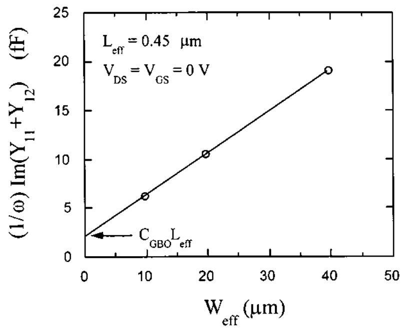

Fig. 4. Measured gate capacitance of (6) at the zero bias as a function of the total effective channel width for three devices ($L_{\rm eff} = 0.45$ μm). From y-intercepts, $C_{\rm GBO}$ is obtained to be 4.7 × 10^{-9} F/m.

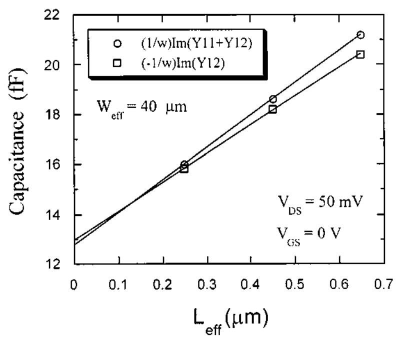

Fig. 5. The measured gate capacitances of (7) and (8) at the zero bias as a function of effective channel length for three devices ($W_{\rm eff} = 40$ μm). From y-intercepts, $C_{\rm GSO}$ and $C_{\rm GDO}$ are obtained to be 3.22 × 10^{-10} and 3.28 × 10^{-10} F/m, respectively.

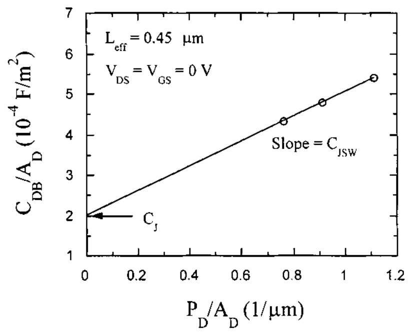

Fig. 6. Extracted values of $C_{\rm DB}/A_{\rm D}$ at the zero bias as a function of $P_{\rm D}/A_{\rm D}$ for three different devices ($L_{\rm eff} = 0.45$ μm). The extracted values are $C_J = 2.0 \times 10^{-4}$ F/m^2 and $C_{\rm JSW} = 3.05 \times 10^{-10}$ F/m.

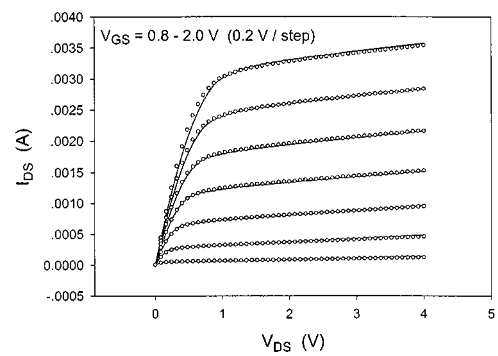

Fig. 7. Measured (symbols) and modeled (lines) $I_{\rm DS} - V_{\rm DS}$ curves for a MOSFET ($L_{\rm eff} = 0.45$ μm, $W_{\rm eff} = 40$ μm).

$C_{\rm GDO}$ between gate and drain) are obtained with higher accuracy owing to the absence of channel capacitance. This zero-bias method is similar to the previous cold FET method [16] and was newly developed to extract accurate overlap capacitances for a MOSFET using S-parameter data in the high-frequency range. This novel method may eliminate the need for large-size test structures that are required to determine overlap capacitances using the conventional CV measurement. Since resistances and inductances in the BSIM3v3 model can be omitted at lower frequencies, gate capacitances measured at zero bias are formulated by Y-parameter equations

$$C_{\rm GBO}L_{\rm eff} + C_{gb}W_{\rm eff} = \frac{1}{\omega}\,{\rm Im}(Y_{11} + Y_{12}) \tag{6}$$

$$C_{\rm GSO}W_{\rm eff} + C_{\rm gbs}L_{\rm eff} = \frac{1}{\omega}{\rm Im}(Y_{11} + Y_{12}) \tag{7}$$

$$C_{GDO}W_{\rm eff} + C_{\rm gbd}L_{\rm eff} = -\frac{1}{\omega}{\rm Im}(Y_{12}) \tag{8}$$

where $C_{\rm gb}$ is the zero-bias gate-to-bulk capacitance per unit width, and $C_{\rm gbs}$ and $C_{\rm gbd}$ are the source and drain portion of zero-bias gate-to-bulk capacitance per unit length, respectively. In Fig. 4, $C_{\rm GBO}$ is extracted to be 4.7 × 10^{-9} F/m by plotting (6) as a function of the effective channel width ($W_{\rm eff}$) and finding the y-intercept for a linear fit. To extract $C_{\rm GSO}$ and $C_{\rm GDO}$, measured values of (7) and (8) at $V_{\rm GS} = 0$ are plotted with varying the effective channel length ($L_{\rm eff}$) in Fig. 5. $C_{\rm GSO}$ and $C_{\rm GDO}$ are obtained to be 3.22 × 10^{-10} and 3.28× 10^{-10} F/m, respectively by finding y-intercepts of these linear fitted lines.

C. Extraction of Junction Capacitances

Generally, model parameters of area/sidewall junction capacitances are determined by fitting CV data for large area and long perimeter test structures, but inconsistency of test patterns from real devices may generate the extraction error . To eliminate this error, several real devices with different perimeter-to-area ratio ($P_{\rm D}/A_{\rm D}$) are used instead of extra test patterns. S-parameter data at zero bias ($V_{\rm GS} = V_{\rm DS} = 0$) are used to determine zero-bias area/sidewall junction capacitances (C_J and $C_{\rm JSW}$) at the source/drain junction. After measuring the drain–bulk capacitance ($C_{\rm DB}$) at zero bias of three devices with different $P_{\rm D}/A_{\rm D}$, the separate extraction of C_J and $C_{\rm JSW}$ is performed by plotting $C_{\rm DB}/A_{\rm D}$ versus $P_{\rm D}/A_{\rm D}$ in Fig. 6.

From the y-intercept and slope of this line, C_J of 2.01 × 10^{-4} F/m^2 and $C_{\rm JSW}$ of 3.05 × 10^{-10} F/m are determined, respectively. However, the direct extraction of $C_{\rm DB}$ is very difficult to be performed due to the complexity of the drain-to-bulk network. Therefore, for Fig. 6, $C_{\rm DB}$ values at zero bias are extracted by optimizing the RF BSIM3v3 model to fit measured S-parameters at zero bias for different $P_{\rm D}/A_{\rm D}$ devices using the optimization routine in HSPICE circuit simulator. In this zero-bias optimization, $R_{\rm sub}$ and $R_{\rm s}$ are determined, but the extracted values are obtained more accurately in the next normal-bias optimization.

Junction built-in potential parameters ($P_{\rm B} = P_{\rm BSW} = 0.98$) are calculated using the substrate doping. Under normal

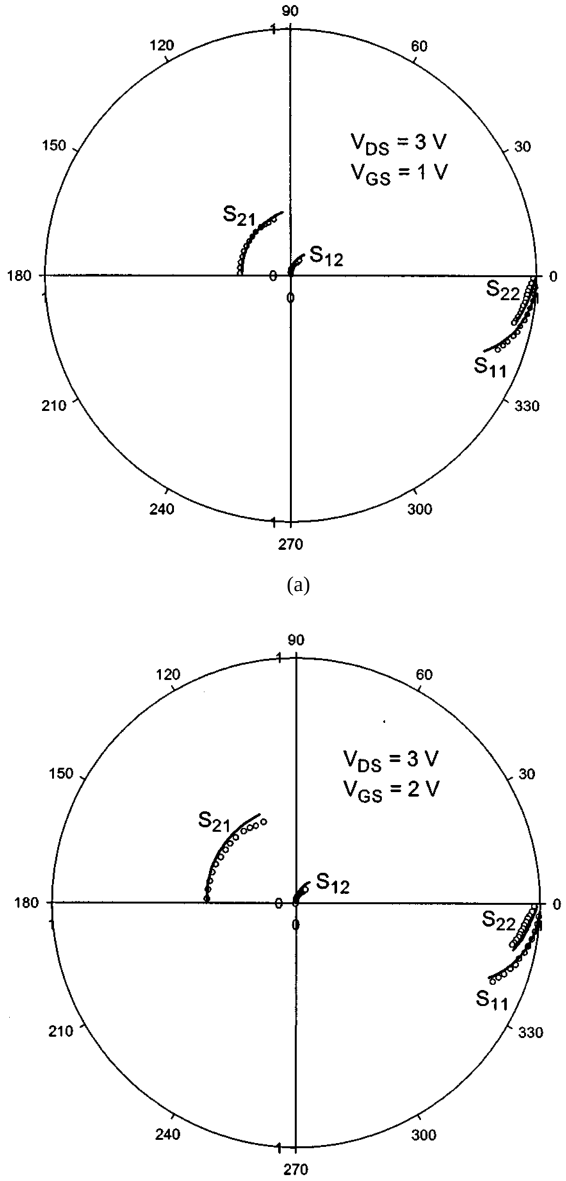

Fig. 8. Polar charts of measured (circles) and modeled (lines) S-parameters from 0.5 to 12 GHz for a MOSFET ($L_{\mathrm{eff}} = 0.45\ \mu$m, $W_{\mathrm{eff}} = 40\ \mu$m) at two different bias points.

bias condition, drain–bulk capacitance is expressed as $C_{\mathrm{DB}} = C_J(1 + V_{\mathrm{DB}}/P_{\mathrm{B}})^{-MJ}A_{\mathrm{D}} + C_{\mathrm{JSW}}(1 + V_{\mathrm{DB}}/P_{\mathrm{BSW}})^{-MJSW}P_{\mathrm{D}}$. After obtaining C_{DB} from the S-parameter optimization of MOSFET's at high drain voltage, grading coefficients ($M_J = 0.46$ and $M_{\mathrm{JSW}} = 0.48$) are determined separately by substituting the previously extracted values of C_J, P_{B}, C_{JSW}, and P_{JSW} into the y-intercept and slope of the extrapolated line for $C_{\mathrm{DB}}/A_{\mathrm{D}}$ versus $P_{\mathrm{D}}/A_{\mathrm{D}}$.

D. Optimization and Verification

Since R_{s} has a greater impact on S-parameters under normal biasing, further optimization is then performed to refine the result of R_{s} extracted at zero bias. At a normal bias point of $V_{\mathrm{GS}} = 2$ V and $V_{\mathrm{DS}} = 3$ V, the BSIM3v3 RF model was next optimized to obtain the closest possible fit to measured

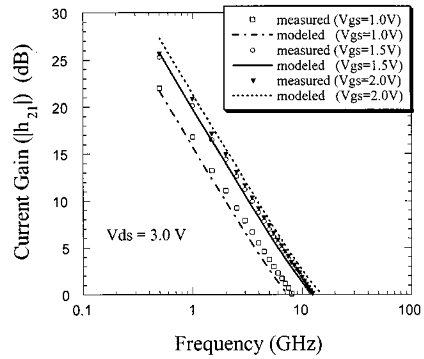

Fig. 9. Frequency response curves of measured (symbols) and modeled (lines) current gain $|h_{21}|$ for a MOSFET ($L_{\mathrm{eff}} = 0.45\ \mu$m, $W_{\mathrm{eff}} = 40\ \mu$m) at different gate voltages.

S-parameters under small error tolerances, while all parameters, except for R_{sub} and R_{s}, are fixed at previously extracted values. The values of R_{sub} and R_{s} obtained from the zero-bias optimization are also used as initial guesses, and allowed to vary within narrow bounds during this optimization. These initial guesses facilitate rapid convergence to a global minimum ($R_{\mathrm{sub}} = 1.1$ kΩ and $R_{\mathrm{s}} = 40\ \Omega$), while maintaining physically acceptable values. The agreement between measured and modeled $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ curves for a MOSFET with $L_{\mathrm{eff}} = 0.45\ \mu$m and $W_{\mathrm{eff}} = 40\ \mu$m is excellent, as shown in Fig. 7. Fig. 8 shows good correspondence between the measured and modeled S-parameters of a MOSFET at different bias points of $V_{\mathrm{GS}} = 1$ and 2 V in the frequency range of 0.5–12 GHz. This good correspondence verifies that our novel parameter —extraction technique is accurate and reliable. After S-parameters are converted to H-parameters, modeled curves of current gain $|h_{21}|$ versus frequency are compared with the measured ones under different bias conditions in Fig. 9, and show close agreement. The cutoff frequency (f_T) is extracted by extrapolating the frequency response data of $|h_{21}|$ (in decibels) over the wide frequency range. As shown in Fig. 9, the errors between measured and modeled f_T are relatively small over a wide bias range.

III. Conclusions

A novel and efficient parameter-extraction method combining analytical and optimization techniques was developed to apply for the modified RF large-signal BSIM3v3 suited for high frequencies. In this new approach, CV data measured at megahertz are not required. S-parameter data of MOSFET's with various channel lengths and widths at zero gate bias are used to determine all overlap gate capacitances. The area and perimeter parameters of junction capacitance model are separately extracted by measuring S-parameters for devices with various perimeter-to-area (P/A) ratio at zero and high voltages. The parasitic gate and drain resistances as well as inductances are accurately obtained by the simple curve fitting of Z-parameter equations. After these extractions, R_{sub} and R_{s} are finally determined by optimizing the BSIM3v3 model to fit measured S-parameter sets. Excellent agreement is observed between measured and modeled S-parameters from 0.5 to 12 GHz over the wide range of bias points, demonstrating the validity of this semianalytical method.

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