Reduction of Common-Source Inductance in FET/HEMT Structures Utilizing Wave-Propagation Effects

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***Abstract*—In this paper, a novel high-frequency/high-power field-effect-transistor structure is presented to reduce gain degradation caused by common-source inductance. In this structure, the reduction in common-source inductance is achieved without the need for using very thin substrates or very complicated fabrication technology, such as vias under each source finger. Using detailed transmission-line modeling, it is shown that a significant reduction in common-source inductance and improvement in RF performance can be achieved even for moderately high values of source grounding via inductance. The new structure allows simpler fabrication technology and is expected to be particularly useful to reduce the cost and improve the performance of high-power microwave and millimeter-wave devices and circuits.**

***Index Terms*—Distributed, inductance, MESFET, modeling, pHEMT, source.**

I. Introduction

IT IS WELL known that in order to improve the power gain of field-effect transistors (FET's)/high electron-mobility transistors (HEMT's) at microwave and millimeter-wave frequencies, it is necessary not only to improve the intrinsic device characteristics, but also to reduce parasitic elements. The source inductance L_s is a particularly important parasitic element and its effect on high-frequency gain (in common-source operation) is well approximated [1] by (1), shown at the bottom of the following page, where the various symbols have their usual meanings.

It is clear from the above equation that the effect of L_s is particularly serious in modern submicrometer devices with very high f_t values, and also in high-power large-periphery FET's, where the intrinsic device resistance's R_g, R_s, and R_i become very small, thus necessitating a proportionate reduction in L_s to maintain gain. The most effective techniques developed thus far to reduce source inductance include reducing the chip thickness to very small values and using via holes in combination with plated heat sink (PHS) techniques [2], flip-chip bonding [3], and by formation of via holes [4] under each source finger in a very thin wafer. While these techniques have enabled the development of very high-performance devices, they all suffer from the common drawback of requiring a very complicated fabrication technology, which reduces process yield and increases manufacturing costs. It is, therefore, important to develop alternative procedures to reduce the effect of common-source inductance. The purpose of this paper is to show that, with a simple modification of a widely used device structure, the effect of source inductance can be reduced to very small values. A distributed model of the FET is used to compare the source inductance effects in the different structures.

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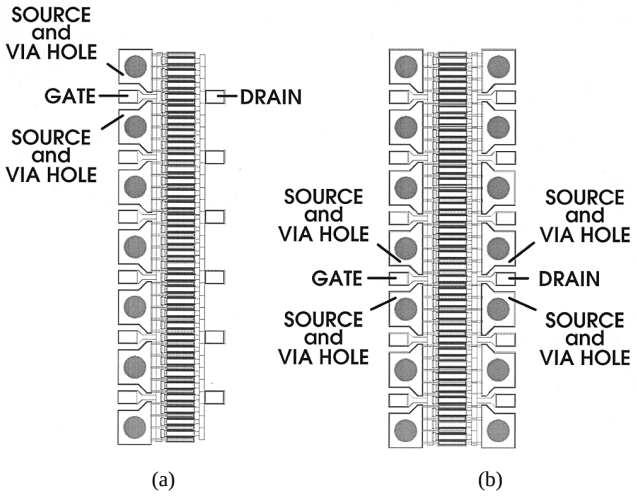

Fig. 1. Layout of: (a) conventional FET with source via at gate end of device and (b) proposed device with vias at both ends.

II. Device Structure

The device structures analyzed in this paper are shown in Fig. 1(a) and (b). The structure in Fig. 1(a) is the conventional FET structure widely used in high-power devices. In this structure, the source fingers are connected to pads on the side by either using air bridges or dielectric crossovers, and via holes in the source pads are used for grounding.

The new structure proposed in this paper is shown in Fig. 1(b). It is very similar to the conventional structure in Fig. 1(a), with the exception that the source fingers are connected to pads on both sides and vias are provided on both sides. At first it might appear that this structure might reduce the source inductance by just a factor of two due to the availability of two parallel paths to ground. However, using a distributed FET model, it will be shown in this paper that in properly designed structures, the common-source inductance will be reduced to negligible values.

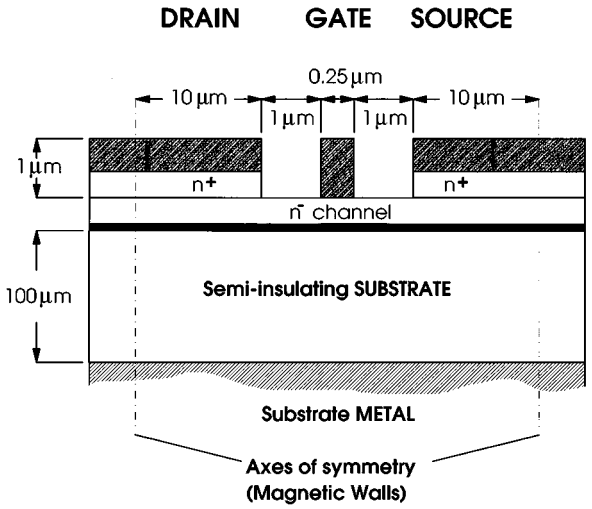

Fig. 2. Cross-sectional view of the FET structure.

TABLE I
DISTRIBUTED EQUIVALENT-CIRCUIT PARAMETER VALUES OF ONE GATE FINGER IN A MULTIFINGER DEVICE FOR DIFFERENT SUBSTRATE THICKNESSES h

	h=50μm	h=100μm	h=150μm
L_d, L_s	29.3 nH/cm	57.5 nH/cm	85.7 nH/cm
L_g	31.0 nH/cm	59.2 nH/cm	87.4 nH/cm
M_{gd}, M_{gs}	27.9 nH/cm	56.1 nH/cm	84.3 nH/cm
M_{ds}	26.9 nH/cm	55.1 nH/cm	83.3 nH/cm
C_{gd}	1.5 pF/cm	1.5 pF/cm	1.5 pF/cm
C_{gs}	1.0 pF/cm	1.0 pF/cm	1.0 pF/cm
C_{ds}	2.0 pF/cm	2.0 pF/cm	2.0 pF/cm
C_{s0}, C_{d0}	0.237 pF/cm	0.118 pF/cm	0.0788 pF/cm
C_{g0}	0.0282pF/cm	0.0141pF/cm	0.00938pF/cm
L_{id}, L_{is}, L_{ig}	0	0	0
R_{id}, R_{is}	50 Ω/cm	50 Ω/cm	50 Ω/cm
R_{ig}	1200 Ω/cm	1200 Ω/cm	1200 Ω/cm
C_g	5.62 pF/cm	5.62 pF/cm	5.62 pF/cm
R_i	0.1 Ω-cm	0.1 Ω-cm	0.1 Ω-cm
R_d, R_s	0.05 Ω-cm	0.05 Ω-cm	0.05 Ω-cm
g_m	2.2 S/cm	2.2 S/cm	2.2 S/cm
R_0	5 Ω-cm	5 Ω-cm	5 Ω-cm
τ_0	2 psec	2 psec	2 psec

III. METHOD OF ANALYSIS

A. FET Distributed Model

Fig. 2 shows the cross-sectional view of the modeled FET structure. The magnetic walls shown in this figure simulate the periodic continuation of the structure in multifinger FET geometries such as those shown in Fig. 1. The assumption of lateral symmetry allows one section containing a single gate finger to be modeled, with simple scaling being applicable for multiple gate fingers. The source, drain, and gate electrodes, together with the ground plane on the back of the FET structure, form a system of coupled transmission lines and can be modeled [5] by the distributed equivalent circuit shown in Fig. 3. In this approach, the active region of the FET is modeled by the conventional FET equivalent circuit embedded in the transmission lines. A similar, but simplified, distributed model of the FET has been widely used by several groups [6]–[8]. The self and mutual inductances and inter-electrode capacitances, shown in Fig. 3, were calculated using the procedures described by Heinrich [5] and are listed in Table I. Details of the derivation of the distributed element values can be found in [5]. It is sufficient to note here that the simplified approach using the distributed equivalent-circuit model was shown to be in good agreement with a more rigorous full-wave analysis [9]. The longitudinal L and R terms in Fig. 3 also include the frequency-dependent internal resistances and inductances of the various electrodes [5]. The internal inductances were very small compared to the other inductances and, hence, were neglected. The internal resistances of the source and drain electrodes were frequency dependent and varied from 32 $\Omega \cdot$ cm at 5 GHz to 109 $\Omega \cdot$ cm at 100 GHz. To simplify calculations, a frequency-independent value of 50 $\Omega \cdot$cm was assumed since these resistances are small in comparison with the other impedances in series with them. The internal resistance of the gate varies only 5% in the frequency range of 5–100 GHz and, hence, a constant value of 1200 $\Omega \cdot$ cm was used. The gate–drain feedback capacitance $C_{\rm gd}$ is a very important parasitic element that seriously degrades RF performance. The experimentally observed values for $C_{\rm gd}$ are usually higher than the value of 1 pF/cm calculated using the above transmission-line modeling techniques, probably due to the finite conductivity of the channel under the gate. Due to the importance of $C_{\rm gd}$ on RF performance, we used a higher value of 1.5 pF/cm for $C_{\rm gd}$ in our simulations.

The source vias were modeled as lumped inductors and are designated in Fig. 3 as $L_{\rm via}$. Our calculations were performed for various $L_{\rm via}$ values of practical interest. It may be noted that the $L_{\rm via}$ values quoted in this paper correspond to one gate finger and can be scaled for multifinger devices. For example, in practice, the via inductance typically ranges from 10 to 20 pH, depending on via size and substrate thickness, and since 5–10 gate fingers are commonly grounded through this via, simple scaling leads to via inductance per gate finger in the range of 50–200 pH.

The distributed equivalent circuit of Fig. 3 was analyzed using Touchstone to calculate s-parameters and small-signal gain. Ten unit cell sections were used in these calculations and the unit cell width was varied from 5–15 μm, which corresponds to unit gatewidths in the range of 50–150 μm.

B. Determination of Effective Source Inductance

The s-parameters calculated from the distributed model were fitted to the conventional lumped-element FET model shown in Fig. 4, and the source inductance L_s determined in this manner

$$\mathrm{MAG} = \left(\frac{f_t}{f}\right)^2 \frac{1}{\left[4g_o\left(R_g + R_i + R_s + \pi f_t L_s\right) + 4\pi f_t C_{\rm gd}\left(2R_g + R_i + R_s + 2\pi f_t L_s\right)\right]} \tag{1}$$

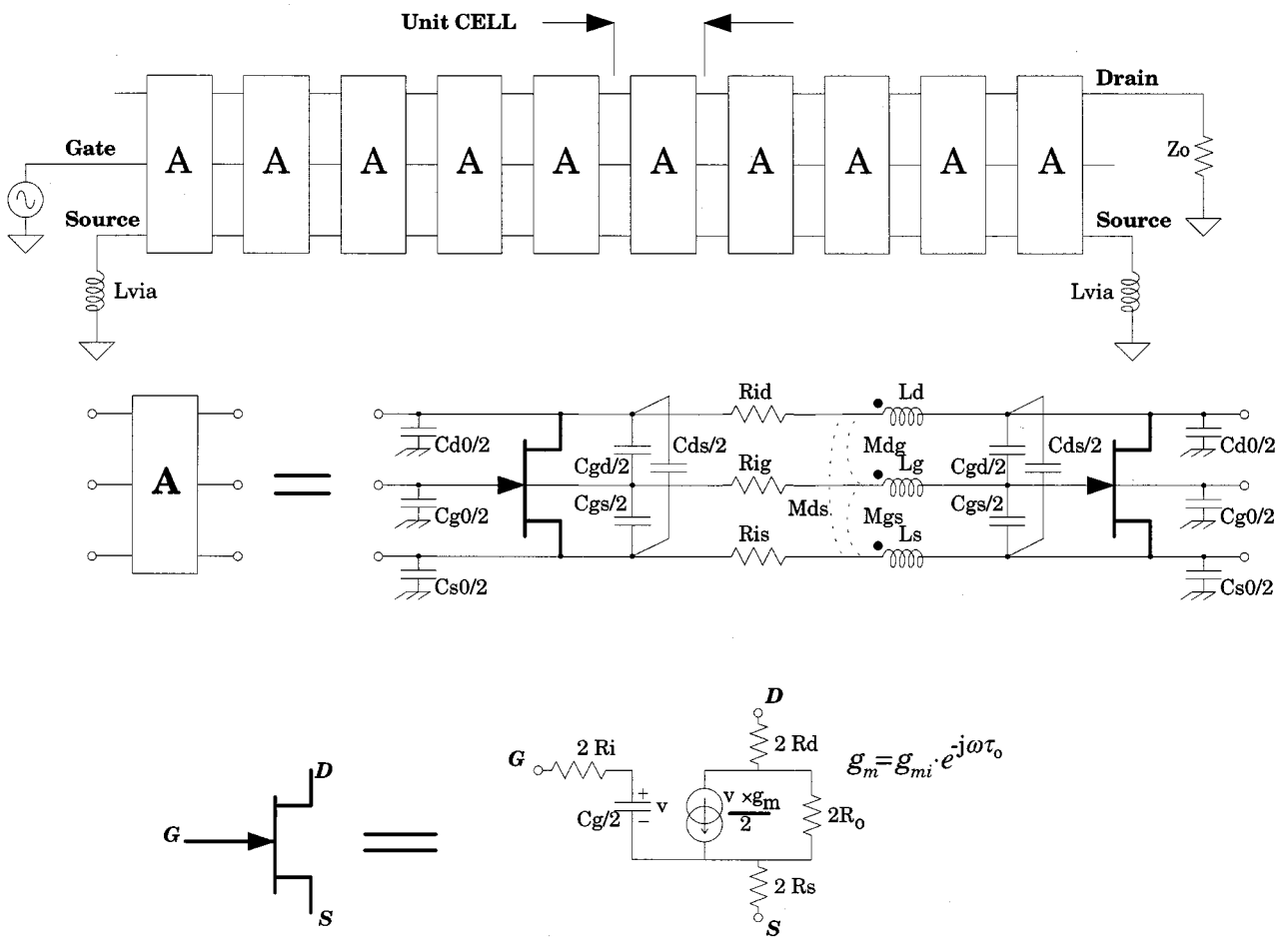

Fig. 3. Distributed equivalent-circuit model of the FET structure.

is defined as the effective source inductance. To ensure the validity of the lumped model, we used s-parameters only up to 25 GHz for fitting. Fig. 5 shows an example of the s-parameters calculated from the distributed model and fitted to the lumped-element model. It can be seen that the lumped model fits the data very well. Similar good fits were obtained for all cases, clearly showing the validity of the lumped model and this approach for determining the effective source inductance.

IV. Results

A. Effective Source Inductance of Different Structures

The lumped-element equivalent-circuit values determined using the procedures described in the previous section are summarized in Table II for the conventional and the novel FET structures with unit gatewidth of 100 mm and via inductance of 100-pH per gate finger. Note that when scaled for a device with ten gate fingers (1-μm gate periphery), the 100-pH via inductance assumed in these calculations corresponds to 10 pH, a value close to that normally obtained for a 100-μm diameter via in a 100-μm-thick substrate [10]. It can be seen in Table II that the values of the intrinsic FET parameters (g_m, C_{gs}, R_{ds}, t_0) are quite similar for the different structures and are consistent with the values expected for a 100-μm-wide device (see Table I). However, significant differences can be noted in

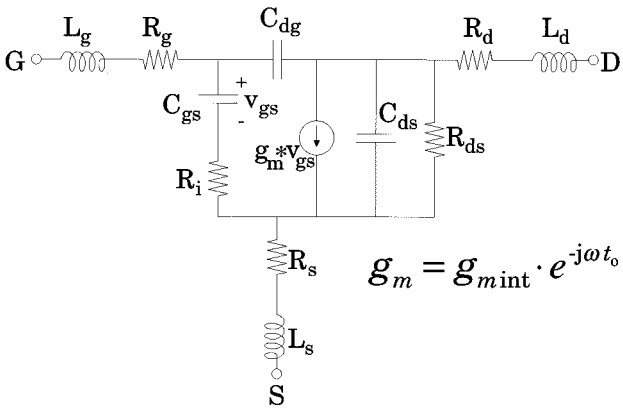

Fig. 4. Schematic diagram of the FET lumped-element equivalent circuit.

the gate, drain, and source inductance values. It is particularly interesting to note that the effective source inductance value for the new device structure with source grounding vias on two sides is very low and much lower than the value of 50 pH expected from the parallel combination of two 100-pH vias. (See Appendix for discussion of sensitivity of the extraction procedure used for determining the effective inductance.) The reduced inductance also leads to the expected higher gain, as shown in Fig. 6. Thus, it is clear that the new FET structure will lead to improved device performance without the need for

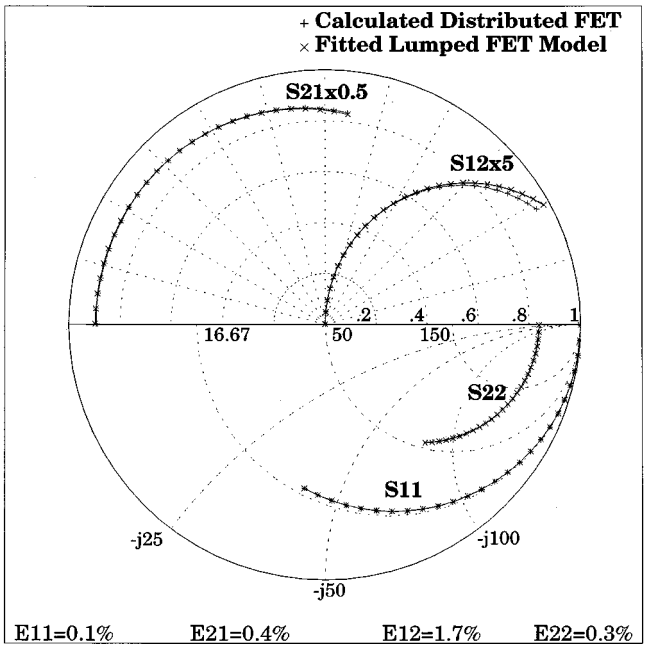

Fig. 5. Calculated s-parameters of the distributed FET equivalent circuit overlaid with s-parameters of the fitted lumped-element model. $W_g = 100\ \mu$m, $h = 100\ \mu$m, and $L_{\rm via} = 200$ pH per gate finger.

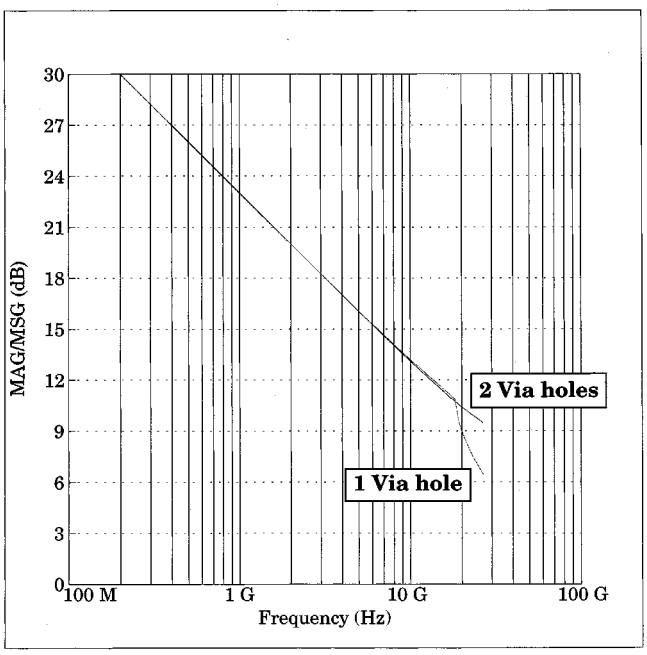

Fig. 6. Calculated gain for the conventional (one via) and proposed (two vias) structures. $W_g = 100\ \mu$m, $h = 100\ \mu$m, and $L_{\rm via} = 200$ pH per gate finger.

very thin chips and the complicated process schemes currently used to achieve low source inductance. The physical reason for this behavior and also the observed differences in the gate and drain inductances are discussed in Section V.

B. Effect of Via Inductance and Unit Gatewidth

The effective source inductance calculations were also repeated for various values of via inductances and unit gatewidths,

TABLE II
EXTRACTED LUMPED-ELEMENT EQUIVALENT-CIRCUIT PARAMETERS FOR THE CONVENTIONAL AND MODIFIED STRUCTURES FOR $h = 100\ \mu$m, $W_g = 100\ \mu$m, AND $L_{\rm via} = 100$ pH

	Conventional Structure	Proposed Structure
C_{gs}	67.5 fF	66.2 fF
R_{gs}	>1 GΩ	>1 GΩ
C_{ds}	22.7 fF	23.3 fF
R_{ds}	509 Ω	511Ω
C_{gd}	14.9 fF	14.9 fF
R_{gd}	>1 GΩ	>1 GΩ
R_i	10 Ω	10 Ω
g_m	22.2 mS	22 mS
τ_0	1 psec	0.7 psec
R_g	5.2 Ω	4.5 Ω
R_d	5 Ω	5 Ω
R_s	5 Ω	5 Ω
L_g	1 pH	87.4 pH
L_d	563 pH	106 pH
L_s	83 pH	1.2 pH

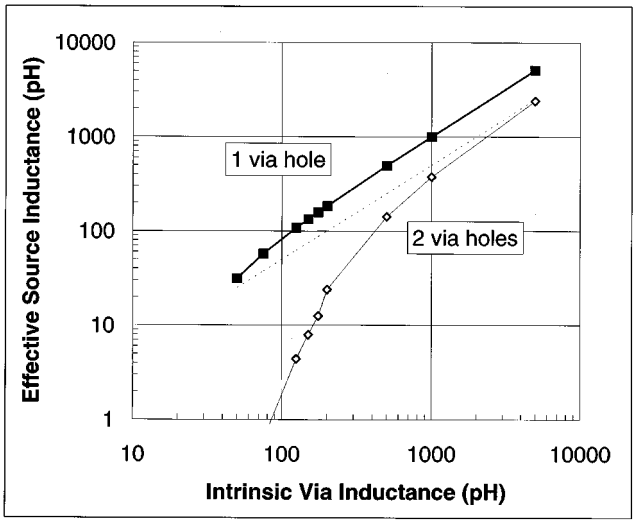

Fig. 7. Effective source inductance versus via inductance for $W_g = 100\ \mu$m and $h = 100\ \mu$m. Dashed line shows $L_{\rm via}/2$ expected for a parallel combination of two vias.

and these results are plotted in Figs. 7 and 8. It can be seen in Fig. 7 that, for several values of the via inductance, the new structure provides a much lower source inductance compared to the conventional structure. However, as the via inductance is increased, the effective source inductance of the new structure increases and finally approaches the value of half the via inductance as expected for the parallel combination of two vias.

The effective source inductances for unit gatewidths of 50, 100, and 150 μm are shown in Fig. 8. It can be observed that the reduction in source inductance achieved with the new structure is smaller for the narrower unit gatewidth devices. The reason for this behavior is described in Section V.

C. Effect of Substrate Thickness

When the substrate thickness is changed, the distance of the ground plane to the FET electrodes becomes different and, thus, changes the transmission-line parameters of the

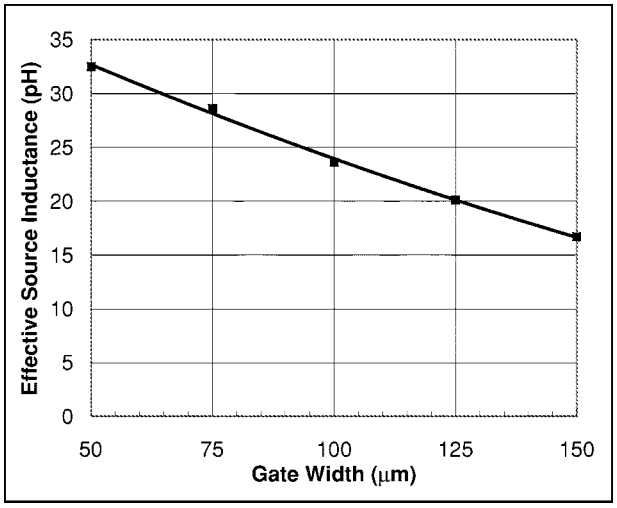

Fig. 8. Effective source inductance of the two via structure for various unit gatewidths. $h = 100\ \mu$m and $L_{\rm via} = 200$ pH per gate finger.

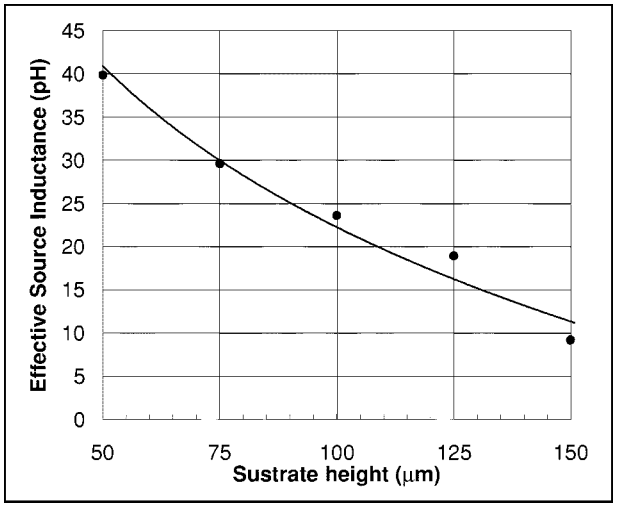

Fig. 9. Effective source inductance of the two via structure for different substrate heights. $W_g = 100\ \mu$m and $L_{\rm via} = 200$ pH per gate finger.

distributed equivalent-circuit model. The effect of this on the effective source inductance is shown in Fig. 9 for three different substrate thicknesses. It can be seen that, for a given via inductance, a greater reduction in source inductance can be achieved with thicker substrates. However, it may be noted that, for a given via size, thicker substrates will also lead to higher via inductance and, as shown in the previous section, this will lead to a higher source inductance. This tradeoff clearly points out the need for careful optimization of substrate thickness and via inductance to achieve desired device performance.

V. Discussion

While the numerical simulations presented thus far clearly show the advantages of the new structure in reducing the effective source inductance, it is useful to gain an insight into the physical reason for the observed behavior. To begin this discussion, it may be recognized that the deleterious effect of source inductance on high-frequency gain arises due to the flow of gate and drain currents through the common-source inductance, as

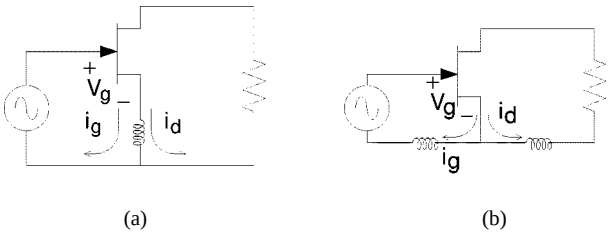

Fig. 10. (a) Illustration of negative feedback due to common-source inductance. (b) Separate return paths eliminates feedback.

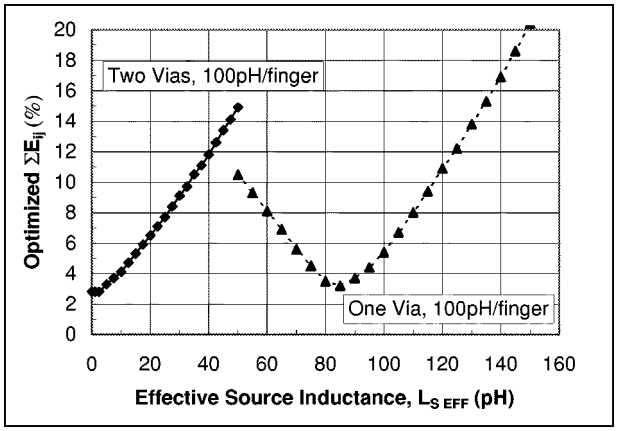

Fig. 11. Optimized error E for various effective source inductance values for the two via and one via structures. $W_g = 100\ \mu$m and $h = 100\ \mu$m. $L_{\rm via} = 100$ pH per gate finger.

shown in Fig. 10(a). The drain current flowing through this inductance leads to an effective resistance on the input side and, thus, lowers gain. It is clear that if we can provide separate return paths for the drain and gate currents, as shown in Fig. 10(b), then the feedback mechanism is eliminated. It is interesting to note that this fact was recognized in vacuum tube work, and triodes with two cathode leads were manufactured [11], and were found to have very low input loading. The present work was motivated by our goal to achieve a similar separation in FET structures while maintaining a common ground between the input and output. An examination of the transmission-line model (Fig. 3) and the high values of the self and mutual inductances listed in Table I clearly shows that the total inductance is very low for drain current returning to ground through the via on the drain side and is much higher for the return path through the via on the gate side. A similar observation applies for the gate current return path with the gate side via being the preferred return path. Thus, most of the drain and gate return currents preferentially flow to separate vias, thus achieving the desired separation. It is easy to see that high values of via inductances will reduce the extent of this separation, whereas wider unit gatewidths will enhance this effect. The numerical simulations clearly show both of these effects. When the substrate thickness is reduced, the self and mutual inductances between the drain, source, and gate electrodes are reduced, which leads to less effective separation of currents and, hence, higher effective source inductances as shown by the numerical simulation. It may also be noted here that the present analysis applies to the case of structures with a large number of fingers where self and mutual inductances are high. In the case of devices with single

fingers, it can be easily shown using coupled-line analysis that the self and mutual inductances will be lower and, hence, the effectiveness of using two vias will be less. Therefore, any experimental verification of the present theory will have to be done using multifinger devices.

The present method of analysis using the transmission-line model derived from coupled line theory is just the starting point and is intended to provide insight and guidance for further analysis of traveling-wave effects in FET structures. Experimental verification and more detailed analysis using detailed electromagnetic modeling and including the effects of input and output feed structures are subjects for future research.

VI. Conclusions

In this paper, we have presented a novel FET structure to reduce common-source inductance. In this new structure, the reduction in common-source inductance is achieved by effectively providing separate paths for the drain and gate return currents to eliminate feedback that causes gain degradation. Detailed transmission-line modeling of the new structure shows that a significant reduction in common-source inductance and improvement in RF performance can be achieved even for moderately high values of source via inductance. The new structure allows simpler fabrication technology and is expected to be particularly useful to reduce the cost and improve the performance of high-power microwave and millimeter-wave devices and circuits.

Appendix

The sensitivity of the parameter-extraction procedure in determining the effective source inductance is an important issue and was determined as follows. The source inductance was fixed at various values, and lumped-element parameter extraction was done to obtain the best fit to the distributed model data by minimizing the error defined by

$$E = \sum_{i=1}^{2}\sum_{j=1}^{2} E_{ij}$$

$$E_{ij} = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left|\frac{s_{ij,\,k\,\mathrm{model}} - s_{ij,\,k\,\mathrm{data}}}{s_{ij,\,k\,\mathrm{data}}}\right|^2}$$

where $s_{ij,\,k\,\mathrm{data}}$ is the distributed model s-parameters, $s_{ij,\,k\,\mathrm{model}}$ is the fitted lumped-element s-parameters, and N is the number of frequency points. The error E is shown in Fig. 11 for two specific examples. It can be seen that the error reaches a minimum and rises rapidly for other values of inductance, thus clearly showing the sensitivity of the extraction procedure in determining the source inductance.

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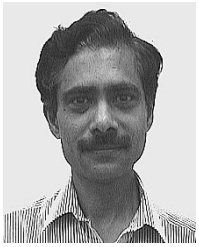

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