Accurate Circuit Model of Interdigital Capacitor and Its Application to Design of New Quasi-Lumped Miniaturized Filters with Suppression of Harmonic Resonance

Lei Zhu, *Member, IEEE,* and Ke Wu, *Senior Member, IEEE*

***Abstract*—A general-purpose circuit model of microstrip interdigital capacitor (IDC) is presented in this paper for use in the design of new quasi-lumped miniaturized filters. This computer-aided-design-oriented model is developed as a versatile admittance π-network with the short-open calibration technique that we have recently proposed for accurate parameter extraction of a circuit from its physical layout. This technique is self-contained in our method of moments, which accounts for frequency dispersion and fringing effects. A J-inverter topology is further conceived to explicitly formulate the coupling behavior of three types of IDC's. This model provides a unique way for the IDC-related circuit synthesis and optimization based on the accurate equivalent-circuit network extracted from the field theory algorithm. It is validated theoretically and experimentally through an example of a line resonator connected with two IDC's. The proposed scheme is used in the design and optimization of new low-loss miniaturized quasi-lumped integrated circuits, namely, two types of three-pole direct-coupled bandpass filters. Our measured and predicted results show interesting features of the proposed filter structure such as size reduction and suppression of harmonic resonance if the line resonator is attached by series-connected equivalent inductance.**

***Index Terms*—Interdigital capacitor, CAD, microstrip line, method of moments, bandpass filter, numerical calibration technique, synthesis and optimization scheme, equivalent circuit.**

I. Introduction

MICROSTRIP interdigital capacitors (IDC's) have been widely used as a quasi-lumped elements in high-frequency and high-speed integrated circuits (IC's) [1]–[4]. In earlier days, various two-dimensional (2-D) static algorithms were applied for deriving its computer-aided design (CAD) model. Unfortunately, such a model may not be reliable since it has to ignore the fringing field effects of multiple finger ends [1], [2] or it roughly accounts for a partial amount of these effects such as the end capacitance [3]. Very recently, a lumped *LC*-network model [4] has been proposed for the CAD purpose and it was derived from a partial-element description (PED) in a three-dimensional (3-D) method of moments (MoM). Nevertheless, this model is valid only for a frequency range in which the total IDC size is a small fraction of the operating wavelength. Since the strip width around the finger section is electrically narrow in this case, a large amount of difficult-to-characterize parasitic effects may become significant [2] such as conductance loss. These effects may cause low Q-factor and probably hinder the IDC itself from its application to the design of high-performance circuits such as low-loss bandpass filters. In addition, such effects may lead to some potential difficulty in the accurate determination of circuit parameters representing the IDC physical layout. To remove or at least reduce these unwanted parasitic effects, we direct our attention to the characterization of IDC's with size comparable to the operating wavelength. Therefore, this type of circuit should be handled as a distributed model considering frequency dispersion and other field effects.

Our deterministic MoM algorithm has recently been developed for the characterization of unbounded multiport microstrip circuits [9] that makes use of impressed voltage excitation, as described in [5]–[8]. This technique allows the simulation of a complete IDC-related circuit, which may call for a field-theory-based optimization procedure [10] through very heavy and lengthy back-and-forth iterations. Nevertheless, the preferred approach is still to use accurate circuit representation of physical layout for a rapid and efficient design with the well-developed synthesis and optimization schemes based on circuit network [11], [12]. In this study, our newly developed short-open calibration (SOC) technique [13]–[16], is applied to explore a unified CAD model for a generalized IDC structure. This SOC concept was inspired from the well-known thru-reflection line (TRL) calibration procedure [17] and it is self-contained in our MoM algorithm [9]. Circuit parameters of the model are extracted from MoM calculations using two calibration elements, namely, "short" and "open" lines. In the absence of any hypothetical condition, this model accounts for all the parasitic effects at any frequency as far as the MoM accuracy is guaranteed.

This paper is an extended version of [18], systematically describing the parameter extraction and features of the proposed IDC model. In this paper, three types of IDC's are studied to showcase the use and performance of the proposed model. Validated with a single IDC, this technique is then applied to the optimization and synthesis of IDC-related bandpass filters using

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The authors are with the Poly-Grames Research Center, Department of Electrical and Computer Engineering, Ecole Polytechnique, University of Montréal, Montréal, P.Q., Canada H3C 3A7.

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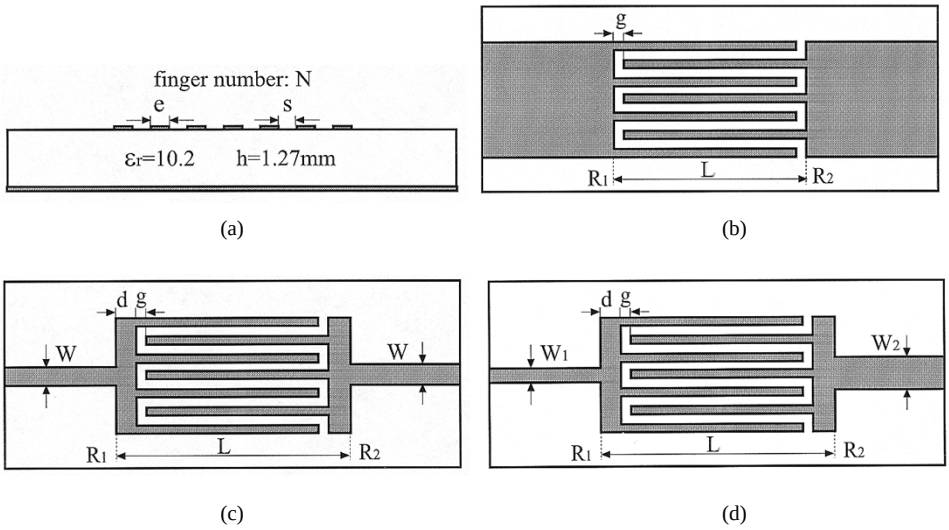


Fig. 1. Cross-sectional view and physical layout description of three types of IDC's with predesignated geometrical dimensions and parameters of structure. (a) Cross section of multiple finger. (b) IDC (Type A). (c) IDC (Type B). (d) IDC (Type C).

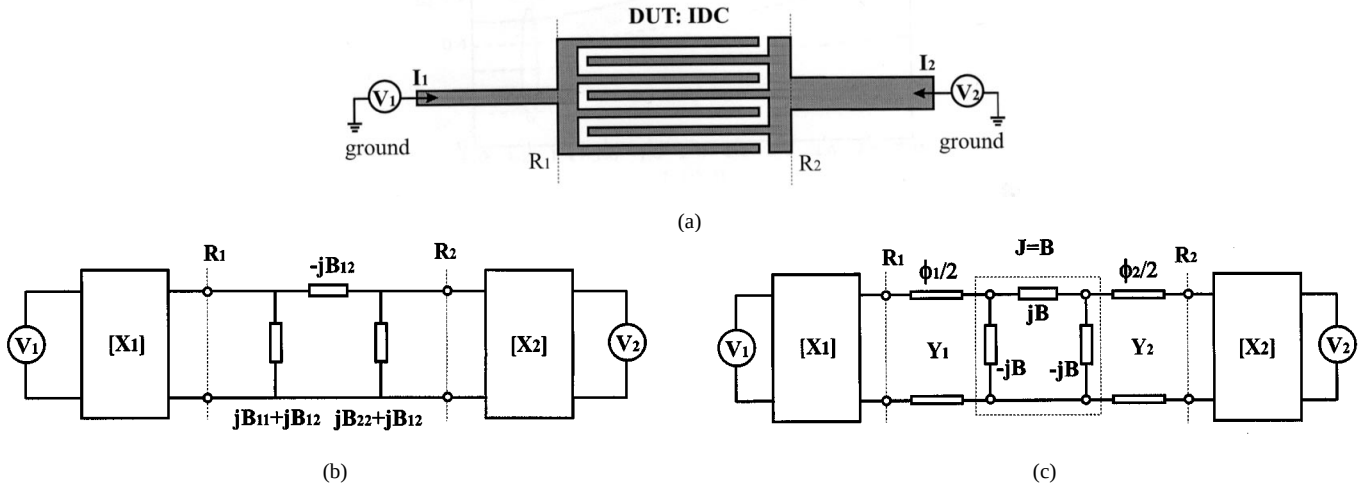


Fig. 2. Physical topology and equivalent-circuit representation prepared for MoM characterization of a generalized IDC attached with two different lines. (a) Physical layout. (b) Susceptance network. (c) *J*-inverter network.

a unified equivalent-circuit network approach [12]. Two direct-coupled bandpass filters are designed and attractive features of a new class of filters using series-connected inductance line are observed theoretically and experimentally as to size reduction and suppression of harmonic resonances.

II. Circuit Model of IDC Structure

Fig. 1(a) describes the cross-sectional view of a typical IDC with multiple fingers while Fig. 1(b)–(d) depict a geometrical sketch of three types of IDC's [1]–[4] to be studied that are attached with two lines as the input/output. In the following, a general-purpose circuit model is described for efficient design and optimization of IDC-related low-loss miniaturized filters based on the versatile lumped-element network approach. To do so, we begin with a deterministic MoM algorithm to simulate IDC's [9]. The SOC technique is then applied to extract a CAD-oriented circuit model from field calculations and it is embedded in the MoM algorithm [13]–[16]. In the end, a J-inverter network is derived to explicitly evaluate the coupling characteristics of the IDC.

A. Full-Wave MoM Algorithm

Fig. 2(a) shows a physical layout prepared for the full-wave MoM characterization of a generalized IDC attached with two input/output lines. To have a general-purpose design requirement, the two lines may be different in width. As described in previous MoM algorithms, e.g., as in [5]–[8], a pair of impressed voltage sources backed by electrical walls is introduced at the reference planes (ports) of choice on the lines. The port locations are electrically far away from the circuit discontinuity to avoid any potential electromagnetic interaction between fields of the ports and discontinuity. It was done in our developed MoM scheme [9] for formulating unbounded multiport planar circuit problems, thus avoiding potential parasitic resonance caused by a shielding enclosure.

The entire IDC is segmented into two distinct parts: *uniform lines* (R_1-V_1) and (R_2-V_2), in which a dominant mode propa-

gates, and *circuit discontinuity* $(R_1 - R_2)$, to which all discontinuity effects are attributed. The use of the image principle leads to the removal of the local electrical walls by an appropriate choice of the Green's functions for the lines and discontinuity so that an unbounded environment is effectively created. With the help of the Galerkin's technique, a source-type matrix equation can be derived, which allows calculation of current density distributed over the transverse meshes at each port location as well as the discontinuity. With the concept of port voltage and current derived from the impressed electric fields and a superposition of the calculated electric density at the port location, an equivalent network can be deduced that interrelates the port voltages and currents, namely, V_i and I_i $(i = 1, 2)$ for the IDC.

B. SOC Procedure

Described below is a deembedding (calibration) procedure applied to the IDC structure to accurately extract parameters of its equivalent-circuit network designated between the reference planes R_1 and R_2. The essence of the proposed SOC procedure is to electrically formulate the IDC physical layout with the lumped elements in a very precise manner. This SOC technique should be able to remove all susceptible numerical noise and MoM model error such as the approximate impressed voltage source. In this way, any circuit parameters can be extracted even though some of them may be far below the intrinsic numerical noise. Fig. 2(b) shows an equivalent lumped model of Fig. 2(a), in which the IDC is modeled as an admittance π-network. The two terms $[X_1]$ and $[X_2]$ stand for parasitic effects of the so-called port discontinuity [16] and inconsistency problem between two-dimensional (2-D) and 3-D models when solving the same line problem. These errors terms, even if very small, are usually frequency- or dimension-dependent and may be very harmful in the parameter extraction [18]. They should be removed from the circuit model.

In a TRL calibration procedure used for circuit measurements [17], three standard elements are applied to remove the error boxes and calibrate the measured parameters for a device-under-test (DUT). In our case, two elements are proposed to work out in a similar way, namely, "short" and "open" lines that are defined in the MoM algorithm. Fig. 3(a) and (b) show the physical layout and equivalent-circuit network of such two elements. Since each error term can be separately calibrated with respect to the attached line by using a pair of calibration elements, this SOC technique is well suitable to deembedding the IDC connected with two different lines. As discussed in [13]–[16], the two SOC elements can be exactly built up by exciting a pair of odd and even impressed voltage at the two ports of a uniform line having a length twice the distance between the port and reference planes of the line. Since its center location simulates ideally the perfect electric (short) and magnetic (open) wall by applying odd and even sources, respectively, such a uniform line is divided into two identical parts, one of which is used to evaluate the error term. Our MoM algorithm briefly described above is applied to calculate the current density over this line. As such, an $ABCD$ matrix representing the error term $[X]$ can analytically be obtained through the solution of three groups of equation on the basis of network theory in connection with the port currents for the

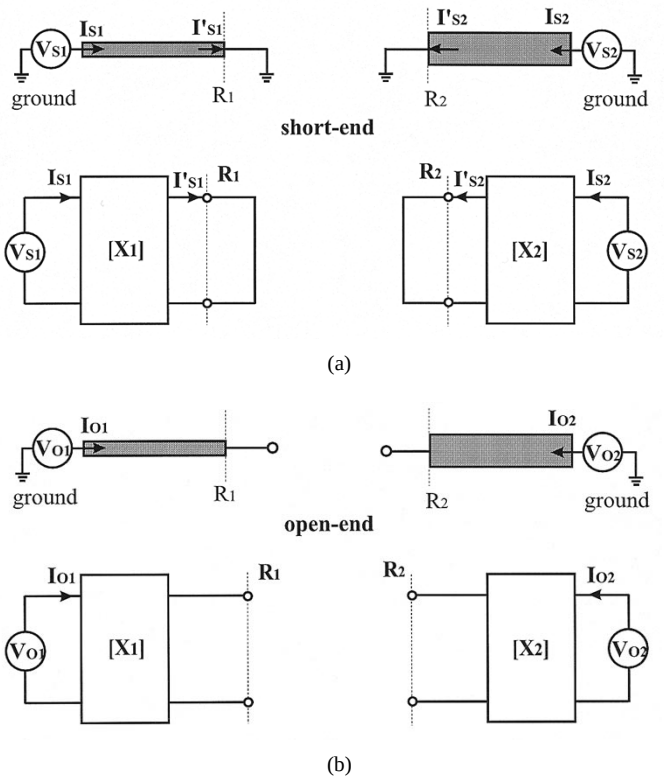


Fig. 3. Physical arrangement and network representation of our proposed SOC scheme with two standard calibration elements. (a) Short element with error box equivalence. (b) Open element with error box equivalence.

odd and even excitations, and the current flowing at the short end, namely, I_{si}, I_{oi}, and I'_{si}. Furthermore, this matrix can explicitly be expressed by the currents normalized with respect to the port voltages V_{is} and V_{io} as a closed-form equation

$$[X_i] = \begin{bmatrix} \bar{I}_{is}/\bar{I}'_{is} & -1/\bar{I}'_{is} \\ -\bar{I}'_{is}\bar{I}_{io}/(\bar{I}_{is} - \bar{I}_{io}) & \bar{I}'_{is}/(\bar{I}_{is} - \bar{I}_{io}) \end{bmatrix} \quad (1)$$

in which $\bar{I}_{io}$, $\bar{I}_{is}$ and $\bar{I}'_{is}$ represent the three normalized currents. In this way, the error terms related to each line can be extracted from (1) with the two SOC elements in the MoM scheme. The admittance π-network can be set up. This model can further be simplified into a susceptance π-network if the lossless case is considered.

C. J-Inverter Network

The derived admittance parameters of an IDC usually exhibit a strong frequency dependency that is not suitable for characterizing its coupling behavior because of the distributed coupling effect. On the other hand, our interests are to use the IDC for filter design. Therefore, the π-network is transformed into its corresponding J-inverter topology, consisting of a susceptance and two equivalent lines, as shown in Fig. 2(c). This alternative notation is useful for design and optimization using the network-based synthesis technique [12]. The J-inverter susceptance J is directly proportional to the coupling (or strength) of the IDC, while the equivalence of two attached electrical lines ϕ_1 and ϕ_2 presents distributed fringing field effects and finger end discontinuities. The equivalence between the two networks allows for deriving a set of new equations that relate the

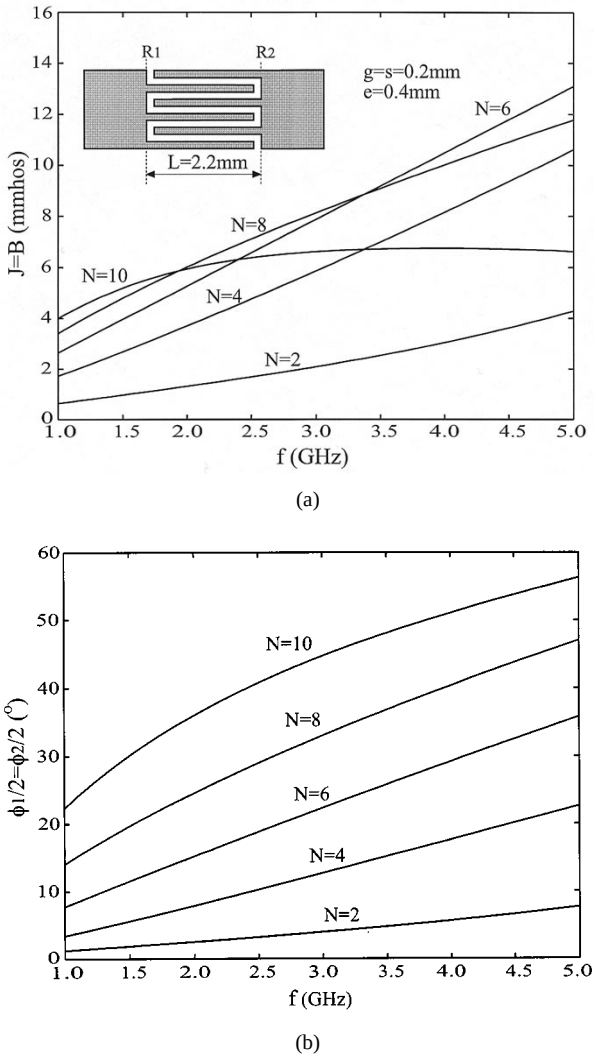


Fig. 4. Extracted parameters of the equivalent network of an IDC (Type A) as a function of frequency versus the number of finger with $N = 2, 4, 6, 8, 10$ (even). (a) J-inverter susceptance J. (b) Equivalent electrical line length $\phi_1/2 = \phi_2/2$.

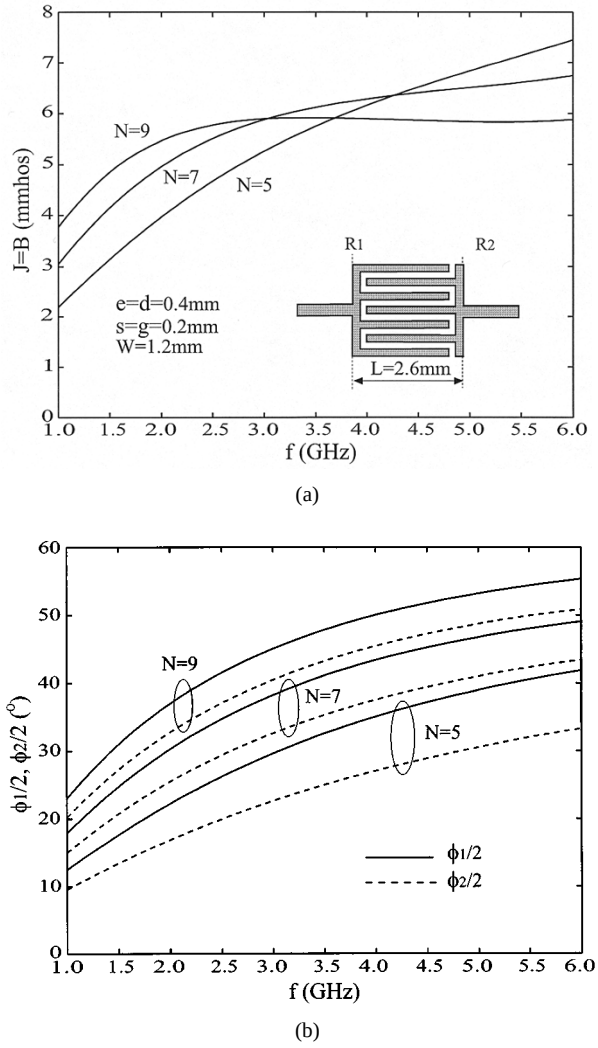


Fig. 5. Frequency dependence of the extracted parameters of equivalent network of an IDC (Type B) versus the number of finger with $N = 5, 7, 9$ (odd). (a) J-inverter susceptance J. (b) Equivalent electrical line lengths $\phi_1/2$ and $\phi_2/2$.

J-inverter parameters and its original network counterparts involving two different generalized lines

$$\frac{J}{\sqrt{Y_1 Y_2}} = \frac{\sin(\phi_1/2) + \bar{B}_{11}\cos(\phi_1/2)}{\bar{B}_{12}\sin(\phi_2/2)} \tag{2a}$$

$$\phi_1 = -\tan^{-1}\left\{\frac{2(\bar{B}_{11} + \bar{B}_{22}|\bar{B}|)}{1 + \bar{B}_{22}^2 - \bar{B}_{11}^2 - |\bar{B}|^2}\right\} \tag{2b}$$

$$\phi_2 = -\tan^{-1}\left\{\frac{2(\bar{B}_{22} + \bar{B}_{11}|\bar{B}|)}{1 + \bar{B}_{11}^2 - \bar{B}_{22}^2 - |\bar{B}|^2}\right\} \tag{2c}$$

in which $\bar{B}_{11} = B_{11}/Y_1, \bar{B}_{22} = B_{22}/Y_2, B_{12} = B_{12}/\sqrt{Y_1 Y_2}$ and $|\bar{B}|^2 = \bar{B}_{11}\bar{B}_{22} - \bar{B}_{12}^2$. Y_1 and Y_2 are the characteristic admittances of two uniform lines in the IDC structure, respectively, as in Fig. 2(a).

These equations are useful for the design and optimization of IDC-related filters since the coupling and dispersion effects are rigorously determined. This is examined in the following examples.

III. IDC Coupling Characteristics and Dispersion Effects

The three types of structure of Fig. 1(b)–(d) are studied for coupling characteristics and dispersion effects. Fig. 4 is the extracted J-inverter susceptance and two equivalent electrical lines as a function of frequency for a symmetrical IDC versus the number of fingers $(N = 2, 4, 6, 8, 10)$. In this example, the strip width is exactly equal to the overall dimension of the multiple finger section, as in Fig. 1(b), so that the parasitic effects happened around the finger section are contributed only by the finger ends. It is found in Fig. 4(a) that the susceptance J increases rapidly with the number of fingers at extremely low frequency (in this example, $f < 1.5$ GHz). It actually indicates the lumped-element characteristics of an IDC in the limiting case for which the total size is much smaller than the operating wavelength, as justified in [3] and [4]. As the frequency goes beyond this limiting

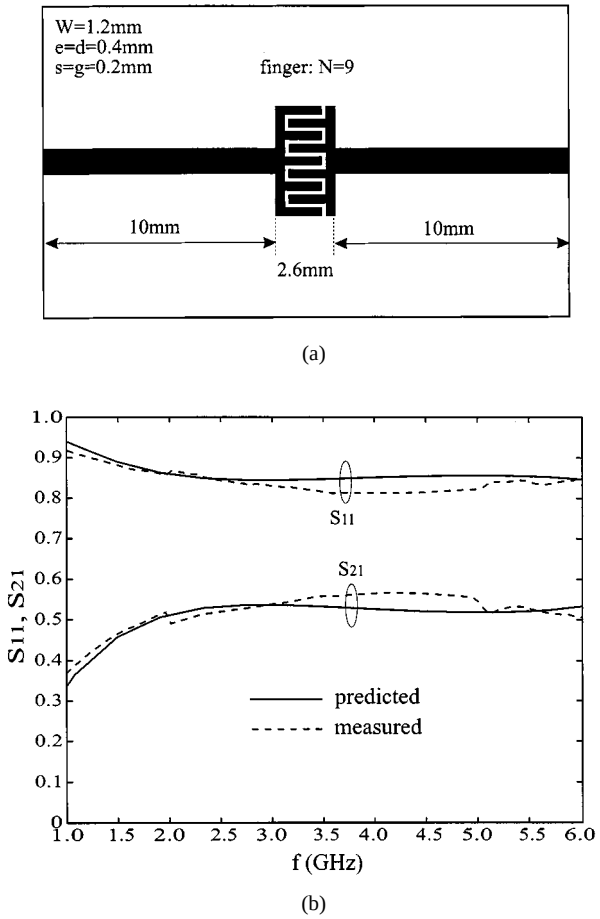


Fig. 6. Predicted and measured insertion and return losses for a simple IDC structure (Type B with $N = 5$) connecting with two 50-Ω lines. (a) Layout sketch. (b) Frequency responses.

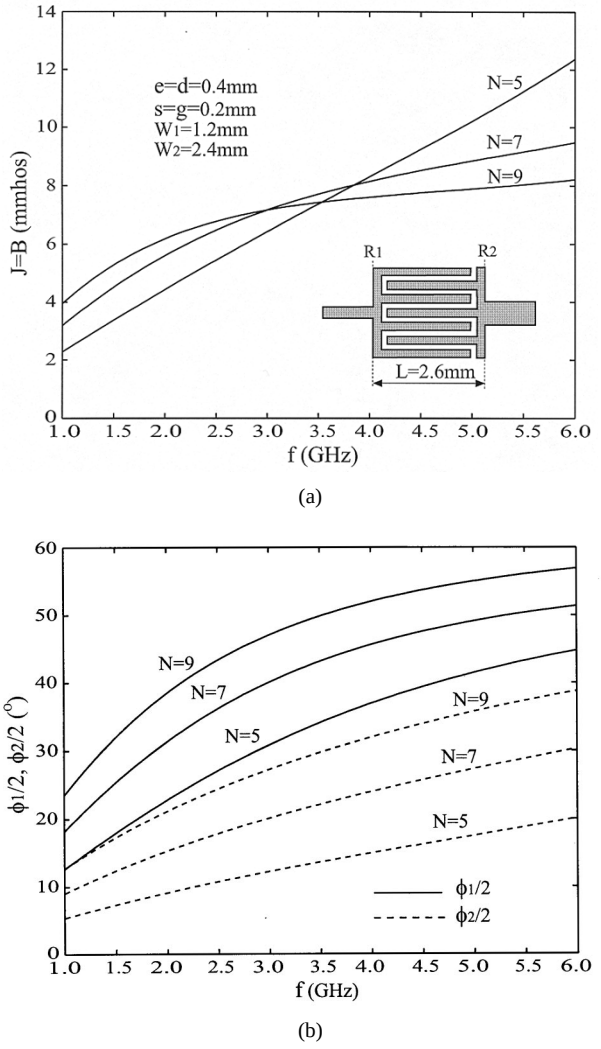


Fig. 7. Extracted equivalent-circuit network and dispersion effects of an IDC (Type C) versus the number of finger with $N = 5, 7, 9$ (odd). (a) J-inverter susceptance J. (b) Equivalent electrical line lengths $\phi_1/2$ and $\phi_2/2$.

point, the susceptance is strongly enhanced for $N < 8$ and it tends to be gradually saturated for $N = 10$. It suggests that the low-frequency lumped effects disappear as the total size (number) of fingers is enlarged to a certain value comparable with the operating wavelength. The structure symmetry and even number of finger yields two identical electrical lengths. Fig. 4(b) shows almost linear phase behavior for different N versus frequency, except for minor nonlinear disturbance for a large N due to its distributed effect.

Fig. 5 shows frequency-dependent J-inverter network parameters for the IDC attached with two identical 50-Ω lines versus three different N (5, 7, 9). With reference to Fig. 5(a), similar distributed behaviors can also be observed, and the saturation effect takes place around 2.5 GHz in, for example, the case of $N = 9$. Nonlinear susceptance curves over $f = 4.0$ GHz for the three cases indicate that the conventional approximate lumped model is no longer valid. As plotted in Fig. 5(b), the two electrical lengths have similar variation with frequency as compared with Fig. 4(b), but there is a visible difference due to the choice of odd number of fingers. In particular, the two electrical phases are not identical with the structure asymmetry. To validate our proposed circuit model, a simple IDC circuit is fabricated with $N = 9$, whose physical layout is displayed in Fig. 6(a). Measured results are in very good agreement with the model prediction even though a small discrepancy of about 5.0% is observed around 4.5 GHz, which may be caused by fabrication or measurement problems.

Now let us look at the IDC structure having two different connection lines that is applied to the design of low-loss miniaturized filters in the subsequent section. Since the narrow strip width of line is primarily responsible for the conductance loss incurred in high-frequency IC's, a relatively wide line is selected to make up the resonator circuit, while the other is designed to be a 50-Ω line connected to the external circuit. Fig. 7 shows J-inverter network parameters extracted for an IDC attached to two lines of 50 and 34 Ω for $N = 5, 7, 9$. Interestingly, the susceptance is enlarged to some extent as opposed to Fig. 5. This may well be interpreted by the interface-related discontinuity effects on the right-hand side of the IDC that are reduced as the linewidth W_2 is widened toward the total width of finger section. Similarly, the electrical length $\phi_2/2$ is found to be reduced by about 6°–4° in the frequency range of interest. The other electrical length $\phi_1/2$, however, appears to be about the same as in Fig. 5(b).

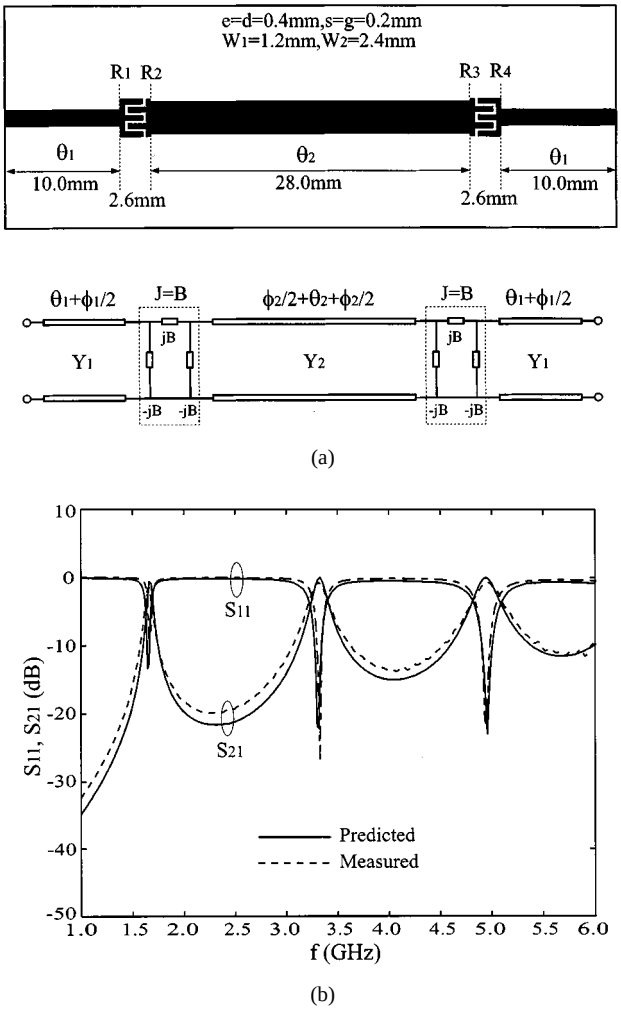


Fig. 8. Equivalence of a global circuit network of an IDC line resonator designed for CAD-oriented model and its predicted and measured frequency responses. (a) Physical layout and network equivalence. (b) Measured and predicted frequency responses.

IV. Filter Design with Size Reduction and Suppression of Harmonic Resonance

In this section, a class of IDC-related filters is designed with the proposed circuit model and our interests are to realize size reduction and suppression of filtering harmonic resonance with new topologies. With the developed circuit model for the three types of IDC presented above, we choose one of the asymmetrical IDC's for use as a tight coupling element for low-loss filter and resonator design. In our study, one IDC line resonator and two bandpass filters are studied theoretically and experimentally. Considering some practical aspect of our experiments, a dielectric substrate of Duroid is fixed with the thickness of 1.27 mm and $\varepsilon_r = 10.2$ through the following calculations.

A. IDC Line Resonator

Fig. 8(a) displays the proposed layout and complete CAD-oriented circuit model of a line resonator interconnected by two asymmetrical IDC structures. The two external lines (50 Ω) are chosen to be different from the line resonator (34 Ω) in strip width, and the number of finger N is five for the IDC. The frequency response and other characteristics of the IDC line resonator can easily be derived from its complete equivalent-circuit model, as shown in Fig. 8(a). In this model, the total electrical length (θ) of the line resonator consists of two parts, namely, the uniform section of the line (θ_2) and the two identical equivalent line lengths $\phi_2/2$ contributed from the two IDC models. Therefore, $\theta = \phi_2/2 + \theta_2 + \phi_2/2$, thereby suggesting that the equivalent electrical length of the two IDC structures affect the resonant frequency of the line resonator. It is usually dispersive due to the distributed characteristics of the IDC.

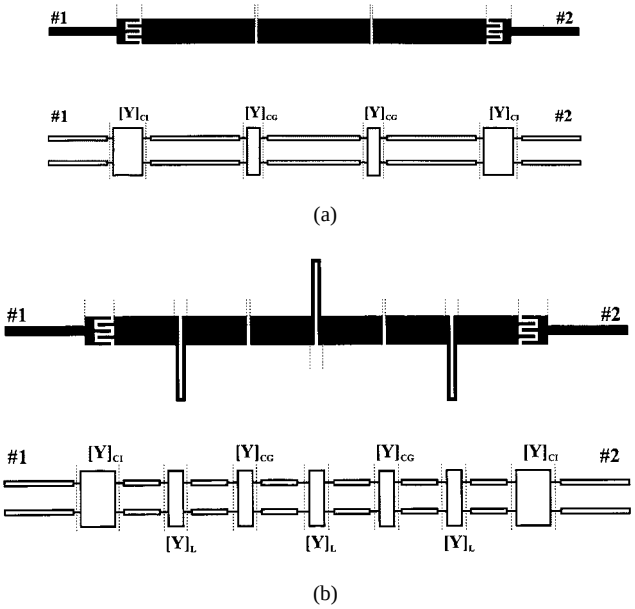


Fig. 9. Circuit description and CAD model of the two types of three-pole direct-coupled bandpass filters. (a) Simple uniform line resonator filter without inductive line compensation. (b) Inductive series-connected shorted stub loaded resonator filter for size reduction and suppression of harmonic resonance.

Similarly, the equivalent network of the externally connected input/output lines should account for effects of the electrical length $\phi_1/2$ on the other side of the J-inverter, as shown in Fig. 8(a). Since the developed J-inverter is explicitly related to the coupling strength between the connecting line and line resonator, the insertion loss and bandwidth of the circuit can be accurately predicted with the proposed model. Calculated and measured frequency responses are presented in Fig. 8(b), showing an excellent agreement over an extremely wide frequency range (1.0–6.0 GHz). Judging from the behavior of S_{21}, the bandpass becomes broader for the higher order of resonant frequency. This is essentially due to the coupling enhancement at higher frequency, as shown in Fig. 7(a), through the characteristics of J-inverter susceptance for $N = 5$.

B. Miniaturized IDC Bandpass Filters with Suppression of Harmonic Resonance

The above example points to the effectiveness and generality of our proposed model for the IDC circuit design using a network approach. In this section, a very efficient network-based synthesis and optimization procedure, as detailed in [13]–[15], is applied to the design of high-quality IDC circuits with minimized computational efforts as opposed to direct, but time-consuming, field-theory-based techniques [10]. In this way, the entire filter is represented in design by an equivalent cascaded cir-

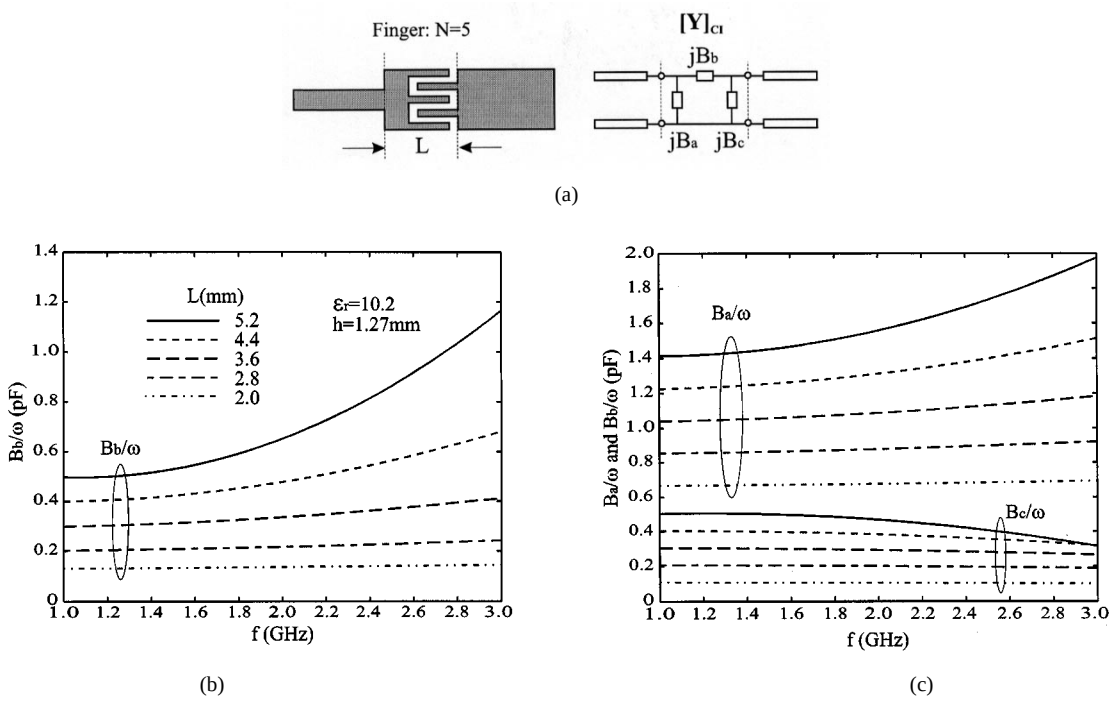


Fig. 10. Extracted design curves of the equivalent network as a function of frequency versus the length of finger section for an asymmetrical IDC. (a) Structure and network sketches. (b) Self-susceptance. (c) Mutual-susceptance.

cuit topology that consists of J-inverter networks and line resonators attached with a series-connected shorted stub element in the following design examples. Once the filter is specified with its characteristics such as central frequency, bandwidth, insertion loss, and number of resonator, all the J-inverter parameters can be calculated in an explicit form with reference to a series of standard design tables or closed-form equations in [13]–[15]. This is usually related to a specific frequency response, such as a maximally flat or Chebyshev type. In our case, each line resonator is designed to operate at the central frequency and its equivalent sloping susceptance parameter is derived from the differentiation of a complete circuit network, as indicated in [21]. In this study, our interest is to design Chebyshev-type IDC bandpass filters. In particular, a new class of miniaturized IDC filters is proposed to suppress the unwanted harmonic resonance over the upper frequency range, thus significantly improving the filter performance and adjacent channel rejection.

Fig. 9(a) and (b) presents the physical layouts and CAD-oriented model of two types of three-pole direct-coupled bandpass filters that use the uniform-line resonator and inductive line-loaded resonator, respectively. These filters operate with quasi-lumped elements whose circuit parameters can accurately be extracted from the above-described SOC technique. Fig. 9(a) shows two asymmetrical IDC coupling elements for interconnecting the line resonators so that a tight coupling is conceptually achieved. Simple gap-coupling structures are used to provide a weak coupling between two adjacent-line resonators. This type of filter structure is usually long in size because the line resonator takes up an appreciable fraction of wavelength. To achieve a dimensional compactness, the resonator lines are split into two pieces and a series-connected shorted stub element having electrically narrow width is inserted to bridge them, as shown in Fig. 9(b). The element generates inductive effect such that the quasi-lumped resonance can take place at lower frequency and the new filter size can significantly be reduced as compared to Fig. 9(a). Obviously, accurate parameter extraction of the quasi-lumped elements is critical for successful design of the proposed filter topology, which should be done with the developed MoM algorithm and SOC technique.

Fig. 10(b) and (c) plots a number of design curves for the extracted self- and mutual-susceptance parameters as a function of frequency for the asymmetrical IDC with $N = 5$, as shown in Fig. 10(a). Within the frequency range of interest (global-positioning-system (GPS) band around 1.575 GHz), the susceptances exhibit a lumped capacitance that gradually increases with extended finger length. Of course, the distributed effects are pronounced over the higher frequency range over where the wavelength is comparable to the finger length. Fig. 11(b) presents a series of curves for the equivalent capacitance versus gap spacing for the gap coupling topology at three different frequencies, whose layout parameters and circuit representation are described in Fig. 11(a). The self-capacitance C_p tends to go up and its mutual counterpart C_g rapidly decreases as frequency goes up. This indicates a reduction of coupling between the open-ends of the two lines. Fig. 12(a) gives the design layout and circuit model of the series-connected shorted stub element, which can be well represented by one series inductance and two shunt capacitances. Fig. 12(b) shows a set of predicted dispersion curves against various stub lengths L that are very useful in design of the new size-reduced IDC filters. It is confirmed that the mutual admittance really points to the effect of a quasi-lumped series inductance, while the shunt susceptance points to a shunt capacitance.

The extracted circuit parameters of Figs. 10–12 are used to design two three-pole bandpass filters with a center frequency

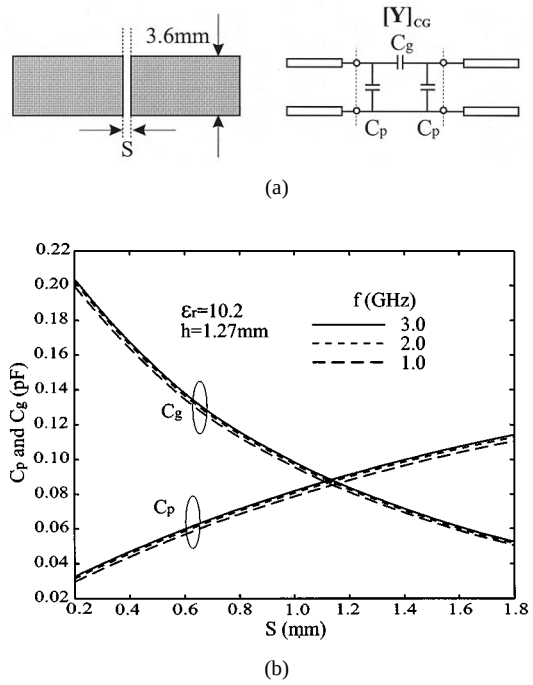


Fig. 11. Calibrated equivalent capacitance of a gap coupling structure for three different frequencies. (a) Physical layout and network equivalence. (b) Self-capacitance and mutual capacitance.

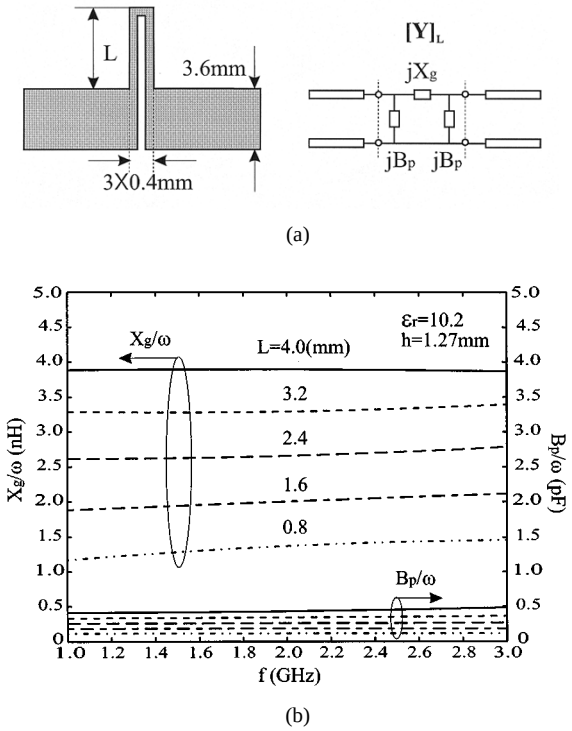


Fig. 12. Calibrated equivalent inductance and capacitance of a series-connected shorted stub element as a function of frequency versus the length of the loaded line section. (a) Physical layout and network equivalence. (b) Shunt capacitance and series inductance.

of 1.575 GHz and a bandwidth of 2.7% (not necessarily a GPS requirement). Fig. 13(a) shows predicted and measured insertion and return losses of our first filter without inductive compensation over a narrow frequency range of 1.48–1.66 GHz. The

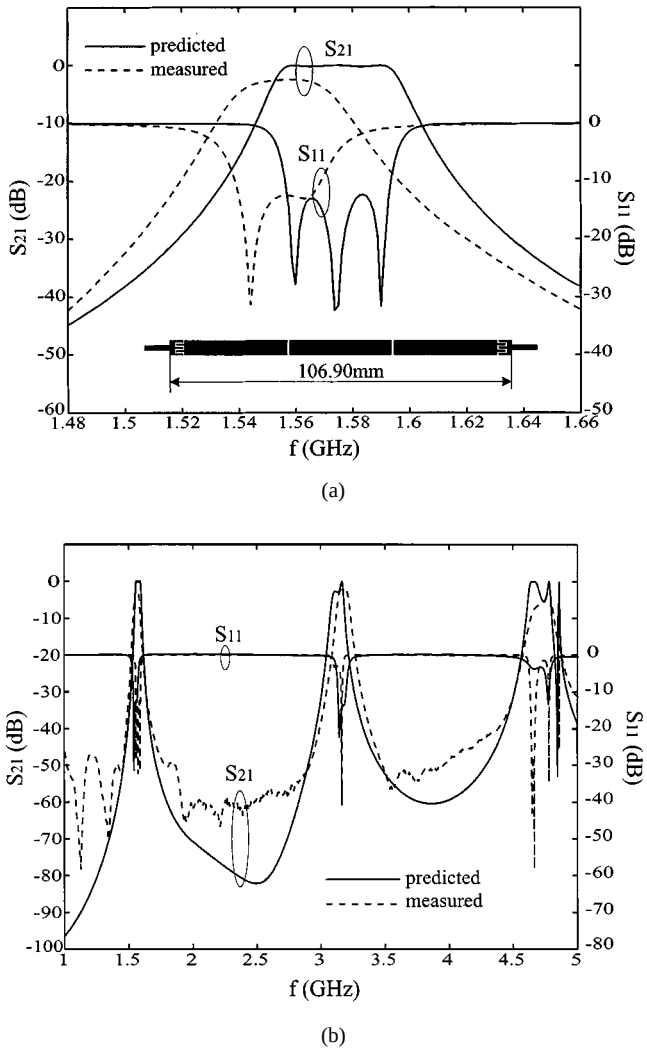
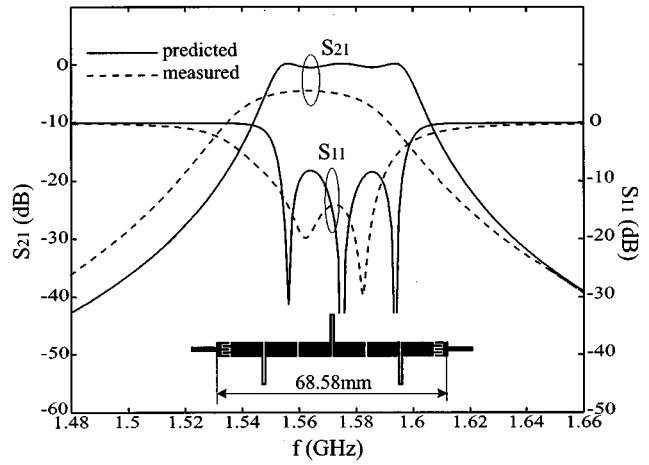


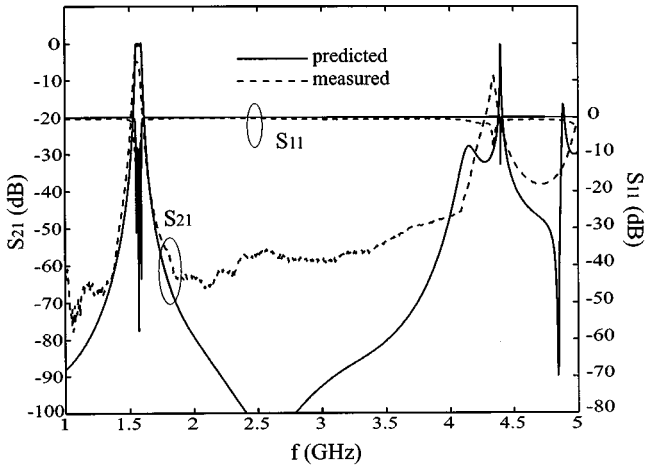
Fig. 13. Predicted and measured results of frequency response for the simple IDC filter that is made up of uniform line resonators. (a) Zoom-in for narrow-band characteristics. (b) Broad-band frequency response.

predicted center frequency is slightly down (within 1.5%) compared with the measured result, and the measured bandwidth is 2.4%. Fig. 13(b) presents the panoramic frequency response, and the second harmonic resonance frequency is found around 3.15 GHz, approximately equal to twice the fundamental resonance. The reduction of 2.4 dB in the insertion loss around 1.56 GHz can be attributed to the conductor loss of the narrow strip of the IDC multiple finger. As described in [19] and [20], an alternate way of overcoming this problem is to use a superconducting conductor for the design of extremely narrow-band filters.

The length of above-described filter is a rather large 106.90 mm. Now let us look at the design aspects of the inductively compensated IDC filters with the proposed circuit model. Fig. 14(a) shows predicted and measured results for a filter that uses the same IDC and gaps as in the above filter design for the purpose of comparison. The length of series-connected shorted stub element is chosen as $L = 4.0$ mm, as discussed in Fig. 12(b), so that the total length of the new filter is significantly shortened to 68.58 mm for the same operating frequency bandwidth as the above example. A slight



(a)



(b)

Fig. 14. Predicted and measured results of frequency response for the compensated IDC filter with inductive series-connected shorted stub loaded resonators and feature presentation for suppression of the second harmonic resonance. (a) Zoom-in for narrow-band characteristics. (b) Broad-band frequency response.

increase in return loss is observed and it can be improved with suitable adjustment of coupling enhancement of the IDC structure. Fig. 14(b) depicts the prediction of complete frequency response over a broad band. It is interesting to find out that the second harmonic resonance is completely suppressed with the inductive effect, attributed by the series-connected shorted stub element. This is a very attractive feature for practical applications. This interesting aspect of our design is also discussed with regard to stepped-impedance resonator (SIR) filtering circuits [21]. The additional insertion loss observed in the experiments can be explained by the conductor loss of the added narrow series-connected shorted stub elements [20].

V. Conclusion

A general-purpose circuit model is proposed for design and characterization of IDC-related structures using an accurate J-inverter network representation. This CAD-oriented model is derived from a newly developed numerical SOC technique, allowing frequency dispersion and other parasitic effects in the parameter extraction of a circuit layout from field calculations. In our study, this SOC technique is self-contained in a deterministic MoM algorithm. It is shown that the proposed model is useful for efficient high-frequency design and synthesis of IDC-related circuits. It is indicated in the analysis that the use of the static lumped-element concept may be valid for IDC parameters at low frequency, however, an extra precaution should be taken for high-frequency design when the IDC is involved. The proposed model is well validated by extensive theoretical and experimental studies conducted during this study. Two IDC bandpass filters are identified, designed, and measured. It is found that the predicted frequency responses are in excellent agreement with the measured results. In particular, interesting features of a new class of filters are discussed, which include the effective size reduction and suppression of harmonic resonance. These aspects are achieved through the introduction of a series-connected shorted stub element that is integrated into the line resonators.

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Lei Zhu (S'91–M'93) received the Bachelor degree and Master degree of engineering from the Nanjing Institute of Technology (now Southeast University), Nanjing, Jiangsu, China, in 1985 and 1988, respectively, and the Doctor Degree of Engineering from the University of Electro-Communications, Tokyo, Japan, in 1993.

From 1985 to 1989, he studied a variety of millimeter-wave passive/active circuits and leaky-wave antennas using a grooved nonradiative waveguide (GNRD). From 1989 to 1993, he conducted studies on the full-wave characterization of planar transmission lines and components for monolithic microwave integrated circuits (MMIC's). From 1993 to 1996, he was with the Matsushita-Kotobuki Electronics Industries, Ltd. Japan, as a Research Engineer, where he conducted research/development works in the design of linearly polarized (LP) and circularly polarized (CP) planar antennas/arrays with compact-size and high radiation gain/efficiency for applications in wireless communications. Since 1996, he has been with Ecole Polytechnique, University of Montréal, Montréal, P.Q., Canada, where he is currently a Research Associate. His current works/interests include the study of planar dual-mode bandpass filters, planar antenna elements/arrays, uniplanar passive/active circuits and antennas, as well as full-wave 3-D modeling techniques, numerical calibration (deembedding) procedures, and field-theory-based CAD techniques.

Dr. Zhu was awarded the Japanese Government (Monbusho) Graduate Fellowship (1989–1993), the First-Order Achievement Award in Science and Technology presented by the National Education Committee of China (1993), the Silver Award of Excellent Invention presented by the Matsushita-Kotobuki Electronics Industries Ltd., Japan (1996), and the 1997 Asia–Pacific Microwave Prize Award presented at the Asia–Pacific Microwave Conference, Hong Kong (1997).

Ke Wu (M'87–SM'92) was born in Liyang, Jiangsu Province, China. He received the B.Sc. degree with distinction in radio engineering from the Nanjing Institute of Technology (now Southeast University), Nanjing, China, in 1982, and the D.E.A. and Ph.D. degree with distinction in optics, optoelectronics, and microwave engineering from the Institut National Polytechnique de Grenoble (INPG), Grenoble, France, in 1984 and 1987, respectively.

He conducted research in the Laboratoire d'Electromagnetisme, Microondes et Optoelectronics (LEMO), Grenoble, France, prior to joining the Department of Electrical and Computer Engineering, University of Victoria, Victoria, B.C., Canada. He subsequently joined the Department of Electrical and Computer Engineering, Ecole Polytechnique de Montréal (Faculty of Engineering, University of Montréal), Montreal, Canada, as an Assistant Professor, and is currently a Full Professor. He held a 1995 Visiting Professorship in France (Telecom-Paris and INP-Grenoble), a 1996-1997 Visiting Professorship at the City University of Hong Kong, a 1999 Guest Professorship at the Swiss Federal Institute of Technology (ETH-Zürich), Zürich, Switzerland, as well as several short-term Visiting Professorships at other universities. He also holds an Honorary Visiting Professorship at the Southeast University, China. He is currently a Visiting Professor at the National University of Singapore. He has been the Head of the FCAR Research Group of Quebec, where he is involved with RF and millimeter-wave electronics, and the Acting Director of the Poly-Grames Research Center. He has authored or co-authored over 250 refereed journals and conference papers and several book chapters. His current research interests involve 3-D hybrid/monolithic planar and nonplanar integration techniques, active and passive circuits, antenna arrays, advanced field-theory-based CAD and modeling techniques, and development of low-cost RF and millimeter-wave transceivers. He is also interested in the modeling and design of microwave photonic circuits and systems. He was chairperson of the 1996 ANTEM Publicity Committee and vice-chairperson of the Technical Program Committee (TPC) for the 1997 Asia–Pacific Microwave Conference (APMC'97). He has served on the FCAR Grant Selection Committee (1993–1996, 1998–1999), and the TPC committee for the TELSIKS and ISRAMT. He has also served on the ISRAMT International Advisory Committee. He was the general co-chair of the 1999 SPIE International Symposium on Terahertz and Gigahertz Photonics, Denver, CO. He serves on the Editorial Review Board for *Microwave and Optical Technology Letters*.

Dr. Wu is a member of the Electromagnetics Academy. He has served on the Editorial or Review Boards of various technical journals, including the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION, and the IEEE MICROWAVE AND GUIDED WAVE LETTERS. He served on the 1996 IEEE Admission and Advancement (A&A) Committee and the Steering Committee for the 1997 joint IEEE APS/URSI International Symposium. He has also served as a TPC member for the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium. He received a URSI Young Scientist Award, the Institute of Electrical Engineers (IEE) Oliver Lodge Premium Award, the Asia–Pacific Microwave Prize Award, the University Research Award "Prix Poly 1873 pour l'Excellence en Recherche," presented by the Ecole Polytechnique on the occasion of its 125th anniversary, and the Urgel-Archambault Prize (the highest honor) in the Field of Physical Sciences, Mathematics and Engineering from the French-Canadian Association for the Advancement of Science (ACFAS).