Modeling and Design Aspects of Millimeter-Wave and Submillimeter-Wave Schottky Diode Varactor Frequency Multipliers

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***Abstract*—Design and optimization of Schottky varactor diode frequency multipliers for millimeter and submillimeter wavelengths are generally performed using harmonic balance techniques together with equivalent-circuit models. Using this approach, it is difficult to design and optimize the device and multiplier circuit simultaneously. The work presented in this paper avoids the need of equivalent circuits by integrating a numerical simulator for Schottky diodes into a circuit simulator. The good agreement between the calculated and published experimental data for the output power and conversion efficiency originates from the accurate physical model. The limiting effects of multiplier performance such as breakdown, forward conduction, or saturation velocity are discussed in view of the optimum circuit conditions for multiplier operation including bias point, input power, and loads at different harmonics. It is shown that the onset of forward or reverse current flow is responsible for the limitation in the conversion efficiency.**

***Index Terms*—Frequency multipliers, harmonic balance technique, numerical modeling, Schottky diode modeling, semiconductor simulation, submillimeter-wave multipliers.**

I. Introduction

VARACTOR frequency multipliers play a vital role in developing all-solid-state power sources at terahertz frequencies. The key points in the progress of the performance of Schottky varactor frequency multipliers have been the enhanced physical insight into and optimization of submillimeter-wave Schottky diode operation [1], the improvement in frequency multiplier analysis methods since the original work of Siegel and Kerr [2]–[5], and in physical analytical Schottky diode models [5]–[9], as well as numerical physical device models [4], [10]–[12]. The performance of active devices is defined not only by their inherent characteristics, but also by the embedding circuit. This coupling can be taken into account by including a numerical physical model into a circuit simulator [10], [11], [13]. The main problem in frequency varactor circuit design today is the inability to reproduce the experimental results without additional empirical parameters. Furthermore, the limitations of multiplier operation at high powers and/or high frequencies is not well understood. Finally, a predictive design and circuit analysis tool is still missing, which is essential for the design of integrated frequency multipliers.

The scope of this paper is to present a circuit analysis tool, which works without empirical parameters and is able to predict the required device and circuit parameters of a frequency multiplier. We focus on the circuit design and operation aspects of frequency multipliers for millimeter and submillimeter bands. As a design tool, we employ the harmonic balance method (HBM) together with a physics-based drift-diffusion (DD) numerical device simulator. Our simulator incorporates accurate boundary and interface conditions for high forward as well as reverse bias, including impact ionization, nonconstant recombination velocity, self-consistent incorporation of the tunnelling, and image-force effects [11]. The validation of the numerical simulator has been performed by comparison of simulated device and circuit characteristics with experimental results obtained for submillimeter-wave Schottky diodes fabricated at the Technical University Darmstadt (TUD), Darmstadt, Germany, and the University of Virginia (UVa), Charlottesville, and for a number of multiplier circuits published in the literature [4], [5].

The integration of numerical simulators for active devices into circuit simulators avoids the need of an equivalent-circuit model extraction. This new philosophy accounts for the device–circuit interaction and provides another degree of freedom to improve the performance of circuits because they can be designed from both a device and circuit point-of-view.

The simulation tool utilized in this paper and its implementation are presented in Section II. The validation of the tool is outlined in Section III, including a comparison of measured dc and RF performance characteristics with simulated values. In Section IV, an analysis of the performance of the frequency multipliers is presented together with an identification of the limiting mechanisms. Simulated results and a detailed discussion for the limiting mechanisms are provided in Section V, including breakdown and velocity saturation effects. Based on these results, the synthesis of an optimum doubler and tripler circuit is dealt with in Section VI. The optimization of the device parameters such as doping concentration and profile, layer thicknesses, etc. are omitted in this paper, but will be dealt with in a future paper. This paper concludes with a summary of the results.

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II. Simulation Tool Based on Physical Device Model

The HBM is the most common technique for the design of large-signal nonlinear microwave circuits. The HBM depends critically on the accuracy of the nonlinear element model employed in the analysis. This model must be valid for a wide range of frequencies, drive levels, and embedding impedances. The electrical and RF performance characteristics of submillimeter-wave Schottky diodes and frequency multiplier circuits investigated here are based on an accurate physical model, which combines DD current transport with thermionic and thermionic-field emission currents imposed at the Schottky contact.

The model for the carrier transport throughout the bulk is based on an extended one–dimensional (1-D) DD formulation [14]. 1-D simulations are adequate for the current flow under the Schottky metal, whereas two–dimensional (2-D) effects like current spreading can be accounted for by analytical formulas. The governing equations are Poisson's equation and continuity equations for electrons and holes as follows:

$$\nabla \cdot (\epsilon \nabla \varphi) = -q(N_d^+ - n + p) \tag{1}$$

$$\nabla \cdot J_n - q\frac{\partial n}{\partial t} = q(R - G) \tag{2}$$

$$J_n = -q\mu_n n \frac{d}{dx}(\varphi + \varphi_n) + kT\mu_n \frac{dn}{dx} \tag{3}$$

$$J_{\mathrm{tot}} = J_n + J_p + J_{\mathrm{disp}} = J_n + J_p + \epsilon\frac{\partial E}{\partial t} \tag{4}$$

$$\varphi_n = \frac{\chi}{q} + \frac{kT}{q}\ \ln\ N_c + \frac{q}{16\pi\epsilon x} \tag{5}$$

where φ is the electrostatic potential, ϵ is the permittivity, and n, p, N_d^+ are the electron concentration, hole concentration, and ionized impurity donor concentration, respectively. J_n, R, and G are, respectively, the electron conduction current density, the recombination rate modeled by the Schockley–Read–Hall recombination, and the generation rate currently restricted to impact ionization [14]. Further, μ_n, T, χ, and N_c represent the field-dependent electron mobility, temperature, affinity, and density of states in the conduction band, respectively. Similar equations also hold for holes. In (5), the conventional formulation of the position-dependent conduction band potential is augmented by the image force term. In contrast to previous publications, we do not introduce direct barrier lowering of the Schottky barrier height [15]. The simulation domain is divided into a nonuniform mesh of approximately 100 mesh points and the simulation time is of the order of minutes for one frequency point.

A. Boundary and Interface Conditions

Dirichlet boundary conditions are imposed at all metal contacts for Poisson's and carrier continuity [14]. In the present model, thermionic and thermionic-field transport at the Schottky barrier is introduced by means of an interface condition at the maximum of the barrier at the point x_m [16]. The position of the maximum is no longer at the metallurgical Schottky contact because of the influence of the bias-dependent image force lowering. The interface condition for the carrier transport is based on the assumption that the carrier distribution can be modeled by a displaced Maxwellian

$$J_n = qn(x_m)v_n - qn_0(x_m)v_r. \tag{6}$$

Here, $n(x_m)$ is the electron concentration at the maximum of the barrier and $n_0(x_m)$ represents a *quasi-equilibrium* density of electrons—the density that would be present at the top of the barrier if the electrons could be brought into thermal equilibrium without disturbing the potential distribution. v_r is the classical recombination velocity $v_r = \sqrt{(kT/2\pi m_e)}$. v_n is the recombination velocity after assuming a displaced Maxwellian shifted by a drift velocity v_{drift}

$$\begin{aligned} v_n &= v_r \cdot F(\xi) \\ &= v_r\Big[\exp(-\xi^2) - \sqrt{\pi}\xi\ \mathrm{erfc}\ (\xi)\Big] \end{aligned} \tag{7}$$

$$\xi = v_{\mathrm{drift}}\sqrt{\frac{m_e}{2kT}} \tag{8}$$

$$v_{\mathrm{drift}} = \frac{-J_n}{qn(x_m)}. \tag{9}$$

In this formulation, it has been assumed that the Schottky contact is located at $x = 0$. This interface condition prevents the unphysical effect of carrier accumulation at the interface [17], [18]. Between the point x_m and the metallurgical contact, the potential is assumed to vary linearly. No mesh points are required here for the calculation of the potential and current densities. Newton's method, Gummel's method, as well as a hybrid Newton/Gummel solution method are used for the solution of (1)–(5) with the interface conditions given in (6)–(9).

Tunnelling transport through the barrier is important for Schottky diodes with high doping in the epitaxial layer. In our model, the time-independent Schrödinger equation is solved for arbitrary piecewise-linear potential barriers using the transfer matrix approach [19], [20]. The grid defined for Poisson's equation is also used for Schrödinger's equation in the volume of the device, but a number of additional grid points are generated between x_m and the metallurgical contact in order to accurately resolve the shape of the conduction band in this region. The new expression for the current density can be represented by a simple integration [21] if the transmission coefficient $\mathrm{T}(E_n, E_t, V)$ is independent of the transversal component of the kinetic energy E_t and the distribution function is of Maxwellian type for the transversal component of the kinetic energy

$$J_n = \frac{A^*T}{k}\ \int_{E_{\min}}^{\infty}\ \mathrm{T}(E_n, V)\Big[f_s(E_n, V) - f_m(E_n)\Big]\ dE_n \tag{10}$$

$$E_{\min} = \max\ \Big\{E_{F_m},\ \min\ \{E_c\}\Big\} \tag{11}$$

where A^* is the Richardson constant, T is the lattice temperature (carrier heating is not considered), $\mathrm{T}(E_n, V)$ is the trans-

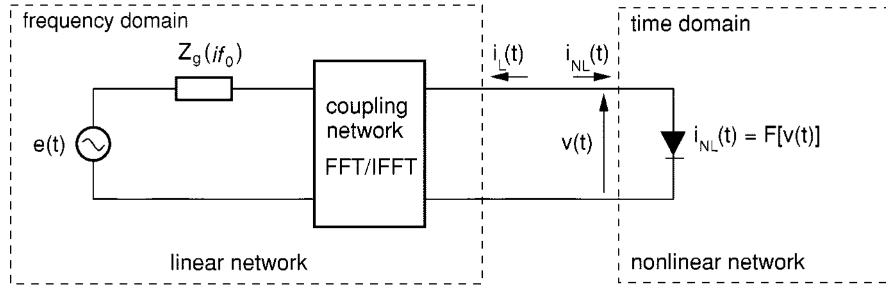


Fig. 1. Schematic drawing of the partitioning of the physical model and linear circuit for the harmonic balance calculations.

mission coefficient for the tunnelling transport, E_n is the energy for the normal component of the carrier velocity, f_s and f_m are the electron distributions in the semiconductor and metal, respectively, E_c stands for the conduction band in the semiconductor, and E_{F_m} is the Fermi level in the metal. We have assumed that f_s is a displaced Maxwellian distribution and f_m is a Maxwell–Boltzmann distribution. If tunnelling is not considered, this equation is similar to that proposed in [16].

B. Coupling the Physical Device Model with Circuit Simulation

Active devices are usually modeled as lumped equivalent circuits in commercial harmonic balance codes. There exist several algorithms for the HBM [2], [22], [23], some of which have been specifically designed to deal with physical device simulators [24]. The selected algorithm for this study is based on the solution of a system of nonlinear equations using a modified Newton's algorithm or Powell's algorithm, or the optimization of an error function by using the Levenberg–Marquardt (LM) algorithm [25]. The LM algorithm is utilized in the current simulations because of its efficiency.

In our case, the linear circuit is represented by the general coupling matrix, defined by $ABCD$ network parameters, and the generator impedance $Z_g(f)$, as can be depicted in Fig. 1.

The harmonic balance error equation for each harmonic i is then

$$\begin{aligned} F_i(V) &= 0 \\ &= V_i - E_i \cdot H_i - I_i(V) \cdot G_i, \qquad \text{for } i = 1, \cdots, N_{\text{harm}} \end{aligned} \tag{12}$$

where

$$H_i = \frac{1}{A_i - Z_g(if) \cdot C_i} \tag{13}$$

$$G_i = \frac{Z_g(if) \cdot D_i + B_i}{Z_g(if) \cdot C_i - A_i} \tag{14}$$

E_i are the phasors of the excitations, and I_i and V_i are the harmonic components of the current and voltage at the diode terminals. In the case of frequency multipliers, E_i is comprised of the dc voltage component and a single sinusoidal signal. The diode is always matched at the fundamental frequency. Six to twelve harmonics are considered in these simulations, and the impedances at the higher harmonics are set to 0.001 Ω for both the resistive and reactive components, if not otherwise specified.

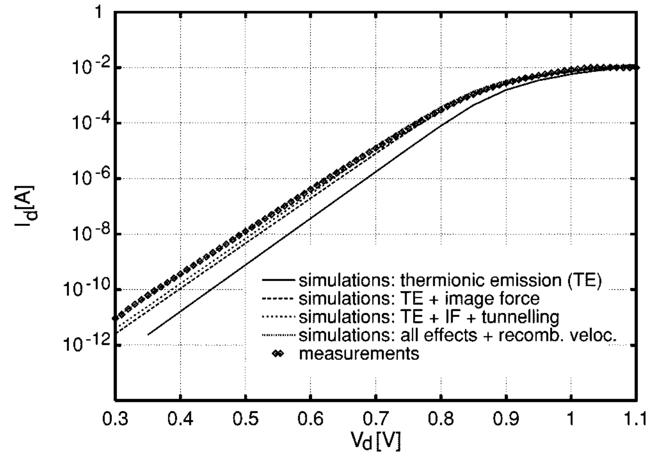


Fig. 2. Measured current voltage characteristic of a varactor Schottky diode compared to simulated values for the diode D1038 from TUD. The diode parameters are indicated in Table I.

All the parasitic elements of the diode are absorbed in the embedding network and included in the impedance seen by the junction at the different frequencies involved in the multiplier operation.

III. Validation of the Physical Model

The physical model has been validated with measurements for a large number of diodes in the doping range of $N_{D,\text{epi}} = 3 \cdot 10^{16}/\text{cm}^3 \sim 3 \cdot 10^{17}/\text{cm}^3$, different epitaxial layer thicknesses and various diode diameters ranging from 1 μm ~20 μm. The simulated current voltage characteristic for all diodes agree excellently with the respective measurements. An example is given in Fig. 2 for the diode D1038. The parameters of all the diodes analyzed in this paper are provided in Table I.

The contribution of the individual components to the total diode current is indicated in Fig. 2. The simulated capacitance voltage characteristic is also in excellent agreement with the measured values, as demonstrated in Fig. 3. The simulation is extended up to the breakdown voltage, where the junction capacitance is known to increase rapidly with reverse voltage [26].

The RF performance of the simulation tool has been discussed in [12]. We have performed simulations for two frequency multipliers published in the literature [4], [5]. In the simulations, we do not use any fitting parameters. In all simulations, a barrier height for the Pt Schottky contact of $\varphi_{b0} = 0.99$ eV is assumed.

The output power and efficiency versus the input power have been plotted in Fig. 4 for a frequency doubler (2 × 100 GHz)

TABLE I
SCHOTTKY DIODE PARAMETERS FOR DEVICES FROM TUD AND UVa

Diode	Epitaxial Layer		$V_{bd,DC}$ (V)
	doping (cm^{-3})	length (μm)	
D734	10^{17}	0.350	-10
D1038	3×10^{17}	0.560	-8
UVa 6P4	3.5×10^{16}	1.0	-20 [4]
UVa 2T2	1.0×10^{17}	0.60	-11 [33]
for D734/D1038	substrate doping: $2 \times 10^{18} cm^{-3}$		
	length: 80-100 μm		

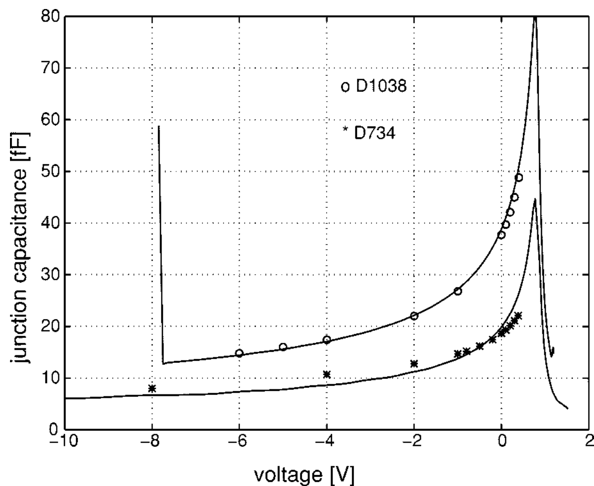
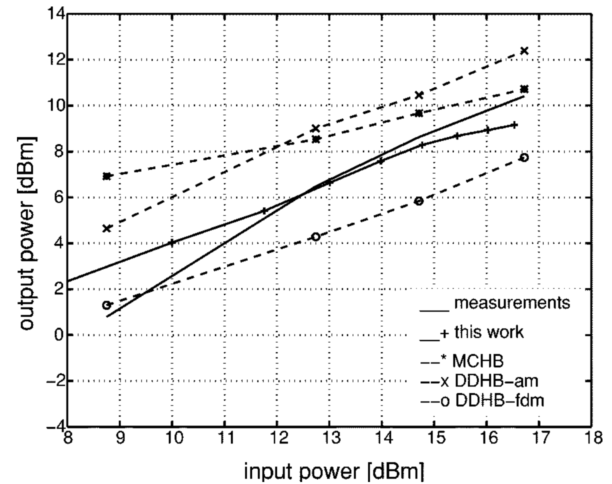
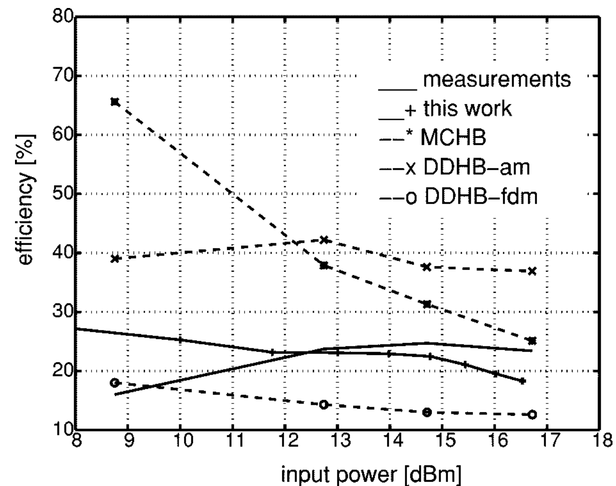


Fig. 3. Comparison between the measured (symbols) and calculated (solid lines) capacitance voltage characteristic for two diodes from the TUD D1038 and D734. The diode parameters are indicated in Table I.



(a)



(b)

Fig. 4. (a) Calculated and measured output power and (b) conversion efficiency as a function of the input power for a frequency doubler at $f_0 = 100$ GHz [4]. The solid line with symbols "+" denotes the results from our model, the solid line shows the experimental results from [4], and the dashed lines represent calculated results from [4].

utilizing a UVa 6P4 Schottky varactor. The results have been taken from [4] with additional simulations achieved with our model (solid line with "+" symbols). The techniques used in Fig. 4 are indicated as: 1) MCHB: self-consistent ensemble Monte Carlo harmonic balance simulator; 2) DDHB-fdm: drift-diffusion harmonic balance simulator with *field-dependent mobility*; and 3) DDHB-am: drift-diffusion harmonic balance with constant *average mobility*. All simulators overestimate the output power [see Fig. 4(a)] and the efficiency [see Fig. 4(b)] of the doubler at $P_{\rm in} \leq 10$ dBm. Results from our model agree well above $P_{\rm in} \geq 11$ dBm and reproduce the measured power slope. The bias voltage was $V_b = -10$ V, and the loads at harmonic frequencies were set to $Z_g(nf_0) = (0 + j0)\ \Omega$ for $n > 2$, while at the fundamental frequency, the diode was matched. The load impedance at the output $Z_g(2f_0)$ was optimized for maximum output power for each input power and obeys a value of $Z_g(2f_0) \approx (70 + j200)\Omega$ at an input power $P_{\rm in} = 14$ dBm. The unrealistic simulated results at low input powers originate from the perfect match of the diode at each power level in contrast to the experimental setup, where the loads have been optimized for high-power levels.

This is emphasized in Fig. 4(b), which shows that the results from the Monte Carlo code predict efficiencies close to the theoretical limit at low input power levels, whereas the measured efficiency is low and increases with power level. In our simulations, we have used the geometrical area and it is outlined below that our results would still improve when an effective diode area would have been employed.

We have also compared our simulations with the measured data for a frequency multiplier using a similar diode at $f_0 = 80$ GHz [5], illustrated in Fig. 5. At the output, the balanced diode configuration has been simulated as a direct parallel connection of two identical diodes. The agreement with measured data is very good. Simulations of the same arrangement at $f_0 = 160$ GHz also agree well at high-input power levels. Although the simulations presented in Figs. 4 and 5 have been performed at different frequencies and with different circuit structures, we achieve very good agreement at large power levels, which demonstrates the capabilities of the simulation tool.

IV. ANALYSIS OF VARACTOR-BASED MULTIPLIER CIRCUITS

The results from a successful circuit analysis of frequency multipliers should predict the following parameters determining

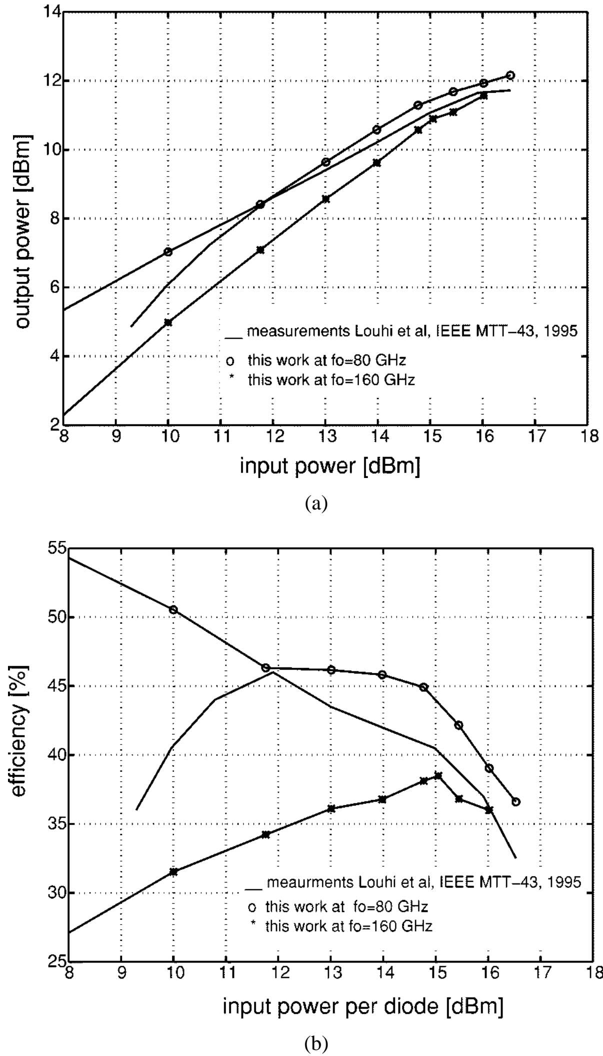


Fig. 5. (a) Calculated and measured output power and (b) conversion efficiency as a function of the input power for a frequency doubler at $f_0 = 80$ GHz [5]. The symbols "o" "*" denote the results from our model at $f_0 = 80$ GHz and $f_0 = 160$ GHz, respectively, and the solid line shows the experimental results from [5].

the multiplier performance for a given diode structure: output power $P_{\rm out}$, conversion efficiency η, embedding impedances at the fundamental, output, and idler frequencies at the diode terminals, bias voltage $V_{\rm bias}$, and load impedances at the remaining harmonics. All conventional multiplier design methods are based on an equivalent circuit of the Schottky diode presented in Fig. 6(a) [1], [2], [27]. However, this simple model cannot explain the decrease in conversion efficiency beyond a certain input power level, which has been frequently observed in experimental results. Improved intrinsic diode models have to be utilized in this case, as shown in Fig. 6(b) and (c), which describe the physical behavior of the device with increasing accuracy. As has been pointed out by Grajal *et al.* [12], at low-input powers equivalent-circuit models, including electron velocity saturation phenomena [see Fig. 6(b)] are sufficient to accurately predict the multiplier performance. However, at high-power levels and near the maximum of the conversion efficiency, only accurate physical models [see

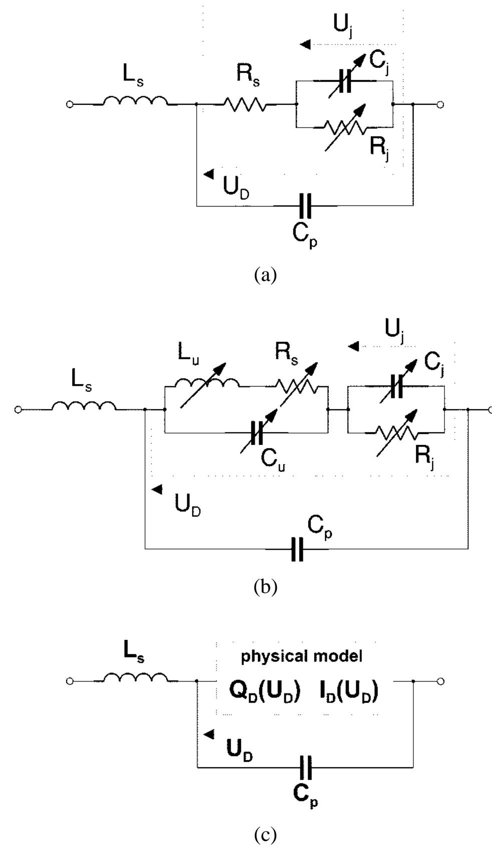


Fig. 6. Equivalent circuits for different Schottky diode varactor models. (a) Constant series resistance model. (b) Variable series resistance model. (c) Proposed physical model including all effects.

Fig. 6(c)] provide reasonable prediction of the multiplier performance.

In Fig. 6(a) and (b), the Schottky junction is modeled by a parallel connection of a voltage-dependent nonlinear capacitance and resistance. The series resistance due to the undepleted region in the semiconductor becomes a nonlinear function of the diode current density at increased current densities [see Fig. 6(b)]. The nonlinear current dependent series resistance has been considered responsible for the decrease in the conversion efficiency at high-power levels [1], [5], [27]. It has been argued that the displacement current becomes comparable to the maximum current in the material at high operating frequencies. An empirical current-dependent series resistance has been introduced in order to fit the measured results, according to Fig. 6(b). It has to be emphasized that the above analysis did not include breakdown effects and its impact on the RF operation of the frequency multiplier. Furthermore, the series resistance increases when the current density in the diode approaches the maximum current density

$$J_{\rm max} = qN_D v_{\rm max} > J_{\rm disp} = \frac{\partial Q}{\partial t} = \frac{\partial (qN_D w)}{\partial t} \tag{15}$$

with $J_{\rm disp}$ being the displacement current. Dividing both sides by the available number of electrons yields the maximum velocity with which the edge of the depletion region can move

$$v_{\rm max} > \frac{\partial w}{\partial t} \tag{16}$$

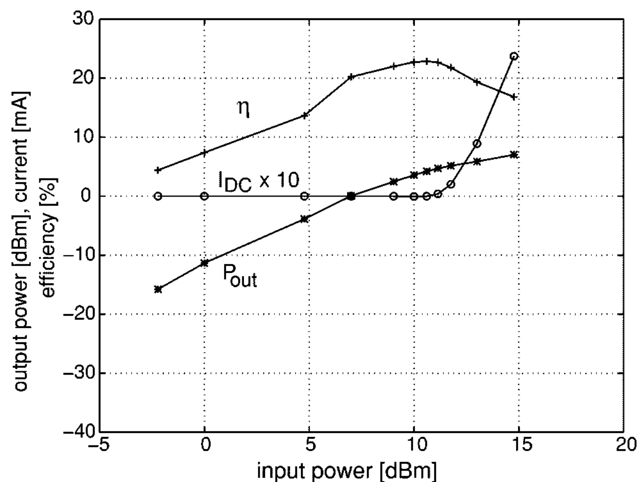


Fig. 7. Efficiency, output power, and dc current at $V_{\rm bias} = -3$ V for the D734 varactor Schottky diode.

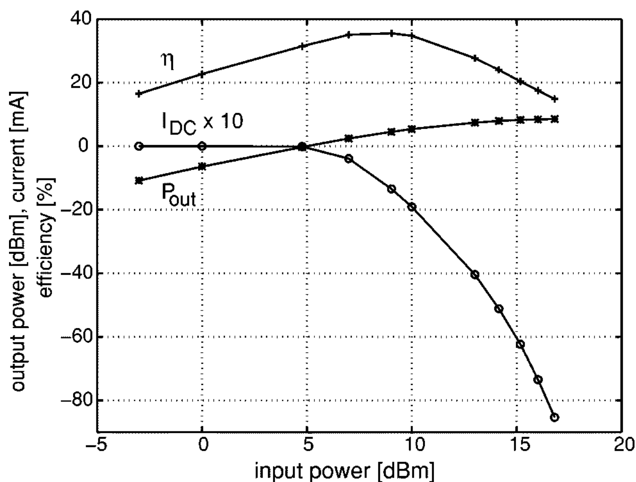


Fig. 8. Efficiency, output power, and dc current at $V_{\rm bias} = -7$ V for the D734 varactor Schottky diode.

where w is the width of the depletion region. Hence, (16) is equivalent to the argument that the displacement current density must be less than the maximum current density in the semiconductor in the undepleted region $J_{\rm disp} < J_{\rm max}$. It cannot be equal to the maximum current density because this would assume a zero conduction current in the depletion region.

The equivalent-circuit models require a separation of physical effects into individual equivalent-circuit elements, an extraction of the equivalent-circuit element values from measurements distinct from the operating conditions, and an identification of equivalent-circuit elements with combined effects at high powers and high frequencies, which is very difficult to achieve.

Therefore, a physical model is proposed, which is based on results from the previous section. Such an approach enables us to concurrently optimize the device electrical and geometrical parameters together with attainable output power, conversion efficiency, and the required loads at the specific harmonics.

Although we agree that the current saturation mechanism becomes important at very high frequencies, typically above 300-GHz fundamental frequency, but it has only a marginal effect on efficiency decrease at frequencies below 200 GHz, which were considered in [1]. The diode 6P4 shows velocity saturation effects only because of its very low doping concentration in the epitaxial layer. We suggest that the limitation in varactor operation is due to the initiation of varistor operation with a concurrent onset of dc current flow at either end of the current–voltage characteristic. For example, we have used the Schottky varactor diode D734 from TUD, similar to the diode 2T2 from UVa for simulations of frequency doublers and triplers with our simulation tool. It can be inferred from Figs. 7 and 8 that the maximum conversion efficiency coincides with the onset of the dc current through the diode. In Fig. 7, the dc current is positive due to forward conduction, as can be depicted from the time-domain waveforms given in Fig. 9. In contrast to this, the dc current component in Fig. 8 is negative, originating from impact ionization when the total voltage exceed the breakdown voltage in the device, as indicated in Fig. 10. Independently of dc current polarity, the maximum of the

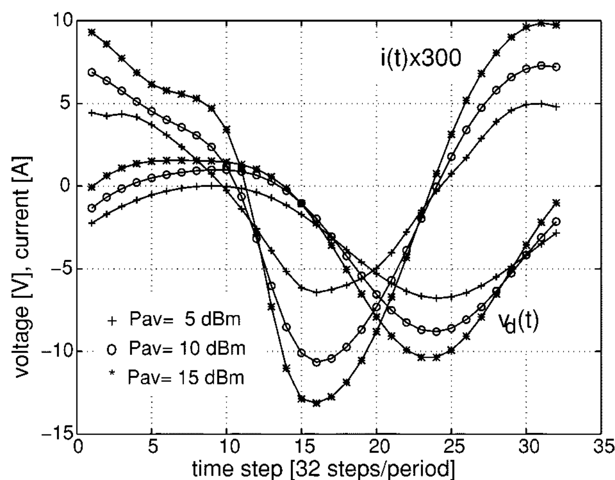


Fig. 9. $v_D(t)$ and $i_D(t)$ versus time for $V_{\rm bias} = -3$ V for the D734 varactor Schottky diode. Operating frequency is $f_0 = 50$ GHz. The time scale is 32 points per period.

conversion efficiency coincides with the onset of current flow, whereas the output power further increases with increasing input power. The increase in output power is due to the mixed varactor/varistor operation and the decrease in the efficiency at high-power levels originates from the conversion of the RF signal into dc power. The dc power is then delivered to the circuit or dissipated in the device, respectively. It is important to observe that the input power level for maximum efficiency does not coincide with the power level for maximum output power. Fig. 11 shows that, at low input power levels, the efficiencies for the bias voltage $V_{\rm bias} = -5$ V and $V_{\rm bias} = -7$ V are nearly equal. The reason is that the capacitance is nearly constant for voltages lower than -7 V. Hence, no effective capacitance modulation takes place for the negative semicycles. The slight increase in the capacitance for $V_{\rm bias} = -5$ V has an effect on the tripler performance, but the doubler circuit is insensitive to this small variation. Hence, the results for the efficiency of the doubler circuit are very similar for these two bias conditions. Similar results have been obtained for the the tripler circuit, as indicated in Fig. 12.

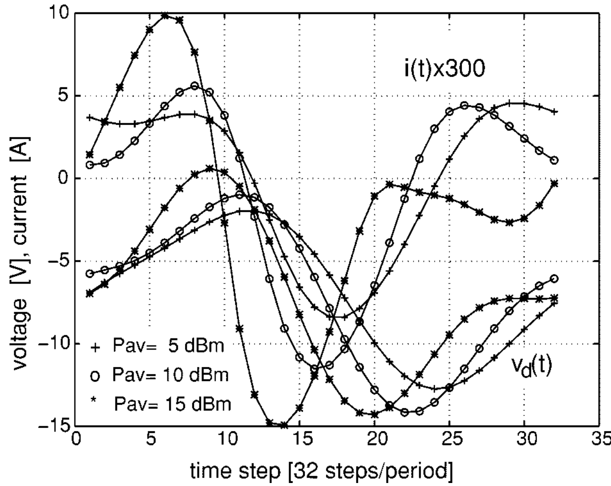


Fig. 10. $v_D(t)$ and $i_D(t)$ versus time for $V_{\rm bias} = -7$ V for the D734 varactor Schottky diode. Operating frequency is $f_0 = 50$ GHz. The time scale is 32 points per period.

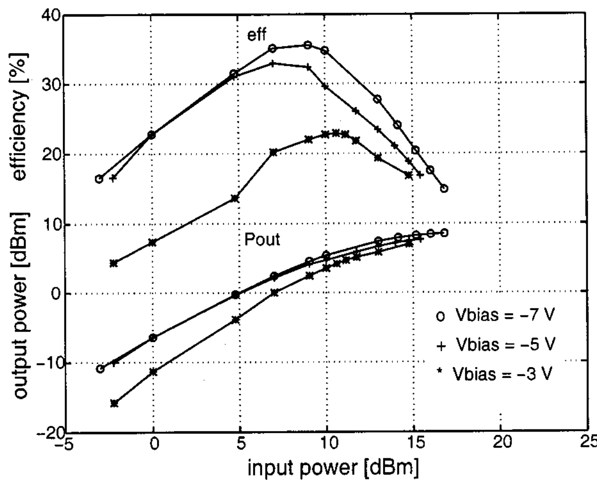


Fig. 11. Frequency-doubler conversion efficiencies and output powers with D734 diode for three different bias conditions $V_{\rm bias} = -3$ V, $V_{\rm bias} = -5$ V, $V_{\rm bias} = -7$ V. Operating frequency is $f_0 = 50$ GHz.

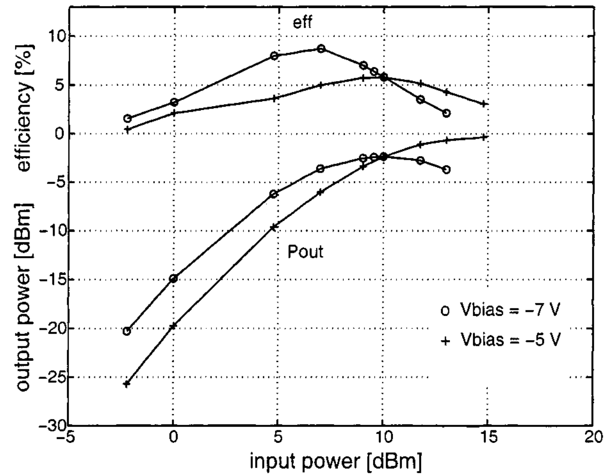


Fig. 12. Frequency-tripler conversion efficiencies and output powers with D734 diode for two different bias conditions $V_{\rm bias} = -5$ V and $V_{\rm bias} = -7$ V. Operating frequency is $f_0 = 50$ GHz.

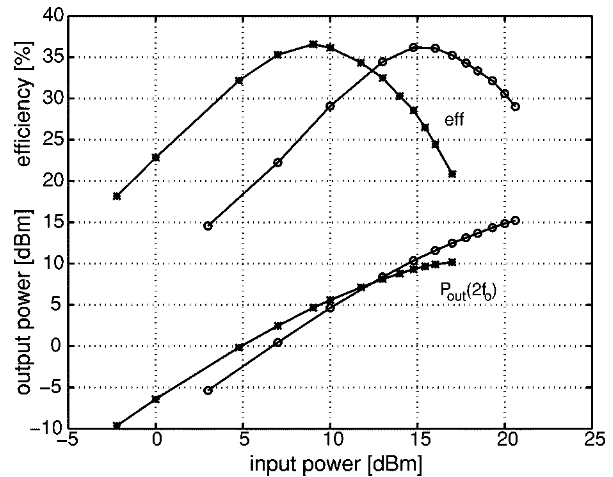


Fig. 13. Calculated output power and conversion efficiency as a function of the input power for two TUD D734 Schottky varactors. The bias voltage is $V_{\rm bias} = -5$ V and optimum loads are chosen at the second and third harmonic. The fundamental frequency is $f_0 = 50$ GHz. The symbols "*" are for a diode diameter of 6.7 μm and the symbols "o" stand for results with a diode diameter of 13.4 μm.

V. Mechanisms and Parameters Limiting Multiplier Performance

There exist three major mechanisms responsible for the limitation of the output power and conversion efficiency: forward conduction, reverse breakdown, velocity saturation. These mechanisms have a direct impact on the muliplier circuit performance such as the bias point, the maximum voltage swing, embedding impedances, and the load impedances at the higher harmonics. The forward conduction mechanism is independent of frequency and restricts the positive voltage swing of the sinusoidal signal at the device terminals. The reverse breakdown mechanism is frequency dependent and limits the signal excursion in the reverse direction. It can also lead to current saturation in a well-designed diode by the increased current flow due to impact ionization.

A. Impact of the Bias Point and the Series Resistance on Multiplier Performance

It should be observed in Fig. 11 that the output power levels for all bias conditions ultimately converge to similar values, however, with high dc currents. Operating the diodes at high dc currents is not desirable due to reliability and burnout problems associated with high-current high-voltage operation. Therefore, the bias point for maximum conversion efficiency for a particular diode is the point with maximum RF amplitude excursion without dc current generation, as $V_{\rm bias;opt} = (V_D - V_{\rm bd;RF})/2$, where V_D is the diffusion voltage and $V_{\rm bd;RF} \approx -14$ V is the RF breakdown voltage for D734. The maximum conversion efficiency can also be shifted with regards to the input power by utilizing Schottky diodes with different areas. Fig. 13 illustrates calculated results for two Schottky varactor diodes D734 with different anode diameters. The maximum conversion efficiency is shifted toward lower values of the input power when

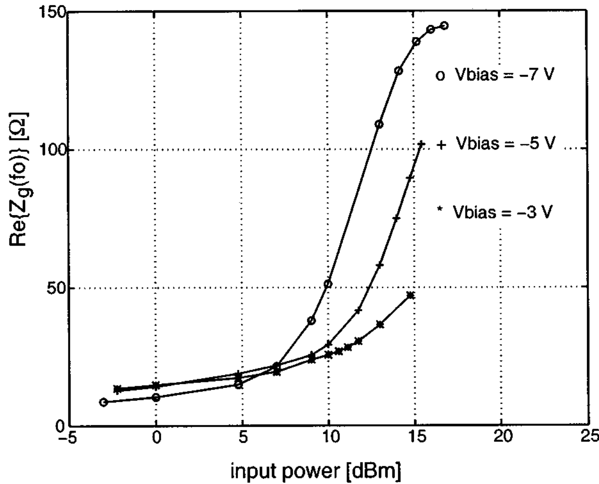


Fig. 14. Variation of the real part of the diode impedance calculated from the physical model as a function of the input power at bias voltages $V_{\rm bias} = -3$ V, -5 V, -7 V for the diode from Fig. 7.

the diode area is decreased. The demand for maximum conversion efficiency at a prescribed input or output power uniquely determines the diode area. The optimum value is a function of the doping concentration, frequency, and desired output power. Highest output powers are achieved with large anode diameters because the output power and displacement current both scale with the area. Whenever sufficient power is available to pump the diode up to maximum conversion efficiency and an appropriate matching is realizable, a large-area diode will provide improved output power performance.

As demonstrated in [1] from DD physical calculations, the real part of the diode impedance rises strongly with input power level. We can reproduce this increase, which is illustrated in Fig. 14 for the diode used in Figs. 7–10. Note that, in the case of reverse breakdown, the real part of the diode impedance increases dramatically by a factor of more than 12. Such large changes in the series resistance cannot be solely attributed to lowering of the mobility. One possible reason is that, at reverse breakdown, the total diode resistance never reaches the zero-bias series resistance values due to the high fields in the space–charge region. The interpretation of the numerical results in Fig. 14 in terms of equivalent-circuit elements is not simple and the identification of the individual mechanisms with particular equivalent-circuit elements is almost impossible in the case of breakdown. In this case, the physical model should be used for the accurate characterization of the diode.

B. Impact of Breakdown Effect on Different Operating Conditions

As pointed out above, the generation of charges due to impact ionization plays a vital role in multiplier performance. The model for the generation of carriers due to avalanche multiplication is based on the following:

$$G = \frac{1}{q}\Big(\alpha_n|\overline{J_n}| + \alpha_p|\overline{J_p}|\Big) \tag{17}$$

$$\alpha_{n,p} = A_{n,p}\exp\left[-\left(\frac{E_{\rm crit}}{|E_{n,p}|}\right)^{\beta_{n,p}}\right] \tag{18}$$

where α_n and α_p stand for the ionization coefficients for electrons and holes, J_n and J_p are the electron and hole current densities, $\beta_{n,p}$ and $A_{n,p}$ indicate empirical parameters for the calculation of the ionization coefficients, $E_{n,p}$ is the electric field in the space–charge region, and $E_{\rm crit}$ denotes the critical field for charge generation, respectively. Some authors have pointed out that the RF breakdown voltage is frequency dependent and can be significantly different from the dc breakdown voltage [30], [31]. This has also been observed in our simulations. One possible explanation for the frequency dependence is that, at high frequencies, the conditions for avalanche are achieved for only a short period of time and, therefore, the carriers in the material may not gain sufficient energy to ionize other carriers. Additionally, the carrier density does not follow the field change in unison because the carrier generation G also depends on the number of carriers already present, which is described through (2). This happens although the impact ionization rates $\alpha_{n,p}$ in (17) follow the field change nearly instantaneously.

C. Velocity Saturation Mechanism at High Frequencies

High-frequency operation of frequency multipliers is limited by the velocity saturation effect. It has been outlined in [32] that the current saturation mechanism should not occur for well-designed diodes at all operating frequencies. This can be achieved by choosing a sufficiently high doping density in the device $N_D \geq J_{\rm disp}/qv_{\rm max}$. The limited carrier velocity in materials such as GaAs determines the upper bound for the rate of change of the space–charge width. Ultimately, the signal frequency becomes larger than the maximum electron velocity (for electrons in GaAs $v_{\rm max} \approx 2.8 \cdot 10^7$ cm/s) and the space–charge cannot be modulated. This is the case for the 6P4 diode at frequencies around 100 GHz because of the low doping concentration. At such high frequencies, other frequency-multiplying mechanisms or different materials like InAs or InSb must be considered. It is shown in Fig. 15 that the edge of the depletion region can follow the voltage waveform at 100 GHz, but cannot follow the voltage waveform at 700 GHz. In Fig. 15, the Schottky diode contact is located on the right-hand side of the diagram. It can be seen that the value for maximum depletion width $w_{\rm max} \approx 80.55$ μm remains nearly constant for the three frequencies, whereas the difference between the minimum and maximum value of the depletion width Δw decreases strongly with increasing frequencies. The decreased Δw leads to a smaller modulation of the space–charge region during one period of the exciting signal, which, in turn, leads to a smaller capacitance modulation. This asymmetry is probably due to the finite time required to empty the space–charge region, while the space–charge region can be rapidly filled with mobile charges. The transition between the space–charge region and the undepleted region is abrupt at 100 GHz and slopes with increasing frequencies.

The design procedure at high frequencies differs from that at low frequencies because the breakdown voltage is no longer the limiting factor. Hence, maximum output power and conversion efficiency is achieved when the current density is smaller than the saturation current [see (15)]. This determines the optimum doping. The epi-layer thickness is then chosen for minimum

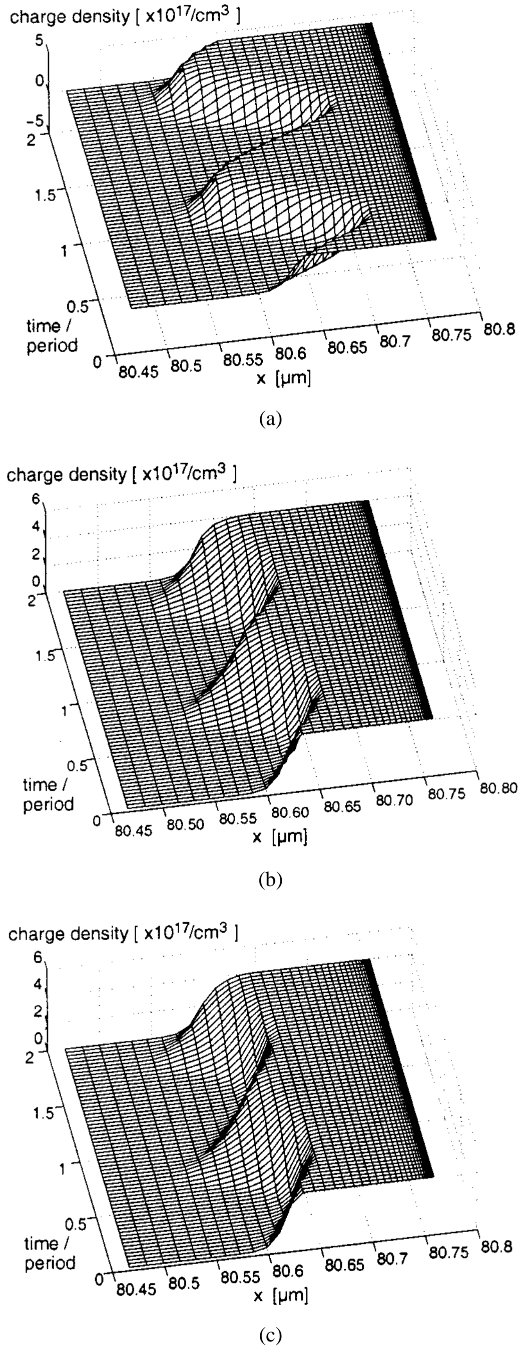


Fig. 15. Variation of the edge of the depletion region with applied RF voltage at (a) signal frequency of 100 GHz, (b) signal frequency of 500 GHz, and (c) signal frequency of 700 GHz. The epi-layer doping is $N_{\rm epi} = 4 \cdot 10^{17}$/cm^3, the epi-layer thickness is $t_{\rm epi} = 560$ nm, diode diameter is 5 μm.

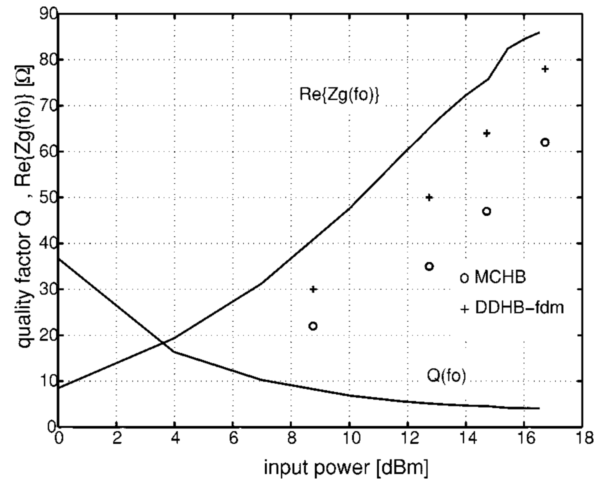


Fig. 16. Quality factor Q and the real part of the diode impedance $\Re\{Z_g(f_0)\}$ as a function of input power for the diode 6P4. The operating conditions are the same as in Fig. 4.

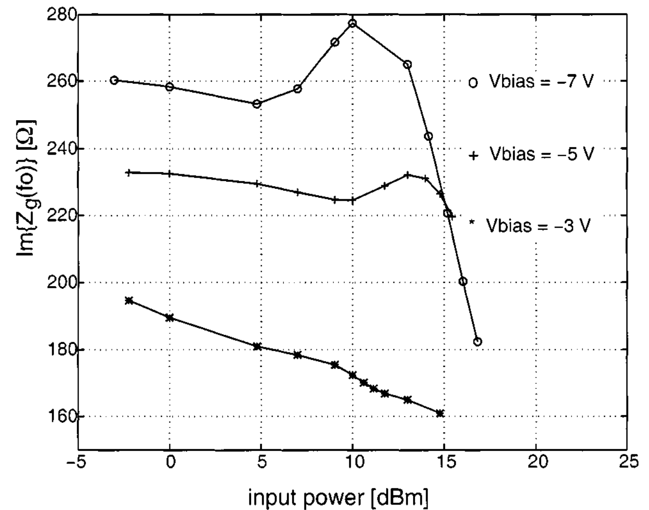


Fig. 17. Imaginary part of the diode embedding impedance $\Im\{Z_g(f_0)\}$ as a function of input power for the diode D734 for three different bias points.

series resistance. The circuit is operated at larger capacitance values (lower reverse bias).

VI. Synthesis of Optimum Frequency Multipliers

It has been demonstrated in [12] that the multiplier circuit is more sensitive to changes in the embedding impedances at low-input power levels as compared to high-input power levels. This is independent of the diode considered in the simulations. The sensitivity can be defined in terms of a quality factor at the respective frequency

$$Q(f_0) = \frac{\Im\Big\{Z_g(f_0)\Big\}}{\Re\Big\{Z_g(f_0)\Big\}}. \tag{19}$$

The real part of the diode impedance vary with input power and frequency, whereas the imaginary part varies essentially only as a function of frequency. When the quality factor Q is large, the circuit is more sensitive to changes in frequency.

The quality factor Q and the real part of the diode input impedance versus input power are illustrated in Fig. 16 for the 6P4 diode. The imaginary part has been omitted because it changes by less than 10% for all power levels. It can be seen that $Q(f_0) \approx 35, \cdots, 13$ at low-power levels below $P_{\rm in} < 6$ dBm. For high-input power levels, the variation of the load is weak ($Q \approx 4$) and all simulations show a strong increase of $\Re\{Z_g(f_0)\}$ in accordance with [1], [5].

TABLE II
MAXIMUM CONVERSION EFFICIENCY OF A FREQUENCY DOUBLER AND TRIPLER FOR $P_{\rm av} = 7$ dBm AT THREE BIAS POINTS. THE DIODE USED IN THE ANALYSIS IS D734. THE FUNDAMENTAL FREQUENCY IS 50 GHz. FOR THE DOUBLER, THE LOAD IMPEDANCE AT THE THIRD HARMONIC IS $Z_g(3f_0) = 0 + \jmath 0$. FOR THE TRIPLER, THE LOAD IMPEDANCES AT THE SECOND AND FOURTH HARMONIC ARE $Z_g(2f_0) = (0 + \jmath 0)\Omega$, $Z_g(4f_0) = (0 + \jmath 0)\Omega$

multiplier	V_{bias} (V)	η (%)	$Z_g(2f_0)$ Ω	$Z_g(f_0)$ Ω
doubler	-3	22.5	$25 + j100$	$26.9 + j185.3$
	-5	31.2	$25 + j125$	$22.0 + j226.8$
	-7	37.2	$25 + j150$	$23.0 + j275.5$
			$Z_g(3f_0)$ Ω	$Z_g(f_0)$ Ω
tripler	-3	2.8	$19 + j70$	$20.1 + j173.6$
	-5	5.0	$17 + j80$	$16.3 + j213.5$
	-7	8.7	$12 + j90$	$17.2 + j258.2$

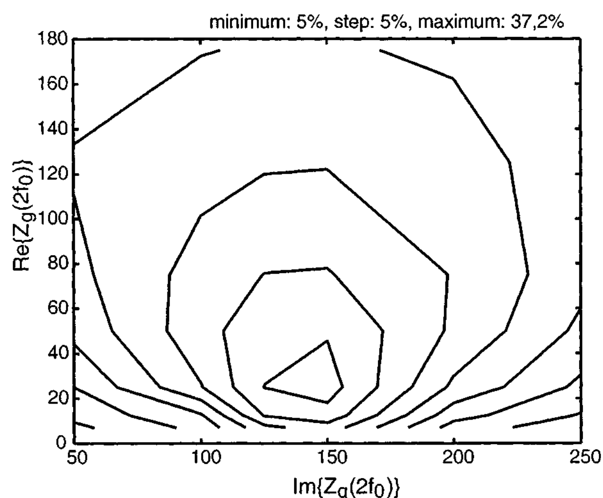


Fig. 18. Sensitivity of the efficiency to $Z_g(2f_0)$ for $V_{\rm bias} = -7$ V and $P_{\rm av} = 7$ dBm.

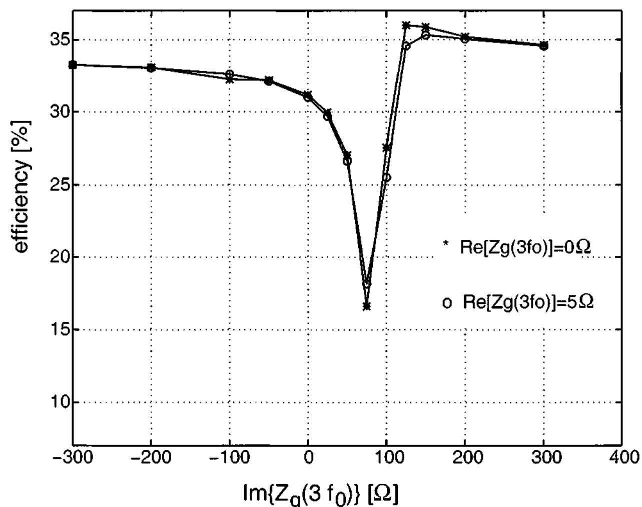


Fig. 19. Sensitivity of the efficiency of the freqeuncy doubler to $Z_g(3f_0)$ for $V_{\rm bias} = -5$ V and $P_{\rm av} = 7$ dBm.

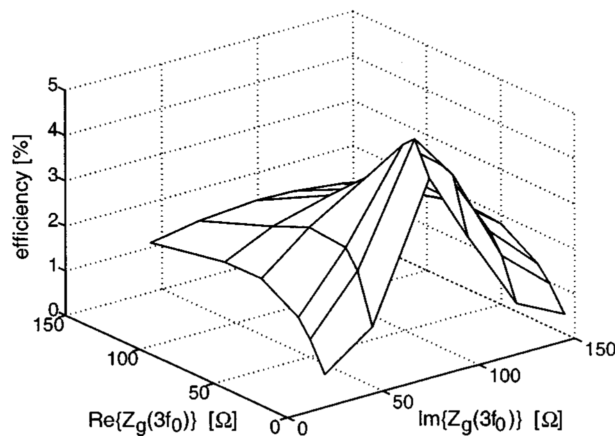


Fig. 20. Sensitivity of the conversion efficiency of a frequency tripler to $Z_g(3f_0)$ for $V_{\rm bias} = -5$ V and $P_{\rm av} = 7$ dBm.

The imaginary part of the embedding impedance for the diode D734 is shown in Fig. 17. It can be inferred from Fig. 17 that the imaginary part changes little with increasing input power, up to a value where a substantial breakdown current is generated in the diode, which increases the junction capacitance in accordance with Fig. 3. Table II summarizes the results obtained for the analysis of a frequency doubler and frequency tripler, respectively, using the diode D734 at a fundamental frequency of $f_0 = 50$ GHz. It can be inferred from the tables that the optimum impedance for the frequency tripler is slightly lower as compared to the frequency doubler.

Once the optimum conditions for a multiplier have been determined, the tuning capabilities of the multiplier circuit are investigated for the extraction of realizable tuning elements. Fig. 18 shows the conversion efficiency as a function of the circuit impedance at the second harmonic $Z_g(2f_0)$ for an input power level of 7 dBm, which coincides with the maximum of the conversion efficiency at a bias voltage of $V_{\rm bias} = -7$ V. It can be deduced from Fig. 18 that for $Z_g(2f_0)$ different from the optimum load $Z_{g-{\rm opt}}(2f_0)$, the efficiency and output power drop rapidly to very low values. Furthermore, it can be seen that decreasing the optimum value for $\Re\{Z_g(2f_0)\}$ has a stronger effect than increasing it.

Exploiting the resonance between a pure reactance and the effective device capacitance at the third harmonic, the efficiency can be further increased by ≈5% according to Fig. 19 ($V_{\rm bias} = -5$ V, $Z_g(2f_0) = (25 + \jmath 125)$ Ω, and $P_{\rm av} = 7$ dBm). This efficiency improvement is sustained even for slightly lossy realizations of the circuit.

Fig. 20 shows the conversion efficiency for the frequency tripler as a function of the load at the third harmonic $Z_g(3f_0)$. The loads at the second and fourth harmonic are chosen short circuits in this figure and the bias voltage is $V_{\rm bias} = -5$ V. Similarly to the results obtained for the frequency doubler, the optimum operation is sensitive to variation of the embedding impedance for an impedance different from the optimum load impedance $Z_{g-{\rm opt}}(3f_0)$. The selection of the impedance of the idler is crucial in frequency triplers. This point is exemplified in Fig. 21. The simulations have been performed with $V_{\rm bias} = -5$ V and $Z_g(3f_0) = Z_{g-{\rm opt}}(3f_0)$. The results obtained from this analysis ($\eta_{\rm opt} \approx 15\%$) suggest that the load at the second and fourth harmonic can be treated

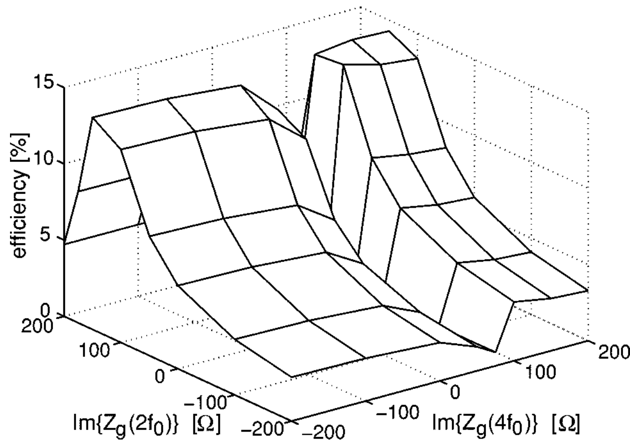


Fig. 21. Sensitivity of the conversion efficiency of a frequency tripler to the idler circuit $Z_g(2f_0)$ and to the load at the higher harmonic $Z_g(4f_0)$ for $V_{\rm bias} = -5$ V and $P_{\rm av} = 7$ dBm.

independently and the impedance value at the idler frequency is more important than the load at the fourth harmonic. The resonance for the idler frequency requires inductive loads and, in the vicinity of the maximum efficiency, the sensitivity of the efficiency to variation in the impedance values is higher for increasing values of $\Im\{Z_g(2f_0)\}$.

In frequency doublers and triplers, the optimum load at the third and fourth harmonic, respectively, does not depend on the power level. A load different from short circuit at even higher harmonics has only a marginal effect on the multiplier performance.

VII. Conclusions

The degree of freedom that arises as a consequence of the coupling of a numerical model for Schottky diodes and a harmonic balance circuit simulator has enabled us to study the different operation regimes and the physical limitations of the frequency multiplier performances. It has also demonstrated its usefulness to design multiplers from the circuit point-of-view: bias, input power, and loads at different harmonics.

We have obtained good agreement between published experimental results and our calculations for device and multiplier characteristics operating at frequencies up to 320 GHz with our enhanced DD model coupled to a harmonic balance simulator.

We have demonstrated that, at low input power levels, the operation of the multiplier is mainly determined by the embedding circuit and the choice for the dc operating point of the diode. The discrepancies observed in many simulation between the measured and calculated results can be explained by mismatching effects and do not originate from device physics. In contrast, at high-power levels, the embedding circuit exhibits only minor contribution to the overall performance of the multiplier and impact ionization in the device is responsible for output power saturation and conversion efficiency decrease at high output powers.

It has been demonstrated that the onset of the dc current is responsible for the decrease of the conversion efficiency at high-power levels. The impact of the breakdown effects, the velocity saturation, and the forward conduction on frequency multiplier performance has been discussed in detail. Simulated results suggest that the output power approaches similar values at high input power independent of the choice of the bias point. At these power levels, the embedding circuit is determined by the increase of the real part of the input impedance. It was also found that an appropriate load at the high harmonics could improve the efficiency independently from the power level.

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