Miniaturized Artificial-Transmission-Line Monolithic Millimeter-Wave Frequency Doubler

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***Abstract*—Millimeter-wave signals are typically generated by frequency multiplication in modern single-chip or multichip module (MCM) systems. Consequently, the multiplication efficiency, spurious rejection, and size of the frequency multiplier ultimately limit the integration level and cost of these systems. This paper points to the size reduction of millimeter-wave frequency doublers by evaluating artificial transmission lines (ATL's) as a means to minimize the size of the low-impedance shunt stubs. As a result, we developed a 40-GHz frequency doubler, which used only 0.6-mm^2 area on a monolithic microwave integrated circuit. Despite the area minimization, the doubler exhibited state-of-the-art conversion loss of 1 dB over 10% bandwidth and rejected the fundamental frequency signal by more than 20 dB over 25% bandwidth. Reported herein is the novel simulation of the frequency doubler with active harmonic loads. Included in this paper are theoretical evaluation and simulation of ATL's with models for lumped components and verification of the results by electromagnetic simulation. Due to the high efficiency, low area requirement, and over 20-dB rejection of the fundamental signal, this miniaturized ATL frequency doubler can be used as a building block in the generation of local-oscillator signals in single-chip and MCM millimeter-wave systems.**

***Index Terms*—Artificial transmission line, frequency doubler, millimeter wave, MMIC.**

I. Introduction

GENERATION of millimeter-wave signals is a central problem in telecommunication applications. The signal source should provide sufficient power to the mixer, minimize the level of harmonic and nonharmonic spurious signals, and operate efficiently and reliably. Phase-noise requirements in modern digital telecommunication schemes are so strict that they usually are only obtained with microwave oscillators and frequency multiplication. A frequency multiplier is thus needed for the generation of the millimeter-wave signal. A significant advantage is achieved when the frequency multiplier can be integrated on the same chip as the mixer. The local oscillator (LO) interconnections then operate at less critical lower frequency and, due to frequency separation, the amount of LO leakage to the RF input is reduced. However, to achieve this integration, the frequency multiplier needs to effectively suppress the unwanted harmonics because on-chip bandpass filters would increase circuit complexity and size. Additionally, it has to occupy a very small area and operate efficiently. FET frequency multipliers have the advantage of low input power and the possibility to achieve conversion gain, whereas the main disadvantages are dc power consumption, potential instability, and narrow operating bandwidth. Previous single FET frequency multipliers were doublers, triplers, quadruplers, or even quintuplers. A doubler is preferred for the generation of a 40-GHz signal because spurious harmonics are effectively filtered in frequency doubling, and microwave oscillators are readily available at 20 GHz. The 40-GHz frequency band is used for point-to-point radio links and point-to-multipoint distribution systems, such as the microwave video distribution system (MVDS).

The analysis and design of a frequency doubler is a demanding task. Harmonic balance is a steady-state method, which is well suited for this purpose. However, potential instability of the doubler makes it difficult to optimize the efficiency with algorithms developed for harmonic balance. To successfully optimize, the design problem has to be restricted. Thus, simulations or measurements have to be performed to gain understanding of the device behavior in frequency doubling. In the past, a comprehensive study in [1] on the operation of a GaAs FET in frequency-doubler application showed that high conversion gain, up to oscillation, is obtained depending on the linear feedback on the fundamental frequency. The results of the study were achieved by varying reactive terminations at the output and input at fundamental and second harmonic frequency, respectively. On the other hand, the reactive terminations may limit the problem too severely. A topology independent optimization method utilized an added-power maximizing function in [2]. The added power was a function of $V_{\rm gs}$ and $V_{\rm ds}$. The powers at the input and output were calculated from the harmonic components of currents and voltages at the gate and drain of the FET. Other studies optimized operating conditions using analytical methods [3], [4]. When applying optimization methods, the instability of the doubler limits the usable terminating impedances. Thus, operating conditions and criteria have to be defined as in [2] and [5]. Another limitation is the performance of the FET model. Frequently, the FET models have incorrect discontinuities, especially at the resistive operating region of the FET. Thus, such a model may produce optimistic frequency multiplier optimization results because these nonphysical discontinuities generate harmonics.

This paper addresses the size reduction and reliable simulation of an efficient frequency doubler. The objectives of this paper are as follows: to demonstrate a new simulation method for the design of frequency multipliers, to assess the performance of artificial transmission lines (ATL's) with analytical

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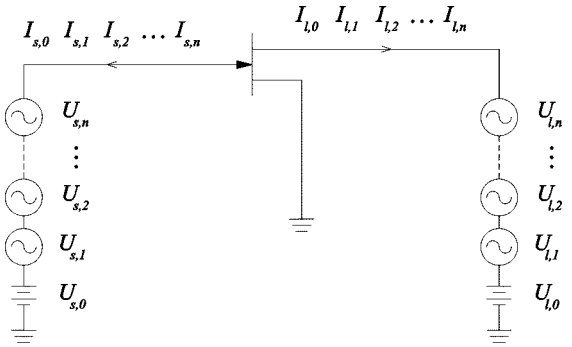

Fig. 1. Simulation network for the simulation of an FET nonlinear model as a frequency doubler. The input source side voltages $U_{s,n}$ at harmonics n are defined independently and the resulting currents $I_{s,n}$ are calculated using harmonic-balance simulation. In a similar manner, the output load side has independently defined voltages $U_{l,n}$ for different harmonics and the harmonic-balance simulation calculates the harmonic currents $I_{s,n}$. The $n = 0$ equals to dc.

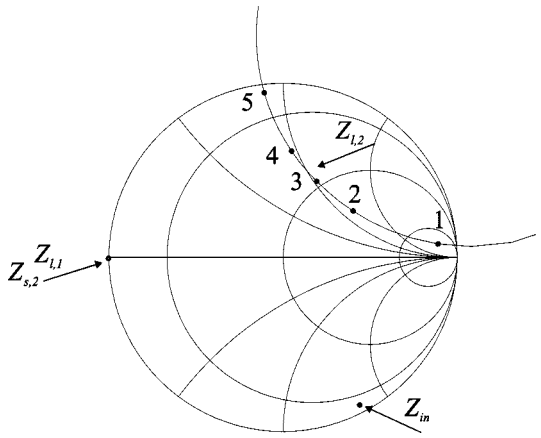

Fig. 2. Simulation results from 360° rotation of the second harmonic load voltage $U_{l,2}$. The second harmonic load $Z_{l,2}$ is the only impedance showing any change. The simulation results corresponding to five points on the $Z_{l,2}$ graph are shown in Table I.

models and electromagnetic (EM) simulations, and to present a novel minimum size monolithic circuit for frequency doubling using ATL's.

II. Evaluation of the FET Performance as a Frequency Doubler

We started the design of the frequency doubler by evaluating the performance of the FET under different harmonic load terminations. The analysis could have been performed using passive terminations with harmonic frequency bandpass filters, however, the use of active loads was more effective and informative. The harmonic-balance simulation had the advantage of separate definition of voltage sources for each harmonic frequency. Thus, we were able to modify the termination of the FET at each harmonic frequency independently with a very simple simulation network. A significant advantage was achieved by maintaining the voltages $v_{\rm gs}$ and $v_{\rm ds}$ of different harmonics n at constant amplitudes. The adjustments of the phases of these voltage sources simulated different loads. In this way, we controlled the operating region of the FET and reduced the amount of variables in the analysis. It was a logical way to approach the frequency multiplication problem since we were interested in the voltage and current waveforms in the intrinsic FET rather than the terminating loads that cause them.

The basic simulation setup is shown in Fig. 1. The voltage U_n at each harmonic frequency n is specified separately and the harmonic currents I_n are calculated by using harmonic balance. Each impedance Z_n created at the harmonics is then calculated from

$$Z_n = \frac{U_n}{I_n}. \tag{1}$$

The resistive part of the impedance has to be positive, i.e., $\mathrm{Re}(Z_n) > 0$, to be synthesized with a passive network. Naturally, at the fundamental frequency, the energy flows into the input of the circuit from the fundamental frequency signal source. Thus, (1) is applied to calculate the input impedance $Z_{\rm in}$ of the FET under large-signal conditions.

These simulations were performed using a foundry proprietary large-signal model of the $L_g = 0.2$ μm pseudomorphic high electron-mobility transistor (pHEMT) device. The device nonlinearities were implemented with nonlinear voltage-controlled current sources. The drain current and voltage waveforms of the internal device were plotted when different load impedances were applied. All voltages U_n were equal to zero, unless specified otherwise. To start the design, the biasing $(n = 0)$ was set to the threshold voltage V_t of the device. With this biasing, the input signal generates current pulses at the drain of the FET. This pulse formation was shown in [3] to efficiently generate a second harmonic signal. To obtain maximum conversion efficiency and low input power, the fundamental frequency voltage amplitude was set to $U_{s,1} = 1.5$ V. The peak voltage swing on the gate of the device was then from $v_{\rm gs} = -2.4$ V to $v_{\rm gs} = +0.6$ V. With these values, the gate of the FET exhibits neither significant forward conduction nor reverse breakdown. The drain of the device was biased to $v_{\rm ds} = 2$ V for operation in saturation region with low dc power consumption. The significant advantage in using active loads was that the second harmonic drain voltage amplitude may be set to a reasonable value and the phase of the voltage source rotated to load the transistor with a varying impedance. By inspecting the *I–V* curves, we noted that the amplitude should be limited to $U_{l,2} = 1$ V to maintain the drain voltage swing within the saturation region of the device and to avoid reverse breakdown of the gate.

Fig. 2 shows the load impedance $Z_{l,2}$ path, which was created when the load voltage $U_{l,2}$ phase rotated in harmonic-balance simulations. The input impedance $Z_{\rm in}$ did not change due to change in the second harmonic load. The corresponding input power, output power, conversion gain, input Q value, output Q value, and efficiency are shown in Table I. The input power was constant, regardless of the second harmonic load. Input Q was very high, which implied low bandwidth and difficulties in matching. The second harmonic power was $P_{l,2} = +6.8$ dBm, when the second harmonic load was optimum at point 3. The output matching did not appear to be critical since the achieved output power was nearly equal from points 2 to 4. Fig. 3 shows the internal load line of the FET superimposed on *I-V* curves

TABLE I

CHARACTERISTICS OF THE FREQUENCY DOUBLER WHEN SECOND HARMONIC LOAD IS VARIED IN HARMONIC-BALANCE SIMULATION. THE POINTS REFER TO THE POINTS IN THE SMITH CHART IN FIG. 2. THE TABLE SHOWS THE INPUT POWER AT FUNDAMENTAL FREQUENCY ($P_{\rm in}$), OUTPUT POWER AT SECOND HARMONIC ($P_{l,2}$), CONVERSION GAIN IN FREQUENCY DOUBLING, INPUT Q VALUE AT FUNDAMENTAL FREQUENCY ($Q_{\rm in}$), OUTPUT Q VALUE AT SECOND HARMONIC FREQUENCY ($Q_{l,2}$) AND EFFICIENCY OF THE DOUBLER CALCULATED AS EFFICIENCY $= P_{l,2}/(P_{\rm in} + P_{l,0})$

Point on Smith chart	P_{in} [dBm]	$P_{l,2}$ [dBm]	Conversion Gain [dB]	Q_{in}	$Q_{l,2}$	Efficiency [%]
1	-1.3	-2.5	-1.2	18.1	0.8	2.4
2	-1.2	5.8	6.9	17.9	0.7	16.1
3	-1.2	6.8	8.1	18.2	1.1	20.4
4	-1.4	6.3	7.7	18.9	2	18.1
5	-1.6	-2.4	-0.8	19.7	19.6	2.4

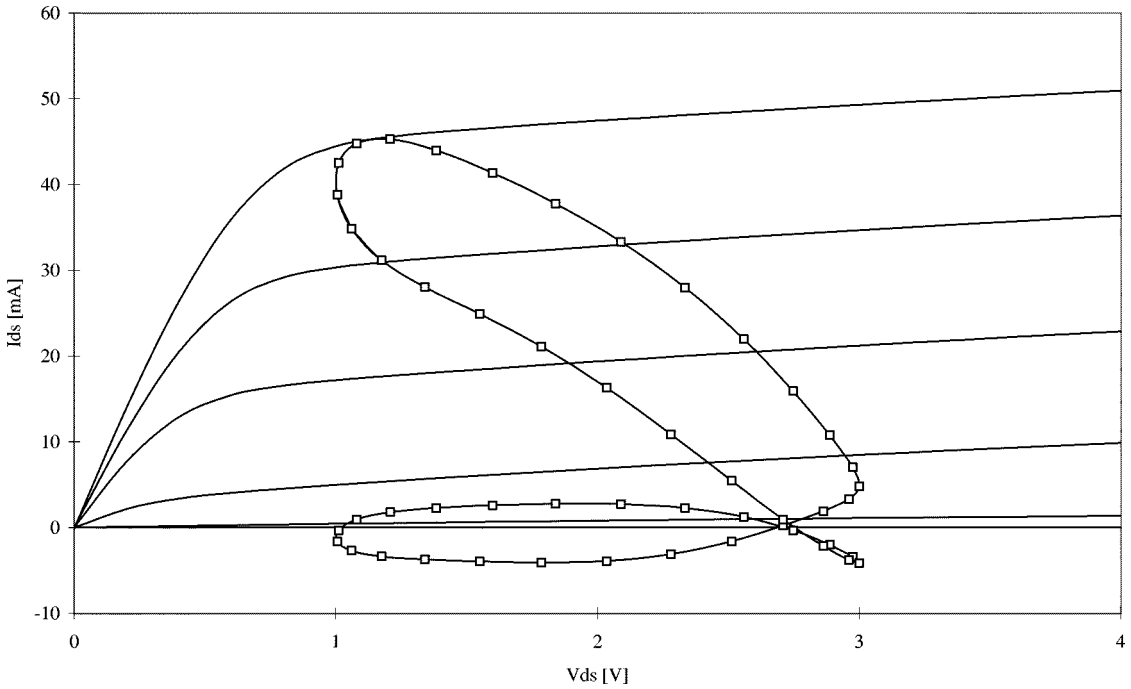

Fig. 3. Simulated internal load line ($-\square-$) at point 3 in Fig. 2. The load line is imposed on *I–V* curves for $V_{\rm gs}$ values from -1 V to $+0.7$ V.

when the second harmonic load was point 3 in Fig. 2. The loading of the FET internal current source was clearly at its optimum with this load. The input and output powers were calculated from the harmonic voltages and currents using the following formula:

$$\mathbf{P}_n = \mathrm{Re}\left\{\frac{U_n I_n^*}{2}\right\}. \tag{2}$$

The second harmonic load and fundamental input impedance were independent of each other, when the FET was operating in the saturation region. This independence of harmonic terminations was also shown in [1] and in [5].

However, in a practical circuit it is impossible to create a perfect short circuit because the passive parts of the circuit exhibit losses and limited bandwidth. Simulations with a different fundamental load voltage $U_{l,1}$ values showed that the load impedance $Z_{l,1}$ changed the input impedance $Z_{\rm in}$ due to the feedback in the transistor. As an example, Fig. 4 shows a $Z_{l,1}$ impedance path when the phase of the fundamental load voltage $U_{l,1} = 0.5$ V was varied. A capacitive $Z_{l,1}$ (point 1) increased the input resistance, while an inductive $Z_{l,1}$ caused the input resistance to decrease and to finally become negative

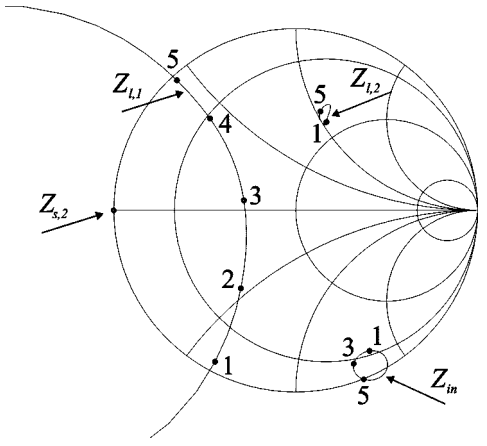

Fig. 4. Simulation results of the full 360° rotation of the fundamental load voltage $U_{l,1}$. The load impedance $Z_{l,1}$ has capacitive values in points 1 and 2, resistive in point 3, and inductive in points 4 and 5. The corresponding points of the FET input impedance $Z_{\rm in}$ show highly reactive impedance and unstability in point 5. The simulation results in these points are listed in Table II.

(point 5). In point 5, the voltage feedback from the $Z_{l,1}$ added in-phase to the input signal at the gate of the FET. The required input power was higher with capacitive $Z_{l,1}$, but the Q value

TABLE II
CHARACTERISTICS OF THE FREQUENCY DOUBLER WHEN FUNDAMENTAL FREQUENCY LOAD IS VARIED IN HARMONIC BALANCE SIMULATION. THE POINTS REFER TO THE POINTS IN THE SMITH CHART IN FIG. 4. ANNOTATIONS ARE AS IN TABLE I

Point on Smith chart	P_{in} [dBm]	$P_{l,2}$ [dBm]	Conversion Gain [dB]	Q_{in}	$Q_{l,2}$	Efficiency [%]
1	3.2	6.6	3.5	6.5	1.3	18.7
2	3.5	6.4	2.9	6.4	1.4	18
3	2.3	5.7	3.3	9.1	1.8	16.7
4	-2.4	5.8	8.2	27.2	1.8	18.2
5	Not Applicable	6.5	Infinite	Not Applicable	1.5	20.6

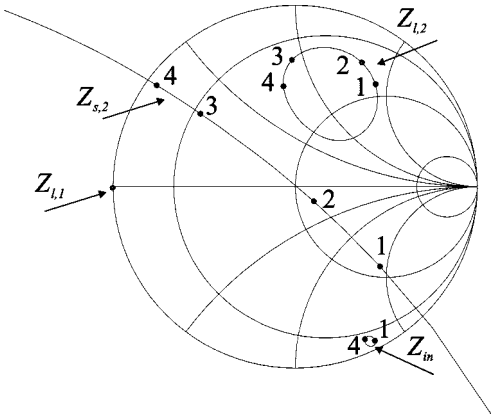

Fig. 5. Second harmonic source voltage $U_{s,2}$ 360° rotation results show the corresponding second harmonic source impedance $Z_{s,2}$ with points 1– 4. These points are also listed in Table III.

was lower and, thus, it was possible to have a fair input match over a wider bandwidth. A wide range of conversion gain performances could be obtained by changing the fundamental load, as is shown in the Table II. They were not achieved by enhancing the output power, but by reducing or increasing the required input power. The lowest possible input power leads to highest conversion gain, unfortunately it also means very difficult input matching due to the high Q value of the FET input. If the fundamental voltage at the output was further increased, the device started to operate partly in resistive region. This leads to modulation of $R_{\rm ds}$ and additional harmonics generation, which enhanced or decreased the doubler performance, depending on the particular loading conditions. However, this was subject to FET model accuracy in the resistive region, as was discussed in Section I and, thus, created uncertainty in the analysis of the doubler. Therefore, the fundamental load was required to be capacitive or short circuited to guarantee the stability of the doubler. The maximum conversion gain available with inductive load resulted in a risk of oscillations. Consequently, an inductive load was avoided in the design of the final doubler.

Thus far, the input impedance at the second harmonic was $Z_{s,2} = 0\,\Omega$. In practice, the nonideal $Z_{s,2}$ generates a reflection voltage $U_{s,2}$. Fig. 5 shows the second harmonic impedance $Z_{s,2}$ path with second harmonic voltage $U_{s,2} = 0.3$ V at the input. This $U_{s,2}$ value was a representative value to demonstrate the effect of $Z_{s,2}$. When $Z_{s,2}$ was close to the open circuit (point 1), the second harmonic voltage on the gate of the FET partially canceled the second harmonic signal on the drain of the FET, as can be seen from the reduction in the internal drain current, $\hat{I}_{d\,\mathrm{int},2}$ (Table III). A $Z_{s,2} = 50\,\Omega$ termination (point 2) improved the second harmonic current modestly, but a major improvement was achieved when the second harmonic voltage at the gate drove the FET close to in-phase (point 4). Point 4 was an inductive load, which resulted in maximum second harmonic current at the drain of the FET. Thus, the phase of the second harmonic input voltage $U_{s,2}$ was an important factor for achieving the maximum output power and an improvement in conversion gain. However, it was difficult to synthesize over a wide bandwidth due to the high Q value of the required network. We decided to synthesize a short-circuit network with small inductance for the second harmonic termination $Z_{s,2}$. The higher order harmonic voltages $U_{s,n}$ and $U_{l,n}$ were maintained equal to zero in these simulations. Thus, they did not distort these simulations, and their effect on the performance of the doubler was considered minor.

III. ATL STUBS DESIGN

Shunt stubs formed the basis of the monolithic-microwave integrated-circuit (MMIC) frequency-doubler design. The stubs allowed the synthesis of the required terminating impedances at harmonic frequencies independently. The $Z_{l,1}$ was close to zero and yet the required $Z_{l,2}$ could be synthesized when an open shunt stub was used, in which electrical length was $\phi = \pi/2$ at f_0. As was discussed in Section II, the low $Z_{l,1}$ reduces the $U_{l,1}$ and, thus, the feedback to the input and, consequently, the effect on the $Z_{\rm in}$, is minimized. However, the input impedance Z_s of the shunt stub was frequency dependent

$$Z_s = -jZ_0 \cot\left(\frac{f}{f_0}\frac{\pi}{4}\right) + R_{\rm loss}. \tag{3}$$

The lower the characteristic impedance Z_0 of the stub was, the lower the reactive part of the impedance was versus frequency. Consequently, bandwidth of the short improved with a low impedance stub under loaded conditions. A major problem with the $\lambda/4$ low impedance stub was the large area requirement, especially in microstrip technique. The physical length of the quarter wavelength stub was 1200 μm and width was 250 μm for a $Z_0 = 25\,\Omega$ microstrip on the 100-μm-thick GaAs substrate. For this reason, an ATL stub was the optimum solution in terms of the required area.

A. Theoretical Design

Transmission lines have been traditionally characterized with the equivalent circuit shown in Fig. 6. This low-pass circuit accurately matches the characteristic impedance Z_0 and propagation constant γ of a transmission line as long as the capacitance C_p and inductance L_p per section are sufficiently small.

TABLE III
CHARACTERISTICS OF THE FREQUENCY DOUBLER, WHEN SECOND HARMONIC SOURCE IMPEDANCE IS VARIED IN HARMONIC-BALANCE SIMULATION. THE POINTS REFER TO THE POINTS IN THE SMITH CHART IN FIG. 5. THE TABLE INCLUDES THE PEAK VALUE OF THE INTERNAL DRAIN CURRENT OF THE FET AT SECOND HARMONIC FREQUENCY ($\hat{I}_{d\,\mathrm{int},2}$) AND INPUT Q VALUE AT SECOND HARMONIC FREQUENCY ($Q_{s,2}$). THE REMAINING ANNOTATIONS ARE AS IN TABLE I

Point on Smith chart	P_{in} [dBm]	$P_{l,2}$ [dBm]	Conversion Gain [dB]	$\hat{I}_{dint,2}$ [mA]	$Q_{s,2}$	$Q_{l,2}$	Efficiency [%]
1	-1.4	3.1	4.5	5.6	1.5	2.3	9.3
2	-0.1	2.2	2.3	8.1	0.1	3.9	7.5
3	1.4	5.5	4.1	15.3	1.4	2.7	14.6
4	1	7.7	6.7	17.5	10.2	1.6	22.4

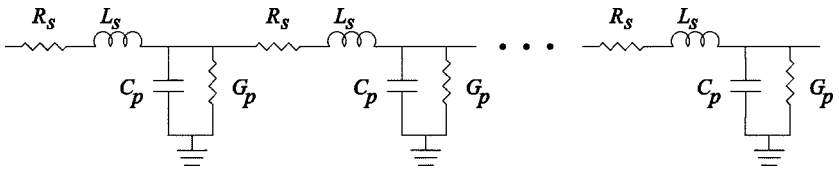

Fig. 6. Equivalent circuit of a transmission line. This circuit is used in the doubler as an ATL or line simulating network [6].

The transmission-line simulating properties vanish totally at the cutoff frequency f_c of the equivalent circuit. The characteristics of the transmission line are calculated from the formulas

$$Z_0 = \sqrt{\frac{L_s + R_s}{C_p + G_p}} \tag{4}$$

and

$$\gamma = \sqrt{(R_s + j\omega L_s)(G_p + j\omega C_p)}. \tag{5}$$

Thus, it was also possible to create a $\lambda/4$ transmission-line simulating network of arbitrary impedance with lumped capacitors and inductors. This type of solution is called an ATL or line simulating network, as in [6]. The main advantages achieved by this approach are a significant reduction in the physical length of the structure and the possibility to use a low-impedance transmission line without increasing the width of the structure. However, the bandwidth of the lossless transmission line was limited by the cutoff frequency

$$f_c = \frac{1}{\pi\sqrt{L_s C_p}}. \tag{6}$$

Thus, there existed a tradeoff in between the required phase shift and the transmission-line cutoff frequency in terms of the number of *LC* sections. The minimum necessary number was to be used; however, the second harmonic frequency of the doubler had to be sufficiently below the ATL cutoff frequency for undistorted operation, regardless of process variations. The change of ATL characteristic impedance Z and phase constant β versus frequency was

$$Z = \frac{Z_0}{\sqrt{1 - \left(\frac{f}{f_c}\right)^2}} \tag{7}$$

and

$$\beta = 2\arcsin\left(\frac{f}{f_c}\right). \tag{8}$$

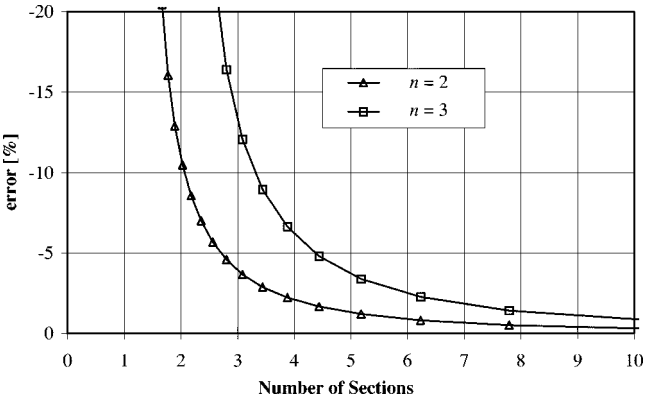

Fig. 7. Error in phase of the quarter-wave ATL stub versus number of sections. The phase is matched to 90° at the fundamental frequency ($n = 1$) and the deviation is calculated at higher harmonics.

We calculated the number of sections n_s needed for a $\lambda/4$ transmission line with certain inductance L_s and capacitance C_p per section as

$$n_s = \frac{\pi}{4\arcsin(\pi f\sqrt{L_s C_p})}. \tag{9}$$

The phase-shift frequency dispersion of the ATL causes an error E at the harmonic frequencies nf_0

$$\begin{aligned} E_n &= \frac{\phi_{\mathrm{err},nf_0}}{n(\pi/2)} \\ &= \frac{n(\pi/2) - n_s\beta_{nf_0}}{n(\pi/2)} \\ &= 1 - n_s\frac{\arcsin(\pi n f\sqrt{L_s C_p})}{n\pi}. \end{aligned} \tag{10}$$

This phase error was plotted in Fig. 7. The second harmonic phase error did not reduce significantly when more than five sections were used.

B. EM and Standard Foundry Model Simulations of ATL's

Today, the commercial MMIC foundries offer well-characterized metal–insulator–metal (MIM) capacitors and spiral and line inductors. Thus, these models were directly applied to the

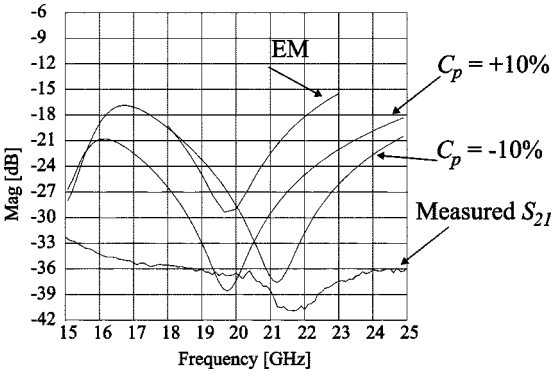

Fig. 8. Simulated shunt open stub S_{21} using: 1) method-of-moments EM simulation and 2) foundry provided models for inductors and MIM capacitors with a manufacturing tolerance ($C_p = \pm 10\%$). The S_{21} of the measured circuit is included for comparison (Measured S_{21}). The simulation with foundry provided models is accurate enough to predict the performance of the doubler since the manufacturing tolerance produces the largest variation.

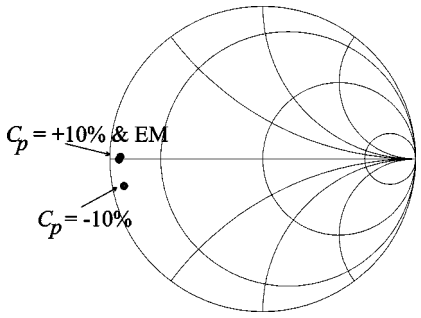

Fig. 9. Simulated input impedance of the shunt stub at $f = 20$ GHz. The annotations are as in Fig. 8.

design of ATL's. The main disadvantage was that the coupling from the lines to the capacitor top electrodes and the ground via metallization were not taken into account. Fig. 8 shows the simulation results of the five-section shunt-open ATL stub, which has an electrical length of $\lambda/4$ at 20-GHz frequency. Simulations were performed utilizing analytical models, provided by the foundry, for line inductors and MIM capacitors. The tolerance of the MIM capacitors was $\pm 10\%$; thus, we simulated the performance of the ATL with these values. The simulation results are compared in Fig. 8 to results obtained with a planar EM simulator. The EM simulator used the method of moments without taking into account the thickness of metal layers. The measured S_{21} of the processed doubler was included in Fig. 8 for comparison. The measured and EM simulation resonant frequencies of the stubs are within the resonance frequencies of the simulations with analytical models, when the tolerance of the MIM capacitors is $\pm 10\%$. Thus, the simulation of the ATL's with analytical models is accurate enough compared to the variation of the MMIC process parameters. The results of the simulations at 20 GHz are also presented on the Smith chart in Fig. 9. These simulations of S_{11} showed the small variation of the $Z_{l,1}$ regardless of the variations in MIM capacitors. The input matching and power requirement was strongly dependent on $Z_{l,1}$, as was demonstrated in Table I. Thus, the low-impedance ATL improved the bandwidth and probability of success in matching the input of the frequency doubler since

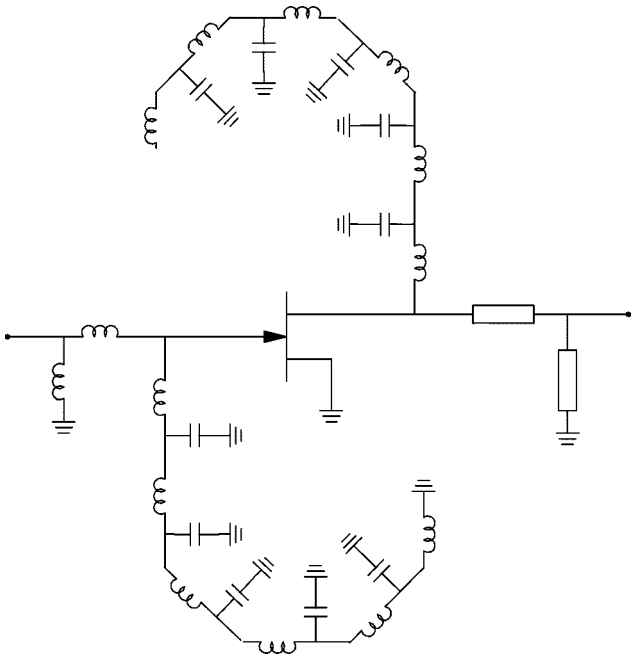

Fig. 10. Schematic of the miniaturized ATL frequency doubler. At the drain of the FET, an ATL open-shunt stub is formed by the *LC* ladder network. The gate side has a shorted shunt stub using the ATL technique. Biasing circuits are omitted for clarity.

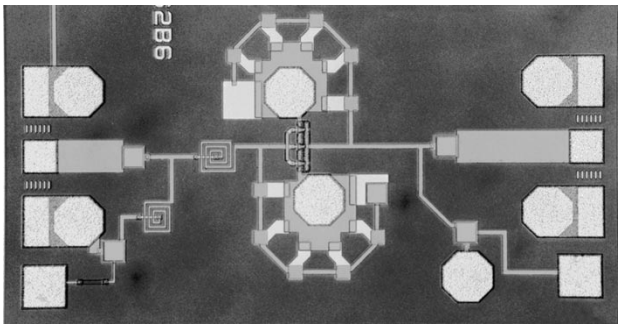

Fig. 11. Processed ATL frequency doubler. The doubler circuit uses a 0.6 mm^2 area on the chip and each ATL stub requires less than a 0.1-mm^2 area.

the $Z_{l,1}$ was close to 0Ω regardless of simulation uncertainties and processing tolerances.

IV. Experimental Results

The evaluation of the FET performance in Section II demonstrated that the best performance was achieved when the output $Z_{l,1}$ and input $Z_{s,2}$ impedances were close to 0Ω, the source impedance was $Z_{s,1} = 5\,\Omega + j80\,\Omega$, and the load impedance $Z_{l,2} = 50\,\Omega + j50\,\Omega$. These conditions were achieved by using ATL shunt stubs at the input and output of the device, a shorted at the input and an open at the output, and normal passive components for input and output matching to $50\,\Omega$. A schematic of the circuit is presented in Fig. 10.

A. Design

The FET in the used commercial MMIC process was a 6×15 μm depletion pHEMT. The gate of the device was a T-structure and source was grounded with via holes on both

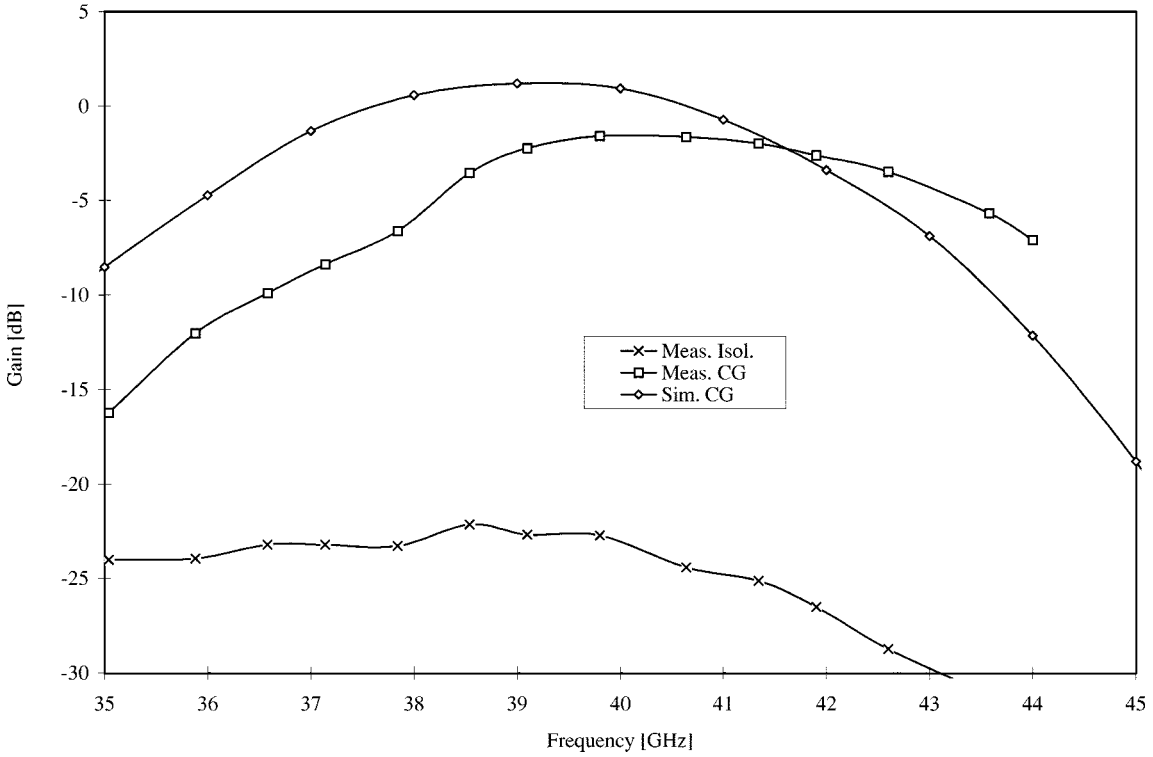

Fig. 12. Measured conversion gain (Meas. CG) of the ATL frequency doubler versus output frequency. The simulated conversion gain is shown for comparison (Sim. CG). More than 20-dB isolation of the fundamental frequency signal (Meas. Isol.) is measured over the measurement bandwidth. The input power is $P_{\rm in} = +5$ dBm.

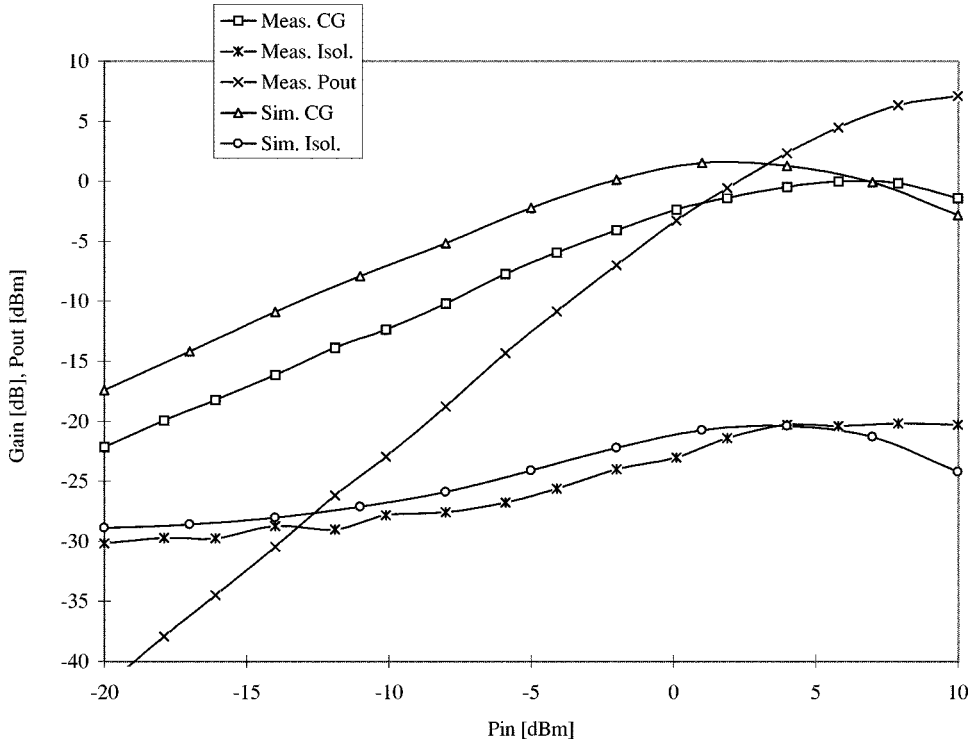

Fig. 13. Input power dependence of the ATL frequency doubler at $f_0 = 20$ GHz input frequency. The measured (Meas. CG) and simulated (Sim. CG) conversion gain and the measured (Meas. Isol.) and simulated (Sim. Isol.) isolation are plotted. The measured output power (Meas. Pout) saturates to $+6$ dBm.

sides. The ATL stubs were also grounded to these same vias and, thus, a very compact structure resulted.

The input matching to 50 Ω included spiral inductors in series and parallel. At 20-GHz frequency, the resonant frequency of these small spiral inductors was at a sufficiently higher frequency. The impedance of the input matching network at the $2f_0$ was insignificant because the input-shunt ATL stub was an effective short at this frequency. At the output, the open

ATL shunt stub shorted the f_0. The output matching was with microstrips.

The photograph of the final circuit is presented in Fig. 11. The area requirement of the circuit was only 0.6 mm^2 on a standard chip in multiuser processing. Of this area, the FET and ATL stubs employed only 0.3 mm^2, even though low impedance $(Z_0 = 25\,\Omega)$ stubs were used. These were excellent results since an electrically equivalent circuit with microstrip stubs would have required at least 1.5 mm^2 circuit area. Consequently, the size of the circuit was reduced to 40% of the conventional one. Even when high-impedance microstrip lines were used in [7], the circuit size was typically 1.5 mm^2, whereas with coplanar techniques in [7] narrow lower impedance $(Z_0 = 50\ \Omega)$ lines were designed for the frequency doubler. However, even with coplanar techniques in [7], the length of the lines was not reduced and the size of the circuit was approximately 1.5 mm^2.

B. Measurement of the Doubler

The processed doubler circuit was measured as a function of frequency and input power with coplanar probes. Fig. 12 shows the measured conversion gain to second harmonic frequency and the rejection of the fundamental frequency component. In Fig. 12, simulation results are also presented for comparison. Input power was $P_{\text{in}} = +5$ dBm in measurements and simulations. The second harmonic conversion gain was -1 dB and the 3-dB bandwidth was 10%. The rejection of the fundamental frequency component was more than 20 dB over the frequency bandwidth of the measurement, which was an important property for future integration of the doubler together with a mixer or an amplifier on a single chip. This unique performance was achieved by using the low-impedance ATL stubs at the input and output of the doubler. We performed the same measurements also as a function of input power at 20-GHz input frequency (see Fig. 13). The maximum conversion gain was -1 dB at $P_{\text{in}} = +5$ dBm input power and the output power saturated to $P_{\text{out}} = +6$ dBm. The rejection of the fundamental frequency component was 20 dB even at output power saturation. To the knowledge of the authors, these results are among the best reported for millimeter-wave FET frequency doublers. This is supported by a comprehensive literature review in [8], which reported best conversion gain values of -1 dB at 40 GHz. The novel ATL frequency-doubler design did not degrade the performance of the frequency doubler; on the contrary, the bandwidth and fundamental rejection performance was improved due to the possibility to use low-impedance stubs.

V. Conclusion

This paper describes the substantial benefits of using ATL's in frequency doublers. More specifically, we have demonstrated a novel frequency-doubler topology, which employed ATL's in the shunt stubs. The ATL's enabled us to design very broad-band very low-impedance stubs, with a record low area of 0.3 mm^2 on the MMIC chip. We measured 1-dB conversion loss from the processed circuits, which was among the best results reported for 40-GHz frequency doublers. The rejection of the fundamental frequency component was more than 20 dB over more than 25% bandwidth, which was a significant property, when this frequency doubler will be used as a LO signal generator for a mixer in a single-chip multifunction circuit. Furthermore, a frequency-doubler simulation methodology was presented, which is applicable for the design of any nonlinear component, such as mixers and power amplifiers, among others. In all of these design tasks, we can control the operating region of the FET to avoid simulations in an unreliable area of the FET model.

References

[1] C. Rauscher, "High-frequency doubler operation of GaAs field-effect transistors," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, pp. 462–473, June 1983.

[2] C. Guo, E. Ngoya, R. Quere, M. Camiade, and J. Obregon, "Optimal CAD of MESFET frequency multipliers with and without feedback," in *IEEE MTT-S Int. Microwave Symp. Dig.*, New York, NY, May 1988, pp. 1115–1118.

[3] A. Gopinath and J. B. Rankin, "Single-gate MESFET frequency doublers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 869–875, June 1982.

[4] S. Maas, *Nonlinear Microwave Circuits*. Norwood, MA: Artech House, 1988, pp. 397–416.

[5] I. Schmale and G. Kompa, "A Stability-ensuring procedure for designing high conversion-gain frequency doublers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Baltimore, MD, June 1998, pp. 873–876.

[6] H. J. White, P. R. Gillette, and V. J. Lebacqz, "The pulse-forming network," in *Pulse Generators*, G. N. Glasoe and J. V. Lebacqz, Eds. New York: McGraw-Hill, 1948, pp. 175–225.

[7] P. Kangaslahti, P. Alinikula, and V. Porra, "Millimetre wave signal generation using monolithic HEMT technologies," *Analog Integrated Circuits and Signal Processing*, vol. 15, pp. 123–133, Jan. 1998.

[8] I. Schmale and G. Kompa, "Choosing the right frequency doubler technology," in *Proc. 2nd ESA Workshop Millimeter Wave Technol. Applicat.: Antennas, Circuits, Syst.*, Espoo, Finland, May 1998, pp. 467–472.

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