Power Optimization of High-Efficiency Microwave MESFET Oscillators

Kwok-Keung M. Cheng, *Member, IEEE,* and Kwok-Po Chan

***Abstract*—Achieving high output power and efficiency in GaAs MESFET oscillators is mainly hampered by the device's parasitics, its static *I–V* characteristics, and the circuit embedding impedance. In this paper, the derivation of the relationship between oscillator output power and various circuit and device parameters is presented. From these analytical expressions, optimum operating conditions for maximum oscillator output power and efficiency are determined. The analysis method employed here is based upon a quasi-linear approach and an open-loop model of the oscillator. The design procedure is verified by measurements on an experimental circuit, which have demonstrated a dc/radio-frequency conversion efficiency of 54%.**

***Index Terms*—MESFET, microwave oscillators, optimization.**

I. Introduction

MAXIMIZING oscillator output power and efficiency has been the design emphasis of many researchers in recent years [1]–[4]. This is particularly important for some applications such as the active phase-array antenna, where cost, power consumption, repeatability, and reliability are the main design requirements. The MESFET is a very attractive device for high output power and efficiency oscillator applications. Evans [1] described a MESFET oscillator at 16.8 GHz with a conversion efficiency of 28%, and an output power of 28 mW. Furthermore, circuit designers [3] have reported improved efficiency resulting from proper terminations at multiple harmonic frequencies. Recently, Bryerton *et al.* [4] have demonstrated a class-E MESFET oscillator at 5 GHz, with efficiency of 59% and output power of 300 mW. Achieving high output power in microwave oscillator is mainly hampered by the device's parasitics, its static *I–V*, as well as the circuit embedding impedances [5], [6]. The favorable embedding impedances are usually determined by using an automatic tuner and/or a circuit-simulation program. Numerical methods such as the harmonic-balance technique [7], while useful for analysis, provide little insight needed for design. In addition, deriving an accurate large-signal device model is a time-consuming task. In this paper, an investigation into the problem of power optimization of GaAs MESFET oscillators operated in a class-B mode is given. Explicit formulas expressing oscillator output power as a function of circuit parameters are derived based upon an open-loop model of the oscillator and quasi-linear approximation. These equations also provide a good understanding of the fundamental limitations in obtaining high output power in microwave oscillators. For demonstration, a 950-MHz hybrid oscillator is constructed and characterized.

Manuscript received February 17, 1999.

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Publisher Item Identifier S 0018-9480(00)03749-2.

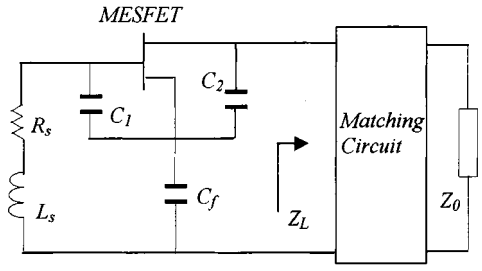

Fig. 1. Oscillator circuit configuration.

II. Open-Loop Model of Oscillator

Fig. 1 shows a conventional oscillator configuration where the external embedding circuits are represented by L_s, R_s (effective loss resistance of L_s), feedback capacitance C_f, and load termination Z_L. To improve phase-noise performance, the inductor can be replaced by a high-Q resonator. In this proposed design, two external capacitors (C_1 and C_2) are inserted into the circuit to allow additional freedom in optimizing the oscillator output power (to be explained later). Generally speaking, a highly efficient oscillator may be achieved by biasing the MESFET device to a low quiescent current and allowing the RF feedback signal to swing the device into conduction. The simple process of reducing the conduction angle is illustrated in Fig. 2. In this operating mode (class B), drain current flows only during half of the RF input cycle. It is clear that a sufficiently large drive signal will swing the device beyond pinchoff, V_p on the negative portion of the RF cycle [8]. It is also assumed that a maximum drain current of $I_{\max}$ is obtained as the gate–source voltage is increased toward its clamping value. Furthermore, $I_{\rm ds}(t)$ is assumed to be independent of drain voltage as long as $V_{\rm ds}(t)$ stays above the knee voltage and below the device breakdown voltage. Accordingly, the coefficients of the Fourier expansion of $I_{\rm ds}(t)$ are

$$I_{\rm dc} = \frac{I_{\max}}{\pi} \quad I_1 = \frac{I_{\max}}{2} \tag{1}$$

where $I_{\rm dc}$ is the dc component and I_1 is the peak value of the fundamental component [8]. It is obvious that the half-cosine current waveform contains many harmonics, and it is, therefore, very difficult to draw the resulting voltage waveform for a given load condition. The analysis can be greatly simplified by assuming that all harmonic currents are presented with a short-circuited termination. This assumption may be justified by the low harmonic content of the current waveform [8] and the presence

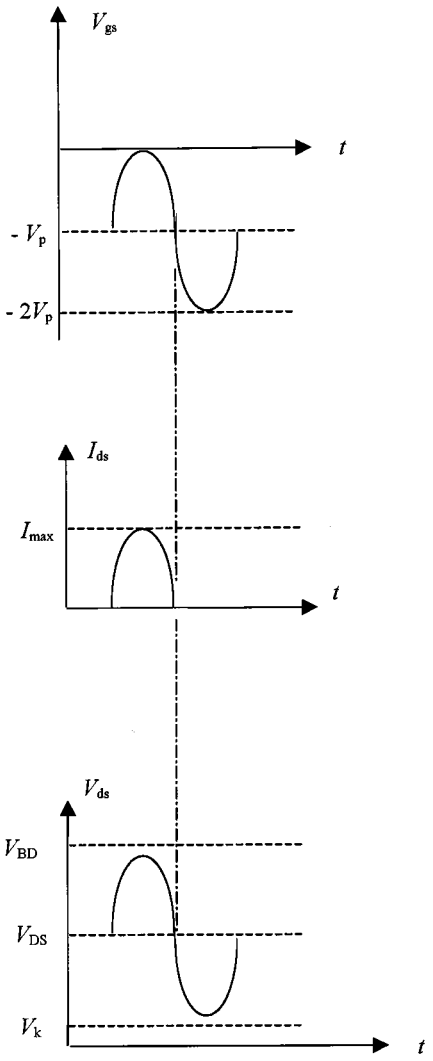

Fig. 2. Voltage and current waveforms.

of the output capacitance. The output capacitor value is chosen such that its reactance at higher harmonic frequencies is much lower than the fundamental load-line resistance. As a result, all voltage harmonics are eliminated and, thus, the drain voltage is simply a sinusoidal waveform whose magnitude is set by the load impedance value.

Fig. 3(a) shows the open-loop model of the oscillator circuit. It is assumed that some of the parasitic elements of the FET are absorbed into the corresponding embedding impedances. This model can be further simplified as the one shown in Fig. 3(b), provided that $\omega_0 C_{\rm gs} R_i \ll 1$

$$\begin{aligned} C_a &= C_1 + C_{\rm gs} \\ C_b &= C_2 + C_{\rm ds} \\ R_a &= R_s + \left(\frac{C_{\rm gs}}{C_a}\right)^2 R_i \end{aligned} \tag{2}$$

where $C_{\rm gs}$, $C_{\rm ds}$, and R_i are the intrinsic elements of the active device; ω_0 is the frequency of oscillation. For the purpose of analysis, the following additional assumptions are required.

1) Class-B mode of operation is assumed. Sinusoidal voltage waveforms of proper amplitude and dc offset are maintained at both the gate and drain terminals of the active device (Fig. 2). The gate–source voltage has to be less than the diode clamping voltage (a zero value is assumed here) and larger than twice the pinchoff voltage of the channel.
2) The maximum drain voltage swing ($V_{\rm dsm}$) can be determined from the supply voltage ($V_{\rm DS}$) and the *I–V* of the FET. Ideally, the drain voltage has to be above the knee voltage (V_K) of the transistor and below the breakdown voltage ($V_{\rm BD}$) of the drain–source junction

$$V_{\rm dsm} = \begin{cases} V_{\rm DS} - V_k, & \text{if } V_{\rm DS} - V_k < V_{\rm BD} - V_{\rm DS} \\ V_{\rm BD} - V_{\rm DS}, & \text{if } V_{\rm DS} - V_k > V_{\rm BD} - V_{\rm DS}. \end{cases} \tag{3}$$

3) The device is considered to have very high output resistance. The gate impedance is assumed to remain constant over the RF cycle, other than some smaller effects arising from the voltage-dependent depletion capacitance.

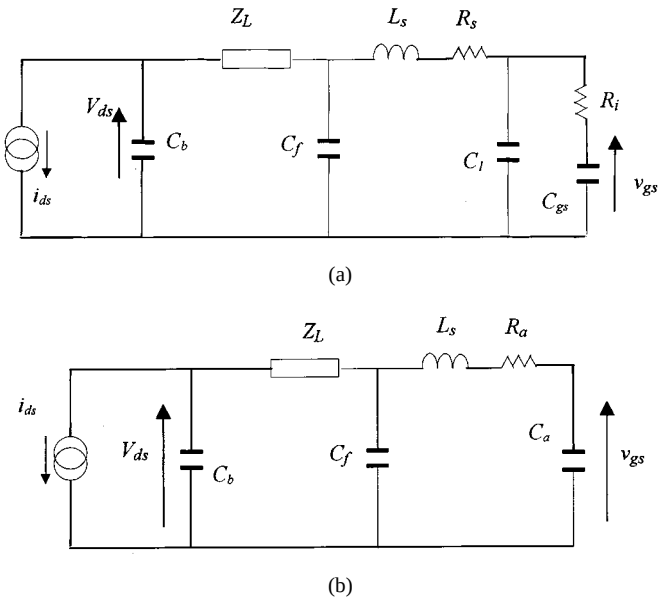

Fig. 3. Equivalent circuit of oscillator. (a) Open-loop model. (b) Simplified model.

III. Derivation of Optimum Operating Conditions

Basically, the model shown in Fig. 3(b) consists of a current source $I_{\rm ds}(t)$ and a frequency-selective network. This network is intended to be used for providing the proper phase shift and signal level for the input of the FET. By applying linear circuit analysis, an expression for $v_{\rm gs}$ may be derived as

$$v_{\rm gs} = -i_{\rm ds} \times \frac{Z_i}{1 + j\omega_0 C_b (Z_L + Z_i)} \times \frac{1}{j\omega_0 C_a (R_a + jX_a)} \tag{4}$$

where

$$\begin{aligned} Z_i &= \frac{R_a + jX_a}{1 + j\omega_0 C_f (R_a + jX_a)} \\ X_a &= \omega_0 L_s - \frac{1}{\omega_0 C_a} \end{aligned}$$

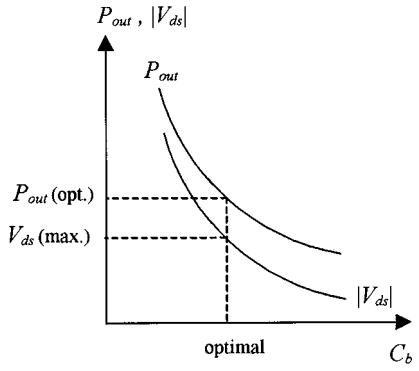

Fig. 4. Dependencies of oscillator output power on C_b.

and $i_{\rm ds}$ is the fundamental component of $I_{\rm ds}(t)$. Steady-state oscillation occurs when $i_{\rm ds} = I_1$ and $v_{\rm gs} = V_p$. Consequently, (4) may be rewritten as

$$1 + j\omega_0 C_b(Z_L + Z_i) = -g_{mc} \times \frac{Z_i}{j\omega_0 C_a(R_a + jX_a)}$$

or

$$Z_L = Z_i \left\{ \frac{g_{mc}}{\omega_0^2 C_a C_b (R_a + jX_a)} - 1 \right\} - \frac{1}{j\omega_0 C_b} \tag{5}$$

where

$$g_{mc} = \frac{I_1}{V_p} = \frac{I_{\max}}{2V_p}.$$

In addition, the power delivered to the load Z_L and the magnitude of $V_{\rm ds}$ can be determined by

$$P_{\rm out} = \frac{1}{2} I_1^2 \times \frac{\mathrm{Re}[Z_L]}{\left|1 + j\omega_0 C_b(Z_L + Z_i)\right|^2}$$

$$|V_{\rm ds}|^2 = I_1^2 \frac{|Z_L + Z_i|^2}{\left|1 + j\omega_0 C_b(Z_L + Z_i)\right|^2}. \tag{6}$$

By substituting (5) into (6) and then simplifying, we obtain

$$P_{\rm out} = \frac{1}{2} I_1^2 \times \left(\alpha \frac{1 - \omega_0 C_f X_a}{\omega_0 C_b} - \alpha^2 R_a \right) \tag{7}$$

$$|V_{\rm ds}|^2 = I_1^2 \times \frac{\alpha^2(1 - \omega_0 C_f X_a)^2 + (1 - \alpha\omega_0 C_f R_a)^2}{\omega_0^2 C_b^2} \tag{8}$$

where

$$\alpha = \frac{\omega_0 C_a}{g_{mc}}.$$

Fig. 4 shows the plots of the variations of $P_{\rm out}$ and $|V_{\rm ds}|$ as a function of C_b, keeping the other parameters fixed. The diagram indicated that the smaller the value of C_b, the higher the output power. However, $|V_{\rm ds}|$ cannot be increased without limit because of the voltage constraint stated in (3). Hence, by setting $|V_{\rm ds}| = V_{\rm dsm}$, the following optimal condition is obtained:

$$\omega_0 C_b R_{\rm opt} = \sqrt{\alpha^2(1 - \omega_0 C_f X_a)^2 + (1 - \alpha\omega_0 C_f R_a)^2} \tag{9}$$

where

$$R_{\rm opt} = \frac{V_{\rm dsm}}{I_1} = \frac{2V_{\rm dsm}}{I_{\max}}.$$

Using the above result, the optimum $P_{\rm out}$ is, therefore, given by

$$P_{\rm out} = \underbrace{\frac{V_{\rm dsm} I_{\max}}{4} \times \frac{\alpha(1 - \omega_0 C_f X_a)}{\sqrt{\alpha^2(1 - \omega_0 C_f X_a)^2 + (1 - \alpha\omega_0 C_f R_a)^2}}}_{\text{power available from the current source, } P_{av}} - \underbrace{(\omega_0 C_a V_p)^2 \frac{R_a}{2}}_{\text{power absorbed by } R_a, P_f}. \tag{10}$$

It should be pointed out that the amount of power delivered to the load ($P_{\rm out}$), as described by (10), is equal to the difference between the power available from the current source and the power absorbed by R_a. The latter can be regarded as the amount of feedback power required by the oscillator. Also, from the above expressions, several important implications can be made as follows.

1) Maximum output power is attained if we set

$$C_f = \frac{1}{\alpha\omega_0 R_a}. \tag{11}$$

As a result

$$P_{\rm out}(\max.) = \frac{V_{\rm dsm} I_{\max}}{4} \left(1 - \frac{1}{G}\right) \tag{12}$$

where

$$\frac{1}{G} = \frac{P_f}{P_{av}} = \omega_0^2 C_a^2 R_a \frac{2V_p^2}{V_{\rm dsm} I_{\max}}.$$

Accordingly, the dc/RF conversion efficiency is calculated by

$$P_{\rm dc} = V_{\rm DS} \times \frac{I\max}{\pi}$$

$$\eta(\max.) = \frac{P_{\rm out}(\max.)}{P_{\rm dc}} = \left(1 - \frac{1}{G}\right) \times \frac{V_{\rm dsm}}{V_{\rm DS}} \times 78.5\%. \tag{13}$$

According to (12) and (13), in order to maximize the oscillator output power and efficiency, the loss resistance (R_A) of the input circuit has to be reduced (increasing G) and an optimal biasing condition ($V_{\rm DS}$) has to be selected.

2) By combining (9) and (11), the optimum value of C_b can be found as

$$C_b = \frac{1 - \omega_0 C_f X_a}{g_{mc} R_{\rm opt}} C_a. \tag{14}$$

In practice, the given device's parasitic may not satisfy the above condition and, therefore, external capacitors (C_1 and C_2) will be needed.

3) From (5) and (14), a simple expression for the evaluation of the optimum load impedance can be derived as follows:

$$Z_L = \frac{1 + j\alpha}{1 + \alpha^2} R_{\rm opt} \tag{15}$$

assuming that $X_a \approx 0$. The load-matching network may be synthesized by either lumped or distributed elements.

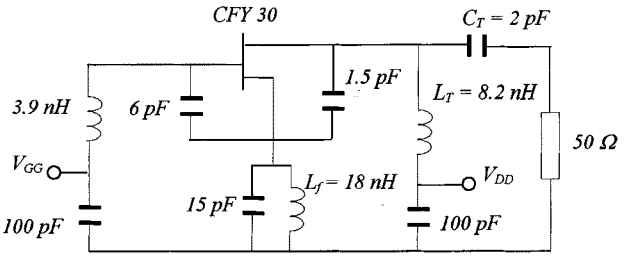

Fig. 5. Circuit configuration of a 950-MHz oscillator design.

IV. Experiments and Discussions

Fig. 5 shows the schematic diagram of an experimental oscillator circuit operating at 950 MHz. A simple high-pass filter (L_T and C_T) is employed to transform the 50-Ω load to the required Z_L value. This oscillator was fabricated using a CFY 30 GaAs MESFET biased at $V_{\rm DS} = 5.0$ V and $I_{\rm DS} = 18$ mA. Other device's parameters are $V_k = 0.5$ V, $V_P = 1.25$ V, and $I_{\max} = 45$ mA. Notice that the effects of the device's parasitics ($C_{\rm gs}$ and $C_{\rm ds}$) are insignificant here due to the presence of the relatively large external capacitors (C_1 and C_2). The 3.9-nH inductor is found to have an effective loss resistance (R_A) of 4Ω. Note that an additional inductor (L_f) is included in the circuit for biasing purposes. Subsequently, by inserting the above information into (11)–(15), the following set of design parameters is obtained:

$$\begin{aligned}
\alpha &= 2.0 \\
R_{\rm opt} &= 200\ \Omega \\
Z_L &= 40 + 80\ j\Omega \\
C_a &= 6.5\ \text{pF} \\
C_b &= 1.7\ \text{pF} \\
C_f &= 20\ \text{pF} \\
C_T &= 1.91\ \text{pF} \\
L_T &= 8.9\ \text{nH} \\
P_{\rm out}(\max.) &= 16.6\ \text{dBm} \\
\eta(\max.) &= 64\%.
\end{aligned}$$

After the oscillator circuit is constructed, some tuning is applied to bring the oscillating frequency back to the required value. Furthermore, in order to ensure stable oscillation, the gate bias is set slightly below pinchoff and, as a result, the mode of operation is close to class AB. The circuit was measured to have an output power of 16.8 dBm, a dc/RF conversion efficiency of 54%, and a second harmonic power level of below -2 dBm. The experimental results indicate that the measured output power deviates less than 0.3 dB from the predicted value. The reduced efficiency is believed to be due to the losses in the matching circuit, which has not been considered. Furthermore, the results are found to be reproducible upon making measurements on several similar oscillator circuits.

V. Conclusion

In this paper, an analytical design method has been described in optimizing the output power of GaAs MESFET oscillators. The maximum achievable output power and efficiency for a given active device can be predicted through the closed-form expressions derived, without the need of sophisticated large-signal device characterization and harmonic-balance simulation. Simple and explicit equations are readily available for determining the optimum circuit parameter values for maximum output power and efficiency. The procedure was successfully applied to designing a high-efficiency GaAs MESFET oscillator operating at 950 MHz. Good agreement between measured and predicted performances was observed.

Acknowledgment

The authors would like to thank the reviewers for their invaluable comments.

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