A Low-Current and Low-Distortion Wide-Band Amplifier Using 0.2-μm Gate MODFET Fabricated by Using Phase-Shift Lithography

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***Abstract*—We have developed a wide-band amplifier that can keep a gain over 10 dB at an operation current of 10 mA from 100 MHz to 3 GHz. The fabricated integrated circuit (IC) achieved a high-output third-order intercept point of 30 dBm and low noise figure of 1.6 dB at 800 MHz, respectively. The present IC employs a MODFET with 0.2-μm gate fabricated by using a phase-shift lithography technique.**

***Index Terms*—Amplifier, feedback, GaAs, lithography, low current, low distortion, MODFET, phase shift, wide-band.**

I. Introduction

RECENT wireless communication systems require high-frequency devices with wider band operation and lower VSWR with lower consumption current. Wide-band amplifier integrated circuits (IC's) are well suited to these demands, except for low-consumption current. A gate-to-drain feedback configuration has been used for wide-band IC's [1]–[5].

Weldish reported on a wide-band amplifier IC from 40 to 860 MHz with negative feedback. Niclas reported on a wide-band amplifier IC up to 14 GHz with both negative and positive feedbacks to obtain wider bandwidth. However, those IC's developed thus far consume large currents over 100 mA, which results in limiting the application fields. It is important to reduce consumption current to apply these IC's for mobile communication handsets. Furthermore, recent digital modulation systems such as $\pi/4$ QPSK, 16 quadrature amplitude modulation (QAM), and offset QPSK demand extremely low-distortion characteristics, which generally causes an increase of the operation current. However, the relationship between low-consumption current and low-distortion characteristics are usually a tradeoff.

In this paper, a wide-band amplifier IC to achieve both low-consumption current and low-distortion characteristics is demonstrated. The methodology to reduce operation current of wide-band amplifier IC's is discussed from the equivalent circuit of the IC's. A phase-shift lithography technique and a high dielectric capacitor using $SrTiO_3$ technology were employed to fabricate a 0.2-μm gate MODFET that is an essential RF device for the wide-band amplifier IC's. These novel process technologies are also described. The RF characteristics of the wide-band amplifier IC's were then evaluated and discussed.

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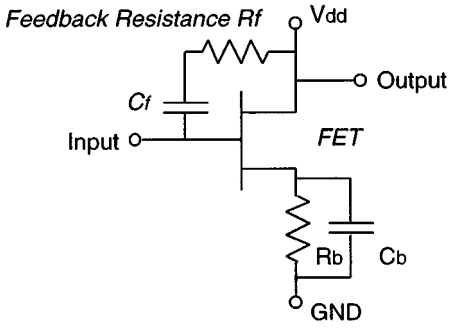

Fig. 1. Circuit schematic of the wide-band amplifier IC.

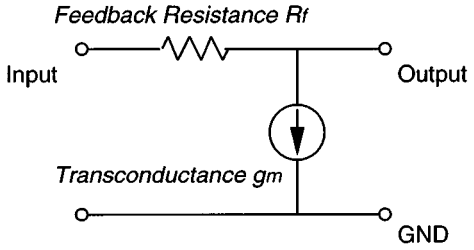

Fig. 2. Equivalent circuit with feedback resistance R_f and constant current source.

II. Design

A. Circuit

Fig. 1 shows the circuit schematic of the present wide-band amplifier IC. The IC consists of an FET, a feedback resistor R_f, and a dc-blocking capacitor C_f. We designed a wide-band amplifier IC that achieves a 12-dB gain from 100 MHz to 3 GHz at a supply voltage of 2 V and an operation current of 10 mA.

Fig. 2 shows a small-signal equivalent circuit that consists of the feedback resistor R_f and a constant current source. Parasitic components such as $C_{\rm gs}$ and $C_{\rm gd}$ are omitted because these

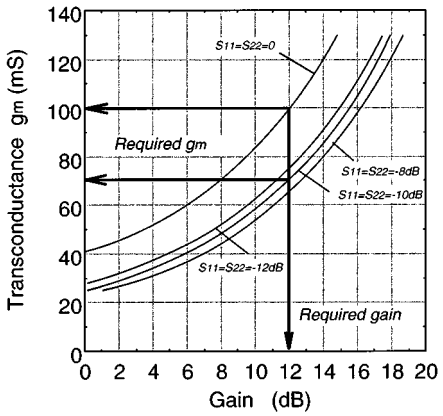

Fig. 3. Return-loss dependence of the transconductance as a function of the gain.

components do not strongly affect the RF characteristics in the low-frequency range. In order to reduce the operation current of the wide-band amplifier, we calculated the relationship between the transconductance and gain for varying return loss by using the equivalent circuit. The gain (S_{21}) and return loss (S_{11} and S_{22}) of the amplifier are described as follows:

$$S_{21} = 2Z_o(1 - g_m R_f) \Big/ \Big(R_f + Z_o(2 + g_m Z_o)\Big) \quad (1)$$

$$S_{11} = S_{22} = (R_f - g_m Z_o^2) \Big/ \Big(R_f + Z_o(2 + g_m Z_o)\Big) \quad (2)$$

where Z_o is the characteristic impedance (50 Ω).

Fig. 3 shows the return-loss dependence of the transconductance as a function of small-signal gain. This relationship is calculated from (1) and (2). Since S_{11}, S_{22}, and S_{21} are design parameters, and R_f and g_m are circuit parameters, the relationship between the transconductance and the gain (S_{21}) is obtained from (1) and (2) by determining the return loss. A g_m over 100 mS is required to obtain a gain over 12 dB under complete matching conditions, which results in increasing the operation current. However, introducing an off-matching reduces the required transconductance for the gain of 12 dB, which leads to the decrease of the operation current. The required transconductance is 70 mS for the gain of 12 dB and the return loss of -10 dB.

B. Device

It is necessary for FET's to achieve the required transconductance at lower drain current. Increasing the gatewidth (W_g) and operating the gate bias near pinchoff gives the required transconductance with lower drain current. However, it causes gain degradation in the high-frequency range due to the decreasing of the f_T (cutoff frequency).

Fig. 4 shows the gate-length dependence of the measured transconductance as a function of drain current for an FET with gatewidth (W_g) of 1000 μm. The f_T (cutoff frequency) of the FET's were measured at various drain currents. Constant f_T curves are then also plotted in Fig. 4. Increasing the f_T widens the bandwidth of the IC. Since the f_T of the FET is required

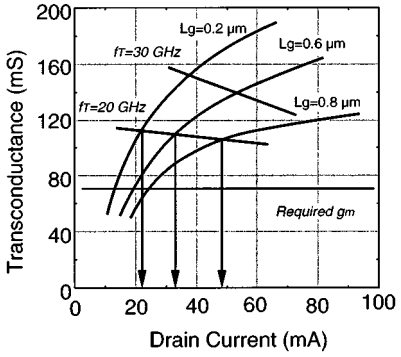

Fig. 4. Gate-length dependence of the transconductance as a function of drain current.

to be several times the bandwidth of the IC, we chose f_T of 20 GHz.

The operation current is reduced by shortening the gate length (L_g) on the constant f_T curve of 20 GHz, as shown in Fig. 4. Namely, the operation current can be reduced from 48 to 22 mA by shortening the gate length (L_g) from 0.8 to 0.2 μm. Furthermore, the operation current of the IC can be reduced by narrowing the gatewidth (W_g) because the transconductance for the required gain of 12 dB is not 110 mS, but 70 mS, as shown in Fig. 4. Actually, reducing gatewidth (W_g) with constant drain current density do not deteriorate f_T. Therefore, an FET with gate length (L_g) of 0.2 μm is essential to reducing the operation current to less than 10 mA, which is the design goal of an operation current. A 0.2-μm gate MODFET fabricated by using a phase-shift lithography technique was then employed.

III. Fabrication

A newly developed 0.2-μm process employs a phase-shifter–edge–line (PEL) method, which is a type of phase-shift lithography technique [4]. Phase-shift lithography makes a dark stripe of 0.2 μm by interference of i-line light. A phase-shift mask is a conventional stepper mask where a transparent film of the phase shifter is patterned on the mask. Since the phase of the incident i-line light is shifted by 180° by the shifter, the light intensity is weakened by the interference along the border of the phase shifter. Fig. 5 shows the 0.2-μm line of the posi-type photoresist obtained by the PEL method. This technique is more cost effective than an electron-beam lithography technique.

The present IC also employs STO ($SrTiO_3$) capacitor technology [5]. The STO capacitor saves the area consumption owing to its high permittivity. The typical dielectric constant of STO is 100, which is more than 15 times higher than that of conventional SiN. The STO film maintains a high dielectric constant from dc to over 10 GHz.

Fig. 6 shows the process flow of the present IC. The starting material is an epitaxial wafer grown by using MOCVD. The epitaxial structure of the wafer is an AlGaAs/GaAs heterostructure where a delta-doped layer is inserted in the AlGaAs layer. The 0.2-μm dummy gates of photoresist are fabricated by using the phase-shift lithography. The gate pattern was then defined by the liftoff of SiO_2 film. STO capacitors were fabricated by using low-temperature sputtering. STO film was sputtered at 200 °C to

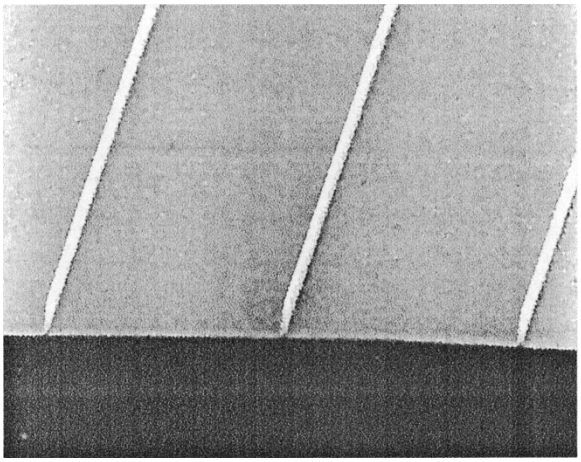

Fig. 5. SEM cross section of the dummy gate of the photoresist obtained by the PEL method.

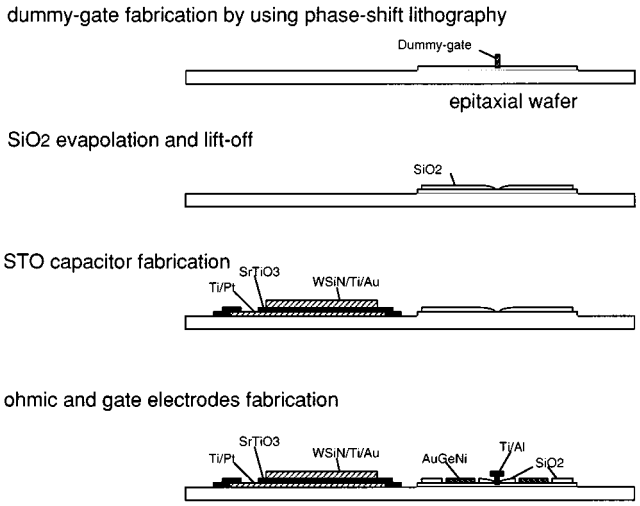

Fig. 6. Process flow of the present IC.

avoid the deterioration of impurity profile in the epitaxial structure. Gate and ohmic electrodes are then fabricated. The gate and ohmic materials are Ti/Al and AuGeNi, respectively. Fig. 7 shows a cross-sectional view of the fabricated MODFET where T-shaped gates are repeated.

Fig. 8 shows the chip photograph of the present IC. The chip size is 500 μm by 430 μm. The MODFET, two large-capacitance capacitors, and two resistors are integrated in a relatively small chip area due to the high permittivity of the STO film.

IV. Performance

A. Gain and Return Loss

The S-parameters of the fabricated IC were measured by a vector network analyzer (Hewlett-Packard 8510B) at a supply voltage of 2 V and an operation current of 10 mA. The frequency dependence of the gain (S_{21}) and return loss (S_{11} and S_{22}) is shown in Fig. 9. The IC achieves a gain over 10 dB with a return loss less than -9 dB in the frequency range from 100 MHz to 3 GHz. The gain and return loss are almost independent of frequency because the parasitic capacitances of the 0.2-μm gate

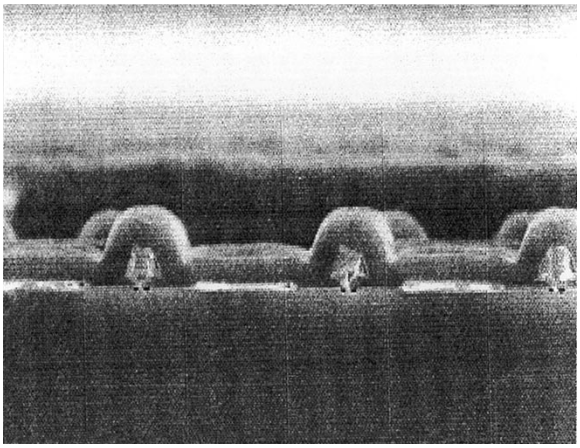

Fig. 7. SEM cross section of the fabricated wide-band amplifier.

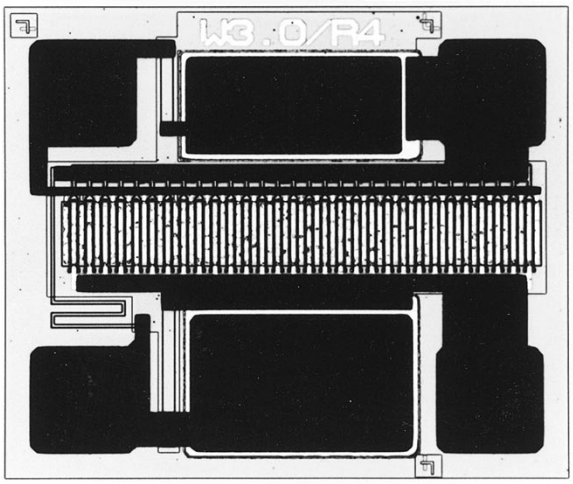

Fig. 8. Chip photograph of the fabricated wide-band amplifier.

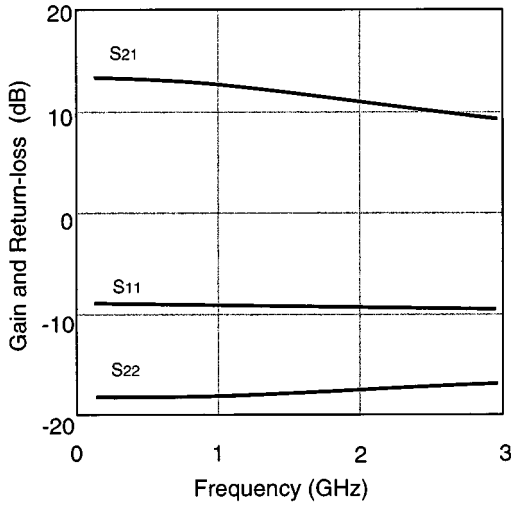

Fig. 9. Gain and return-loss performance of the wide-band amplifier. $V_{dd} = 2$ V, $I_d = 10$ mA.

MODFET are so small that these do not affect the RF characteristics of the IC in the frequency range.

The effect of shortening the gate length on reducing the operation current was confirmed. Fig. 10 shows the gate-length

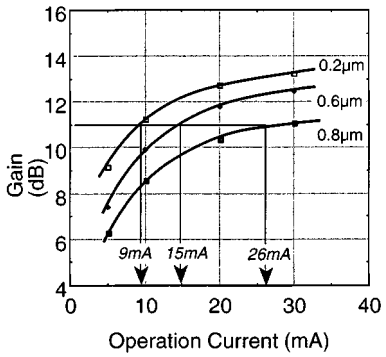

Fig. 10. Reduction of the operation current by shortening the gate length. $V_{dd} = 2$ V @2 GHz.

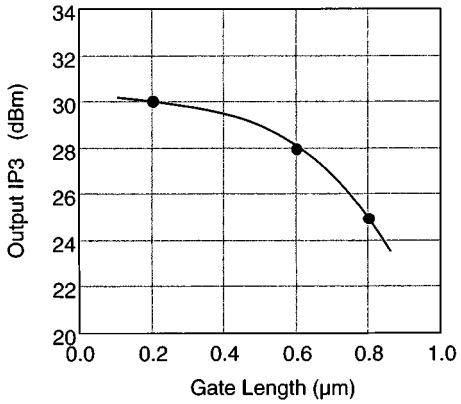

Fig. 11. Gate-length dependence of the output IP3. $V_{dd} = 2$ V, $I_d = 10$ mA @800 MHz.

dependence of the gain as a function of the operation current. The gatewidth (W_g) is 600 μm. Shortening the gate length drastically reduced the operation current. For example, the operation current was reduced from 26 to 9 mA to obtain the gain of 11 dB by shortening the gate length from 0.8 to 0.2 μm.

B. Distortion

The distortion characteristics of the present IC was evaluated. The frequencies of the input signals were 800 and 800.1 MHz. Fig. 11 shows the relationship between the output third-order intercept point (IP3) and the gate length at a supply voltage of 2 V and an operation current of 10 mA. The intermodulation distortion was reduced by shortening the gate length. The IC with 0.2-μm gate MODFET achieved the output IP3 of 30 dBm.

Fig. 12 shows the output IP3 of the present IC with a 0.2-μm gate MODFET as a function of the operation current. The highest output IP3 of 30 dBm was obtained for operation current of 10 mA.

Fig. 13 shows the frequency dependence of the output IP3. Although the output IP3 is degraded in higher frequency region, the IC achieves the output IP3 as high as 23 dBm at 1.9 GHz.

C. Noise Figure

The noise figure of the present IC was evaluated by using a noise-figure meter (Hewlett-Packard HP8970A). The bias condition was a supply voltage of 2 V and an operation current of

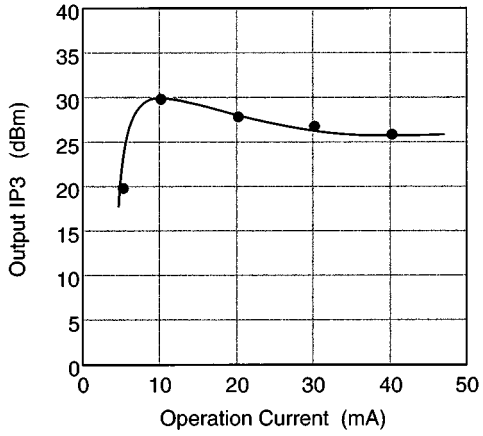

Fig. 12. Operation-current dependence of the output IP3. $V_{dd} = 2$ V @800 MHz.

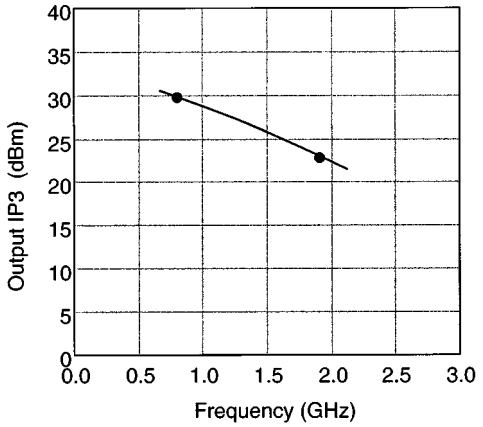

Fig. 13. Frequency dependence of the output IP3. $V_{dd} = 2$ V, $I_d = 10$ mA.

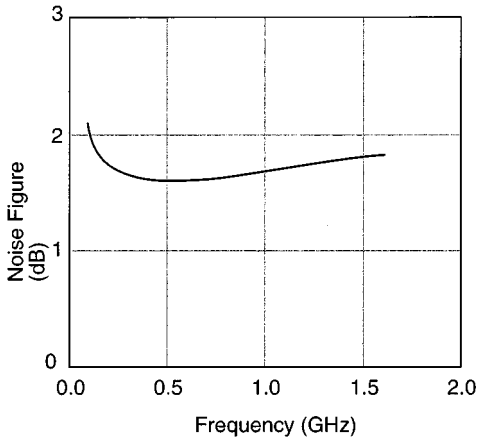

Fig. 14. Frequency dependence of the noise figure. $V_{dd} = 2$ V, $I_d = 10$ mA.

10 mA. The fabricated IC achieved noise figure less than 2 dB in the frequency range from 100 MHz to 1.6 GHz, as shown in Fig. 14.

We evaluated the operation-current dependence of the noise figure. Fig. 15 shows the relationship between noise figure and operation current at 800 MHz. The present IC achieves noise figure less than 2 dB for operation current of more than 7 mA.

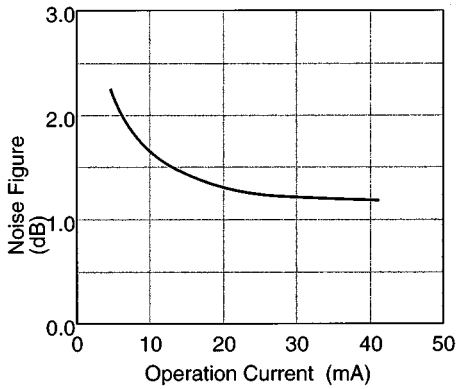

Fig. 15. Operation-current dependence of the noise figure. $V_{dd} = 2$ V, $I_d = 10$ mA @800 MHz.

V. Conclusion

We have developed a low-current and low-distortion wide-band amplifier IC employing 0.2-μm gate delta-doped MODFET fabricated by using phase-shift lithography. The methodology of reducing the operation current of the IC's was discussed from the equivalent circuit. The fabricated wide-band amplifier have achieved a gain over 10 dB with a return loss less than -9 dB for the operation current of 10 mA in the frequency range from 100 MHz to 3 GHz. An extremely high-output IP3 of 30 dBm has been obtained at the same bias point. The fabricated IC keeps a fairly good noise figure less than 2 dB in the frequency range. These low-current and low-distortion wide-band amplifier IC's are useful for mobile communication handsets.

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References

[1] E. Ulrich, "Use negative feedback to slash wideband VSWR," *Microwave*, vol. 17, no. 10, pp. 66–70, 1978.
[2] K. B. Niclas, W. T. Wilser, R. B. Gold, and W. R. Hitchens, "A 350 MHz–14 GHz GaAs MESFET amplifier using feedback," in *IEEE Int. Solid-State Circuits Conf.*, 1980, pp. 164–165.
[3] ——, "The matched feedback amplifier: Ultrawide-band microwave amplification with GaAs MESFET's," *IEEE Microwave Theory Tech.*, vol. MTT-28, pp. 285–294, Apr. 1980.
[4] H. P. Weidlich, J. A. Archer, E. Pettenpaul, F. A. Petz, and J. Huber, "A GaAs monolithic broad-band amplifier," in *IEEE Int. Solid-State Circuits Conf.*, 1981, pp. 192–193.
[5] M. Nishiuma, S. Nambu, M. Hagio, and G. Kano, "A GaAs monolithic low-noise wideband amplifier," *Inst. Phys. Conf. Series*, no. 63, pp. 425–430, 1981.
[6] M. Nishiuma, S. Katsu, S. Nagata, N. Ohmoto, D. Ueda, M. Kazumura, and G. Kano, "A UHF GaAs multi-stage wideband amplifier with dual feedback circuits," in *GaAs IC Symp. Tech. Dig.*, 1987, pp. 223–226.
[7] H. Takenaka and D. Ueda, "0.15-μm T-shape gate fabrication for GaAs MODFET using phase shift lithography," *IEEE Trans. Electron Devices*, vol. 43, pp. 238–244, Feb. 1996.
[8] M. Nishitsuji, A. Tamura, T. Kunishima, K. Yahata, M. Shibuya, M. Kitagawa, and T. Hirao, "Advanced GaAs-MMIC process technology using high-dielectric constant thin film capacitors by low temperature RF sputtering method," in *GaAs IC Symp. Tech. Dig.*, 1993, pp. 329–332.

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